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Advantages and Limitations of Generalized Open Pin Field Modeling For Array Connectors

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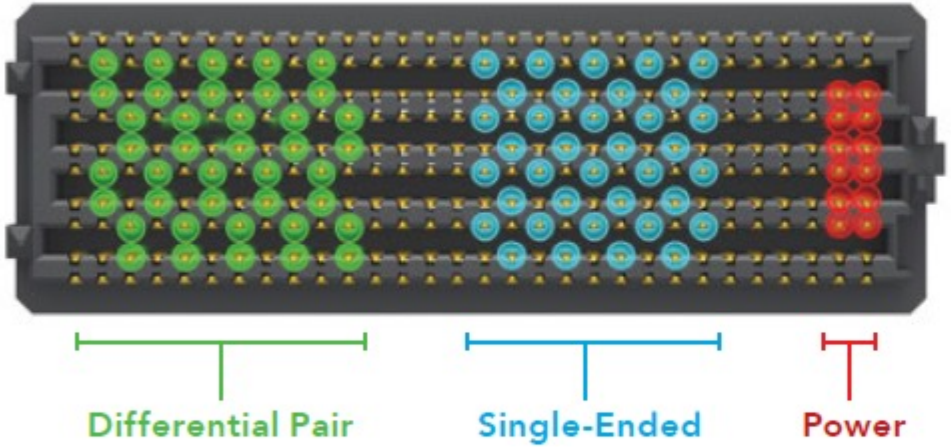
Introduction – Open Pin Field Connectors

What is an open pin field connector?

A connector that does not have dedicated ground structures

Every pin can be treated as a signal, a ground or power

It gives the flexibility to use any signal mapping a customer wants



Open Pin Field Connectors

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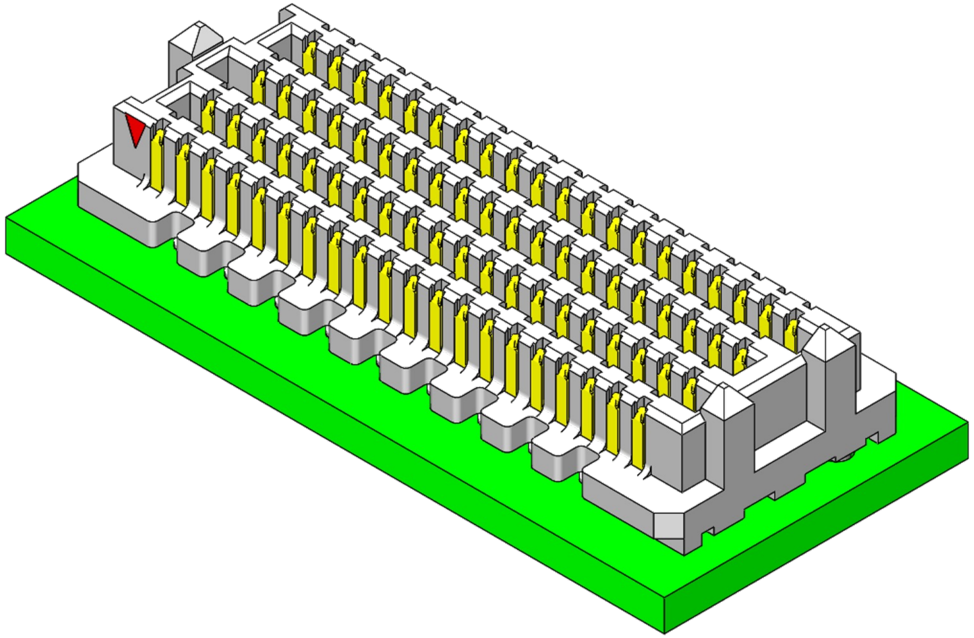
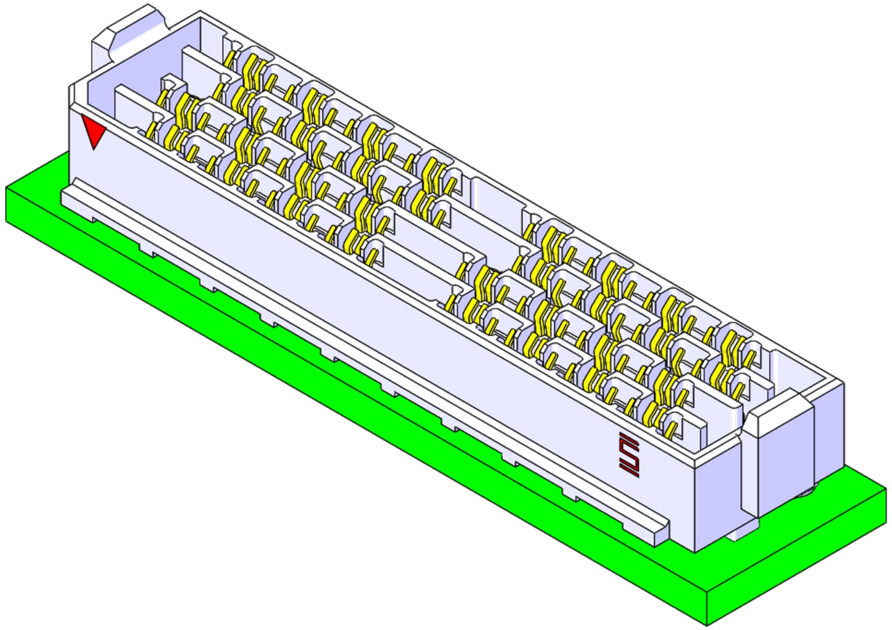
- Open pin field connector



SEARAY™

- Differential signaling aimed connector
  - Every 2 pins have 2 dedicated grounds



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Open Pin Field Connector Model Options

Several different modeling options:

- With a large port that covers all the pins
- Using a single port for each pin
- “Cutting” the model into cascaded parts
- Model the complete signal path from PCB to PCB

Clearly there are frequency limits to which you can treat each portion separately

- Reference our gEEk® spEEk Webinar from Aug. 2022
- Cascaded or End-to-End Models: What Do We Give Up??

Open Pin Field Connector Model Options

Consider these scenarios:

- Application has no need of 20+ GHz performance
- Early design study
- Connector has low and high-speed signals - need to sanity check low-speed signals quickly

Do these need full 3D simulations for every possible signal assignment?

Can a single model cover all possible use cases of signal assignment? In other words, an "All Signal" model?

Towards “All Signal” – Step 1

- The study was made on a standard 7 mm stack height SEARAY™
- The pin and solder parts were substituted by cylinders for this exercise
  - Easier and faster to simulate and manipulate inside the tool
- Test different approaches for simulating all signal models and see which are better by using different port scenarios
- Let’s start with the simplest arrangement, with every pin treated as a signal. See next slide.

“All Signal” Without Dedicated Returns

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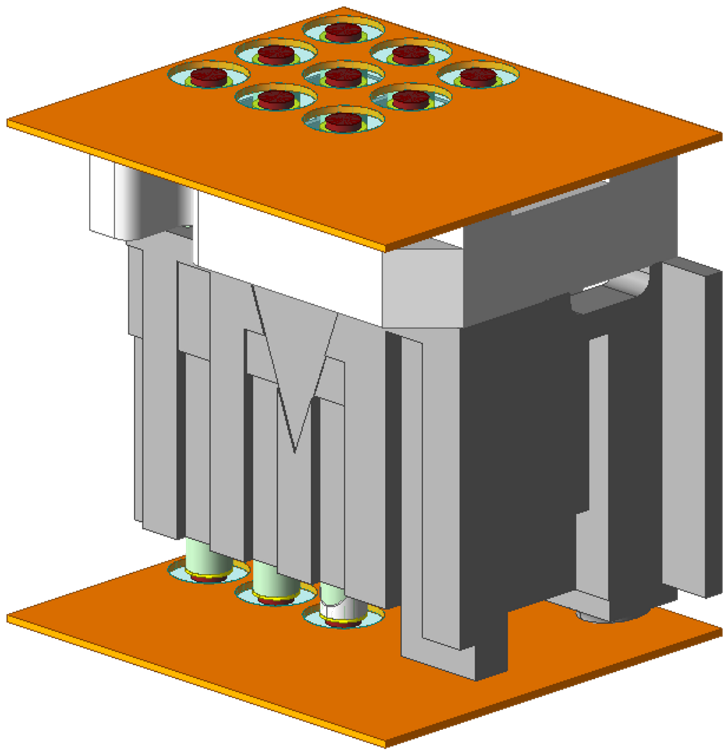
- The pins are treated independently
- A PEC sheet is placed on either end of the connector
- Circular openings are created on each sheet and 50 Ohm coax ports are created
  - This will introduce some error
  - The smaller the opening, the more the mismatch to pin fields
  - If opening is too large, GND web becomes useless
  - This error is ignored for the moment



"All Signal" Simulation Results

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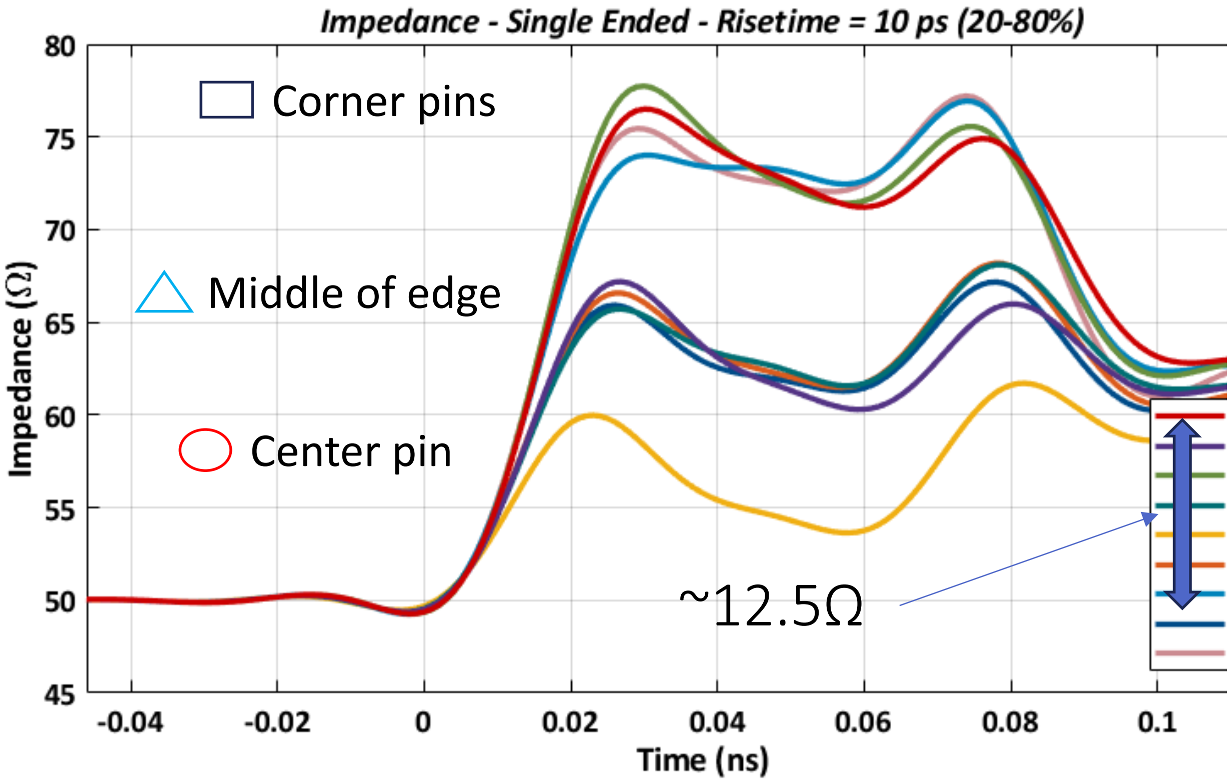
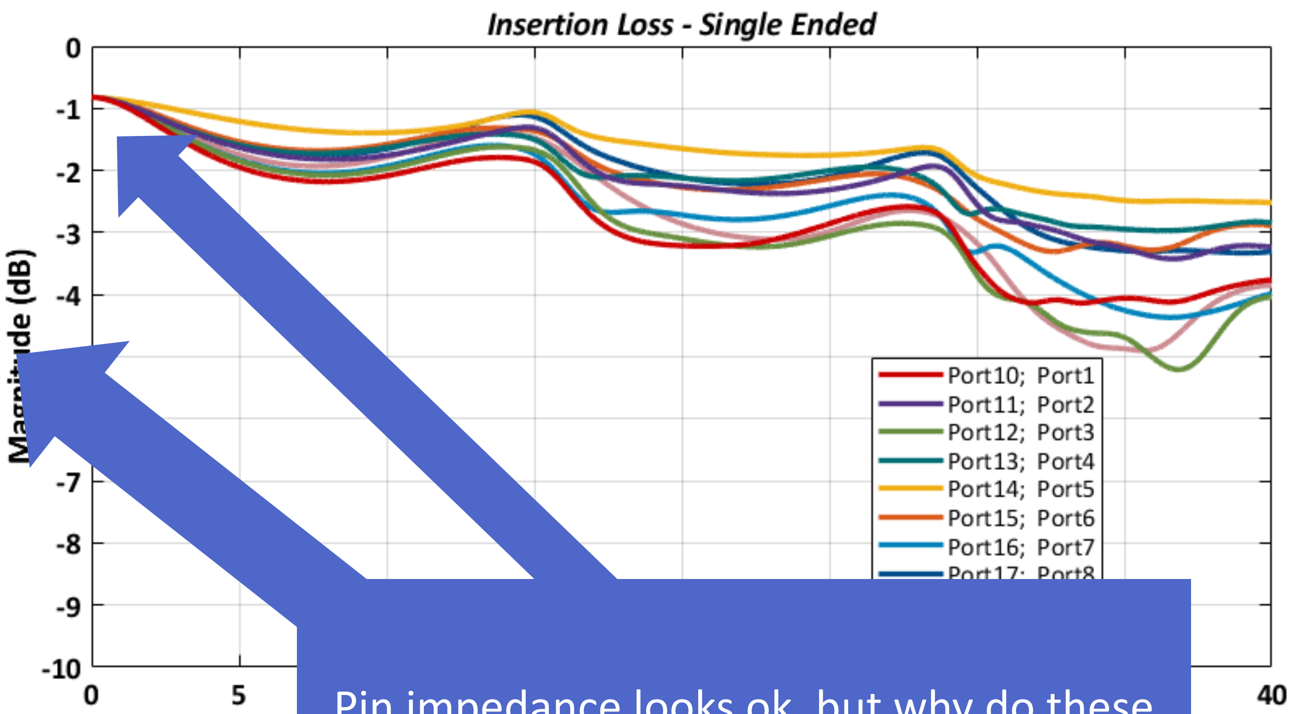
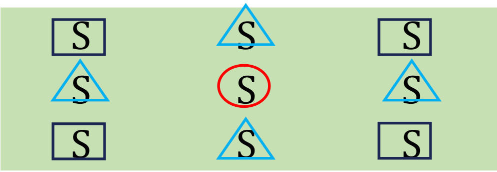




Pin impedance looks ok, but why do these points look weird?



Can Every Pin be Treated as a Signal?

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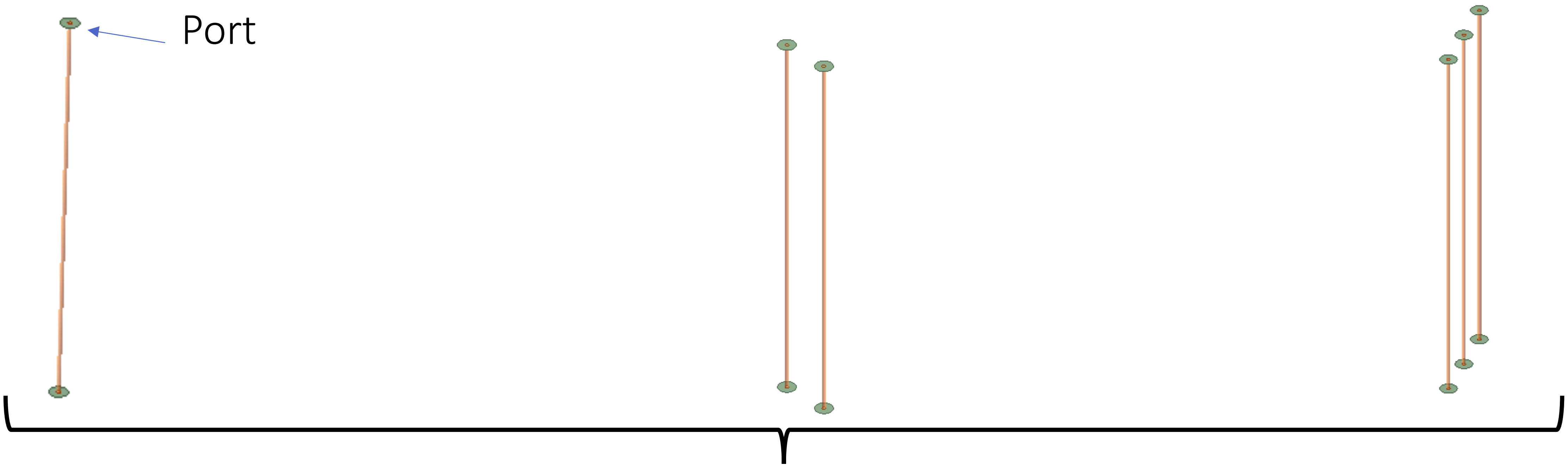
Consider the 3 examples below.



Same pin characteristics. Just different number of pins: 1, 2, and 3.
No designated return pins, all treated as signals.

Can Every Pin be Treated as a Signal? - Results

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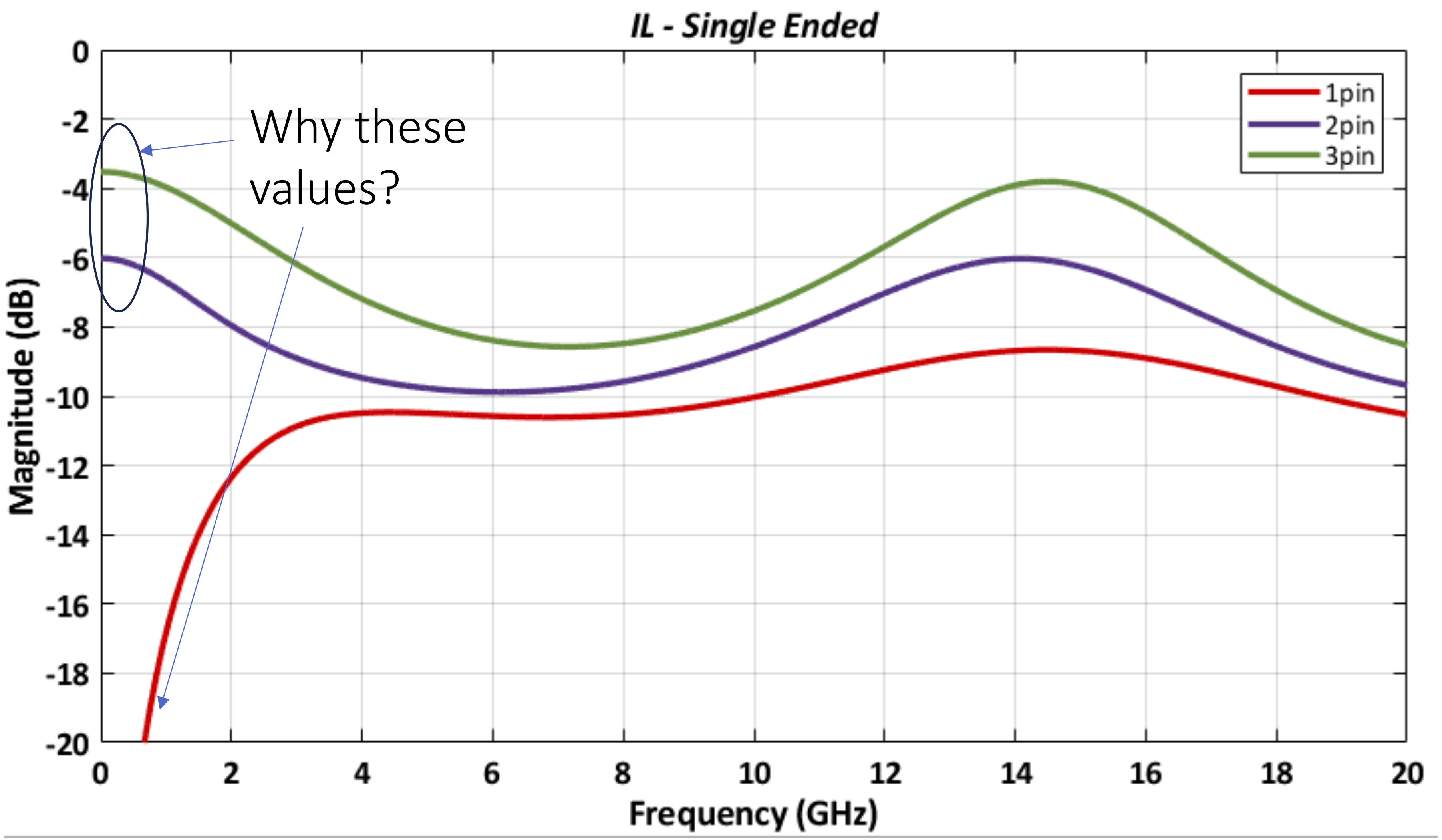

Can Every Pin be Treated as a Signal? – Signal Return

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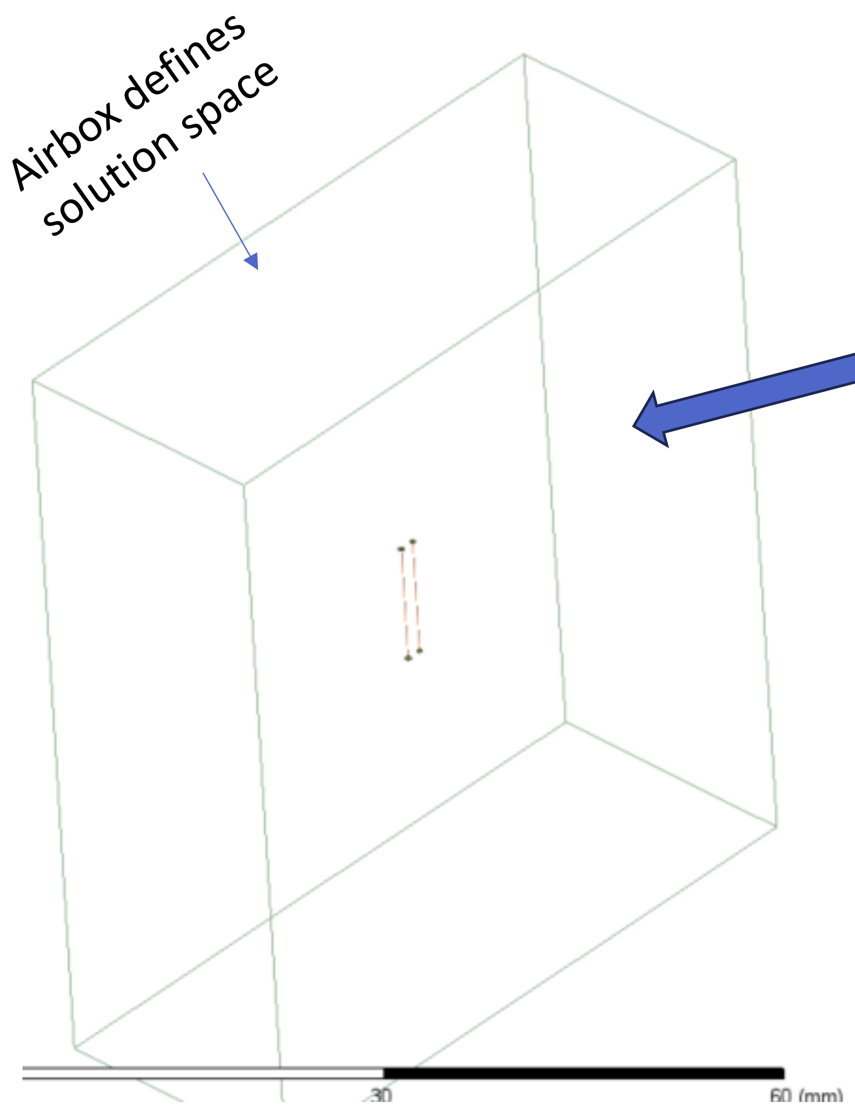
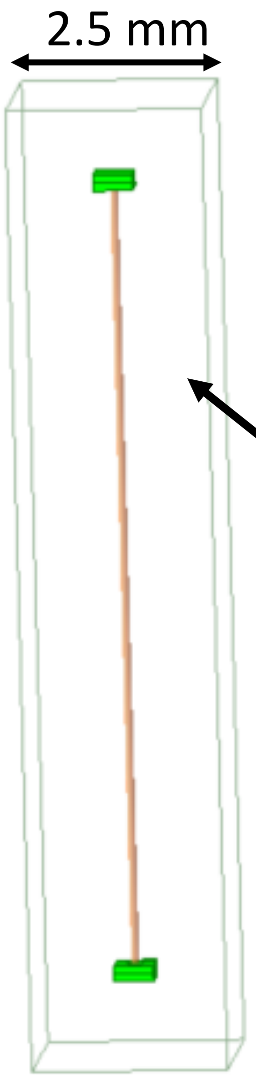


Without designated return pins, the radiation boundary (universe) and coupling to other signal pins become the de-facto return paths

The Case of Just One Pin



Airbox is everywhere at least 1 mm from pin

|E| @ 1 GHz

Field is “off the scale” here

Air box extents are not far enough away for E field component to be perpendicular to airbox faces

The Case of Just One Pin

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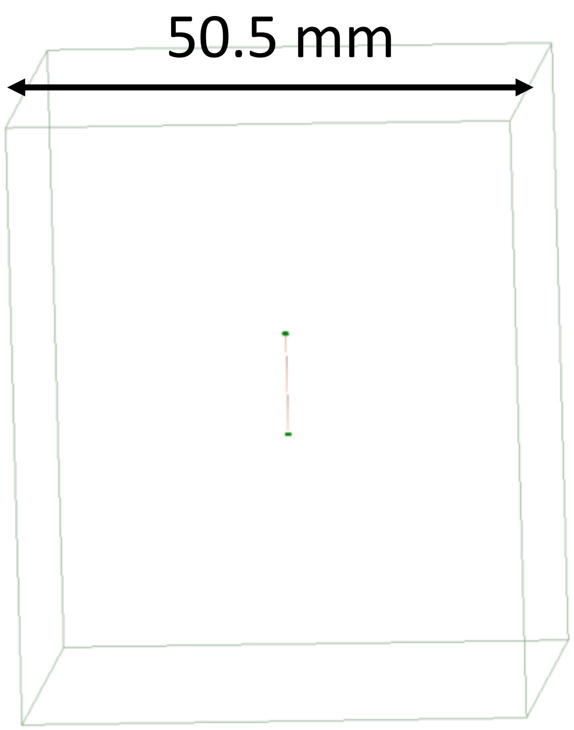
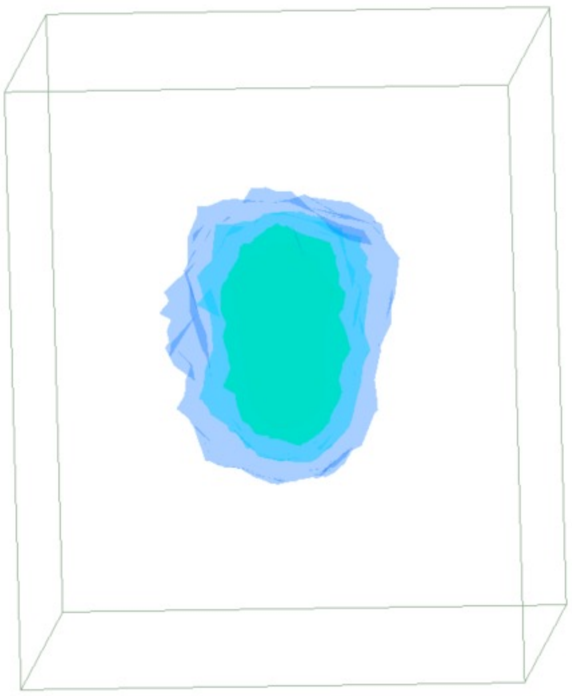


Same pin as before.
Airbox, however, is everywhere at least 25 mm from pin

|E| @ 1 GHz



Same field strength scale as before.

Airbox is now far away from signal.

The Case of Just One Pin - S_{21}

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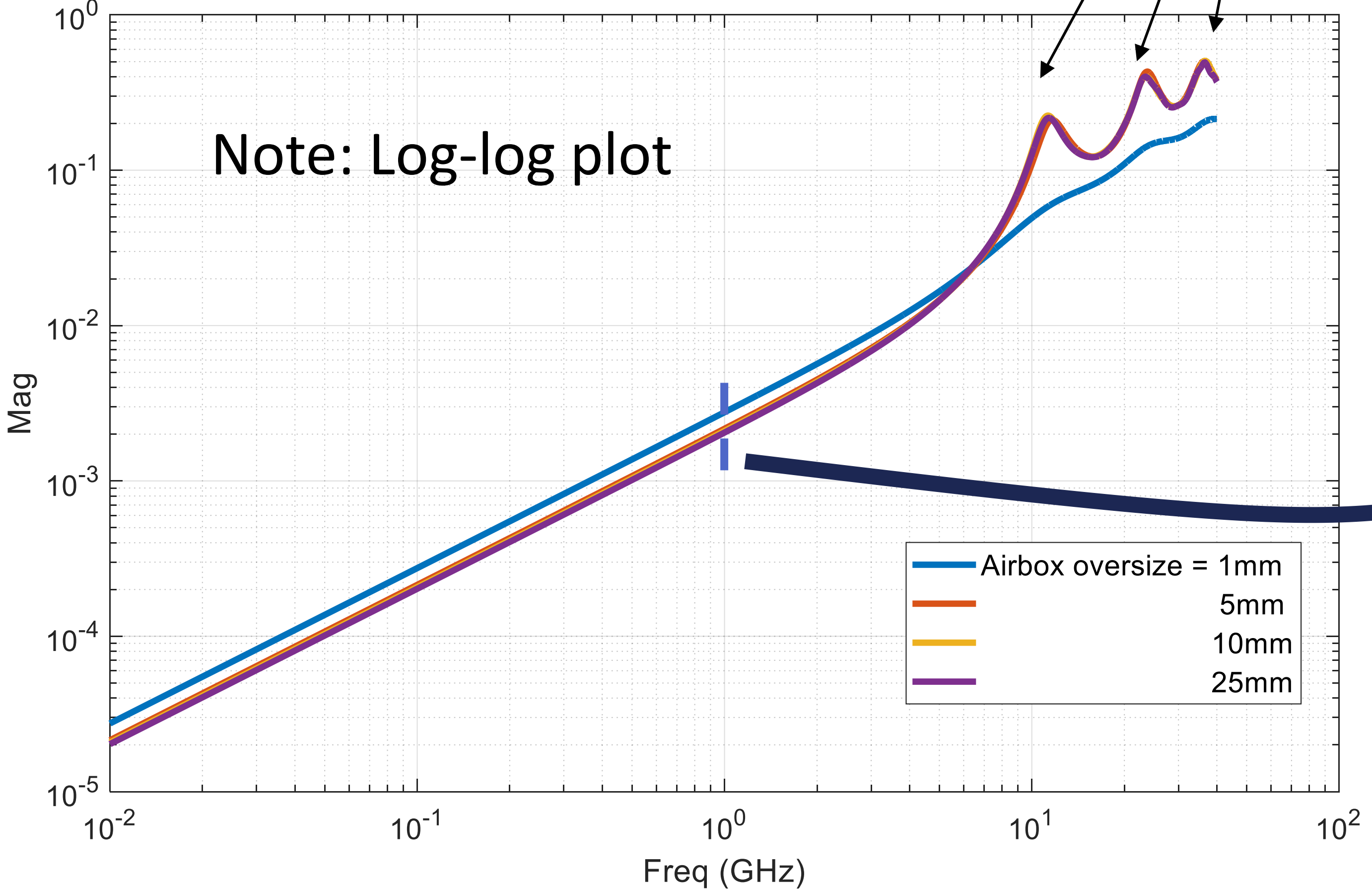
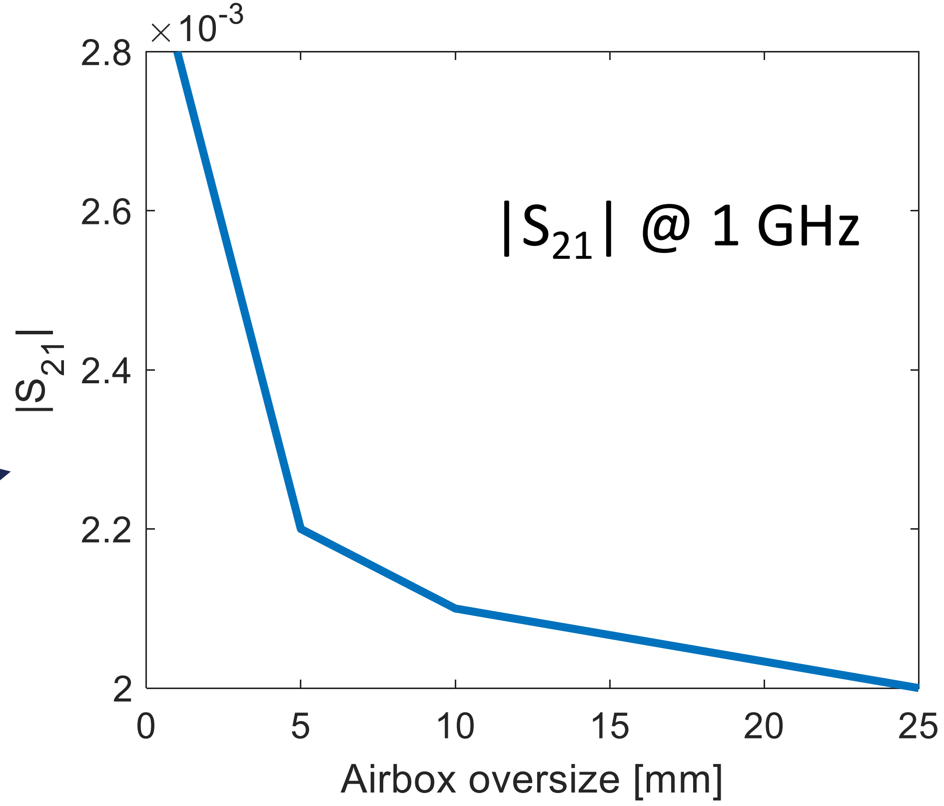
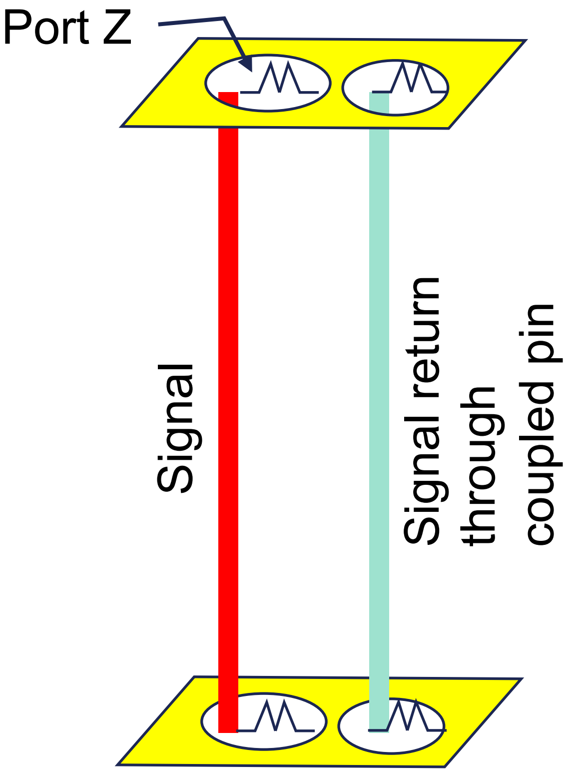
Pin length driven resonances

$|S_{21}|$



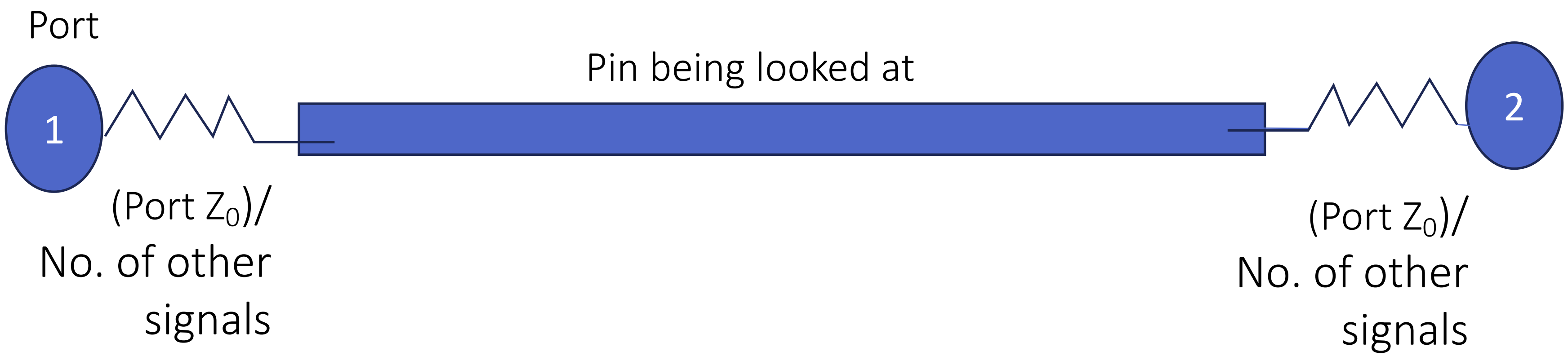


What Happens @ DC?



2 pin case

At DC, all the port Zs of the coupled pins are in parallel



For 2 conductor case, Port Z0 = 50, Additional pins = 1, therefore there is 100 Ohms in series with signal → S21 | DC = S21 (100 Ohm resistor) = -6 dB

For 3 conductor case, Port Z0 = 50, Additional pins = 2, therefore there is 50 Ohms in series with signal → S21 | DC = S21 (50 Ohm resistor) = -3.5 dB

Properly Defined Return Path

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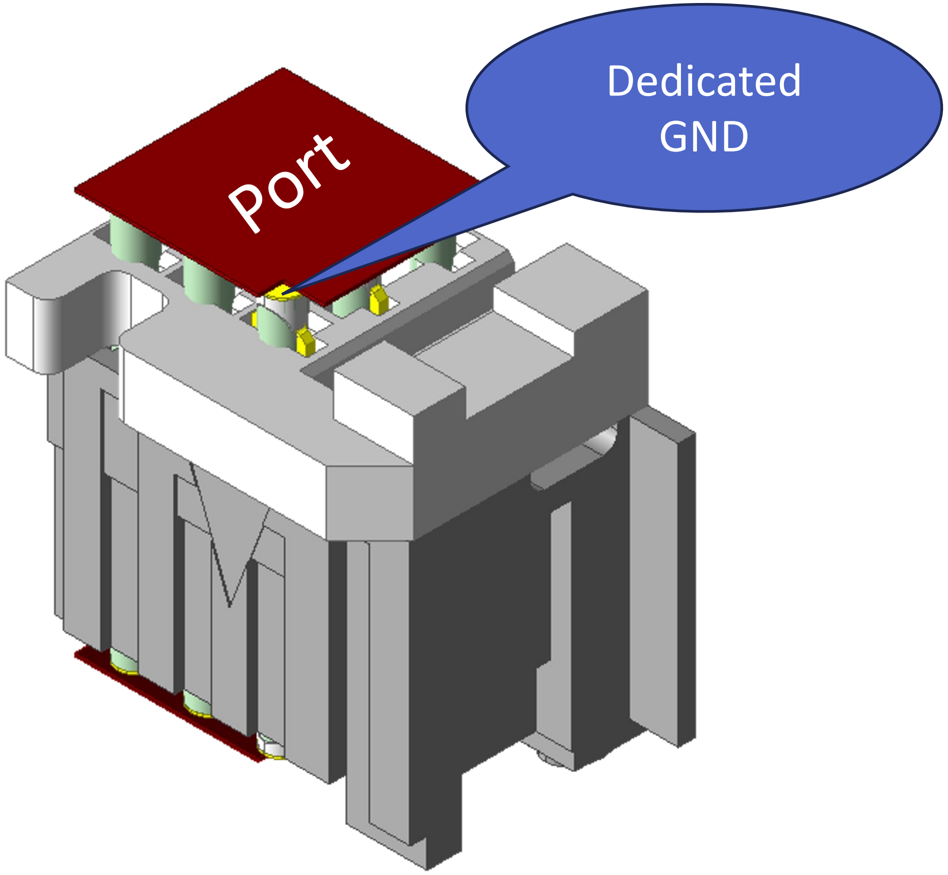
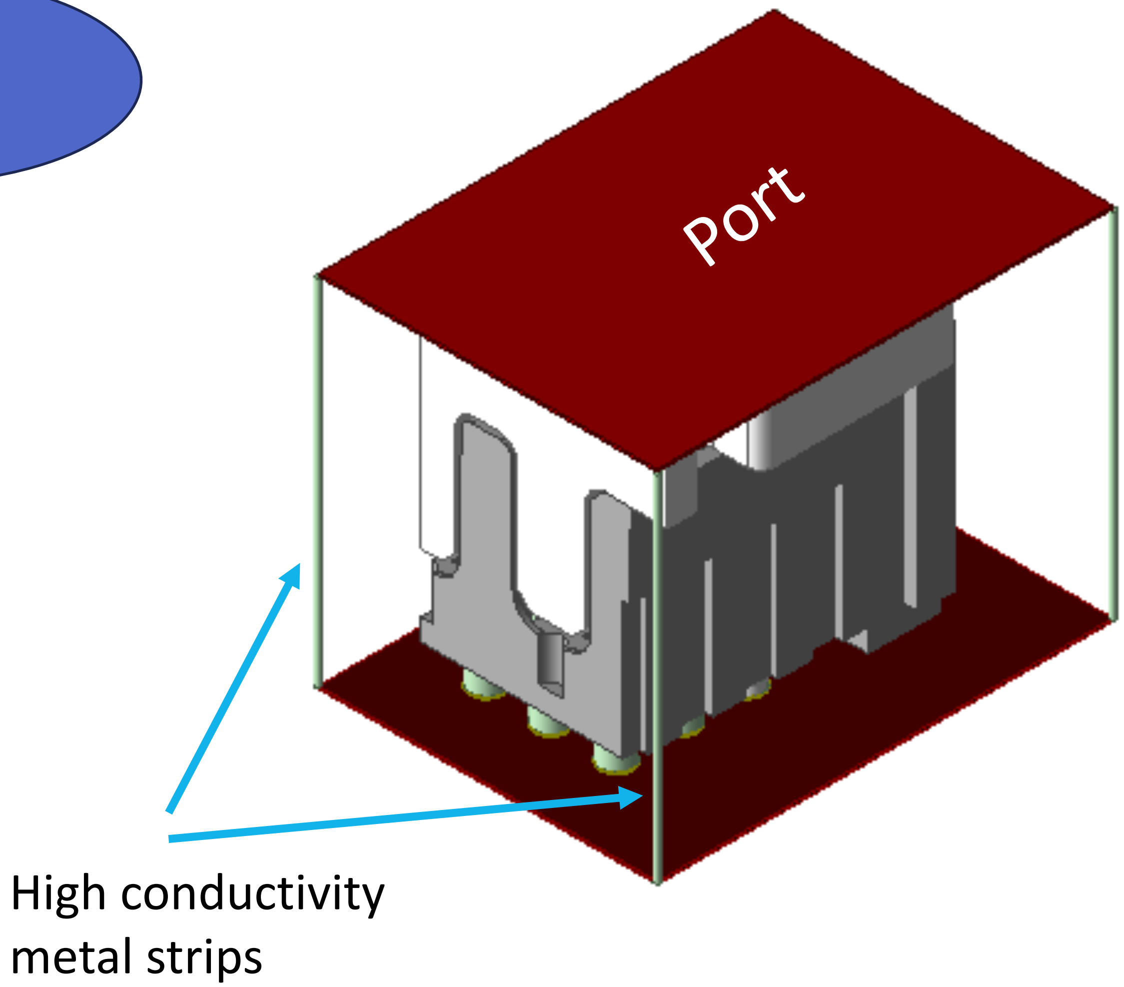
Model 2:
One connector pin is dedicated return





Model 3:
Ports connected with metal strips.
All connector pins are signals

Model 2 & 3 - Results

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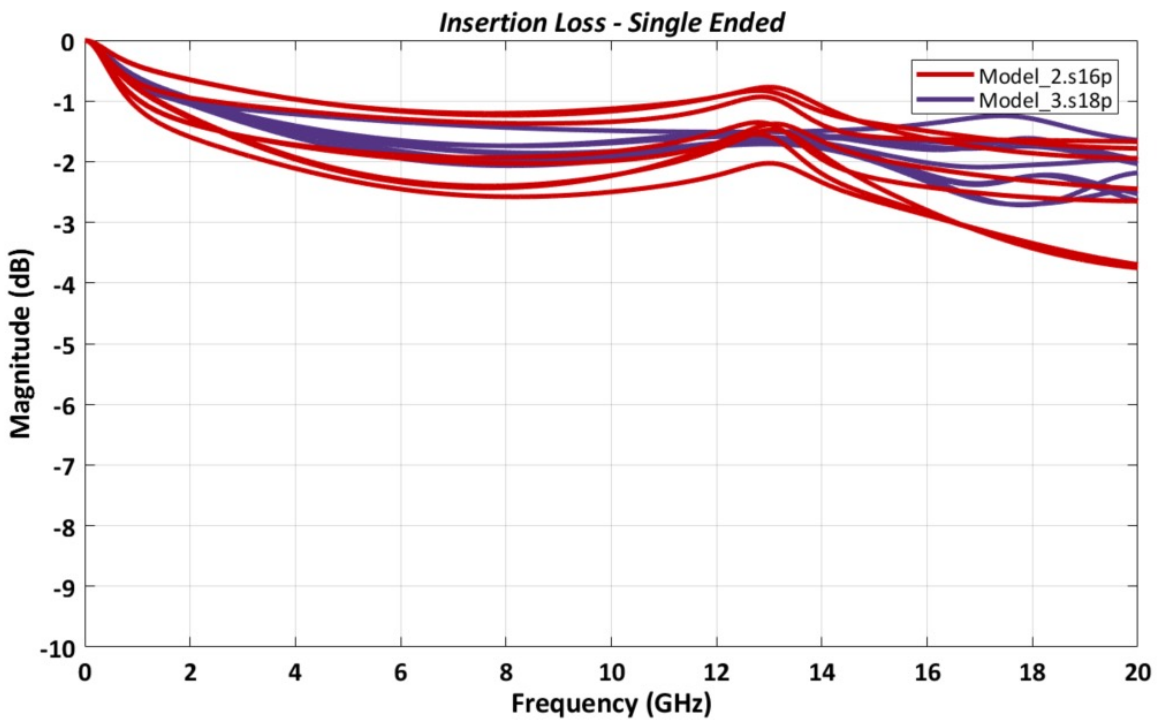
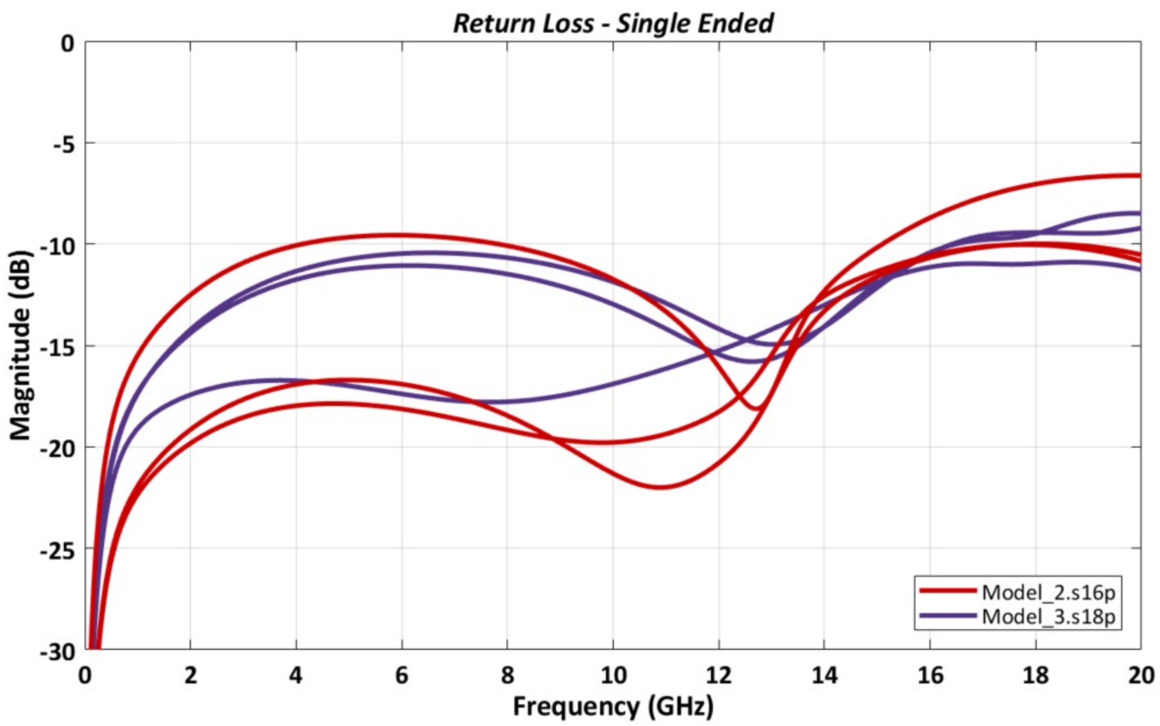




No offsets or convergence issues seen in either model.
Explicitly defining a return path returns good results!!

Towards "All Signal" – Step 2

Clearly a properly designated return path is needed.

Is any reasonable return path definition acceptable?

Let's test this:

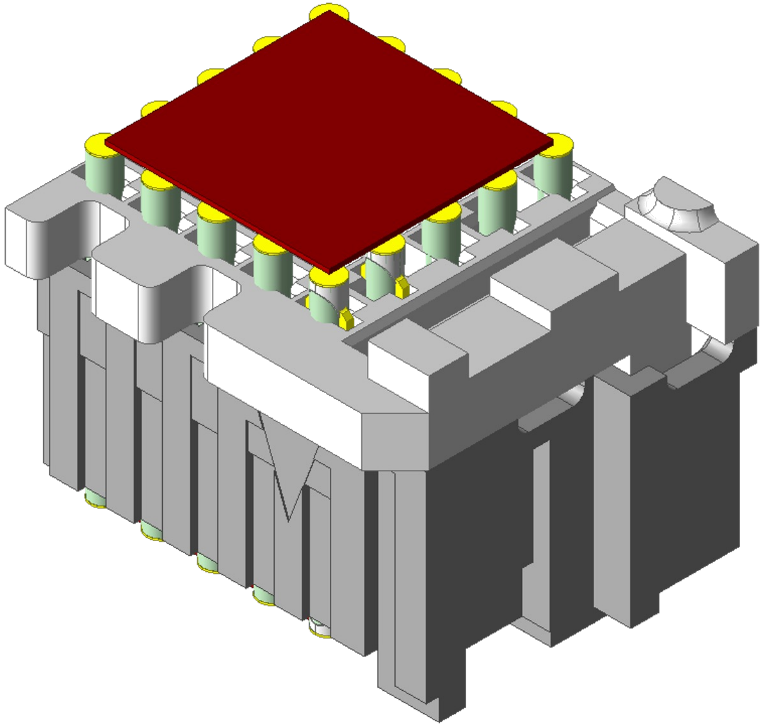
- Used a 5 x 5 arrangement
- Differing numbers of perimeter pins are dedicated GNDs
  → A large port can be properly referenced
- 4 different port arrangements studied. Next slides

Model 4 & 5

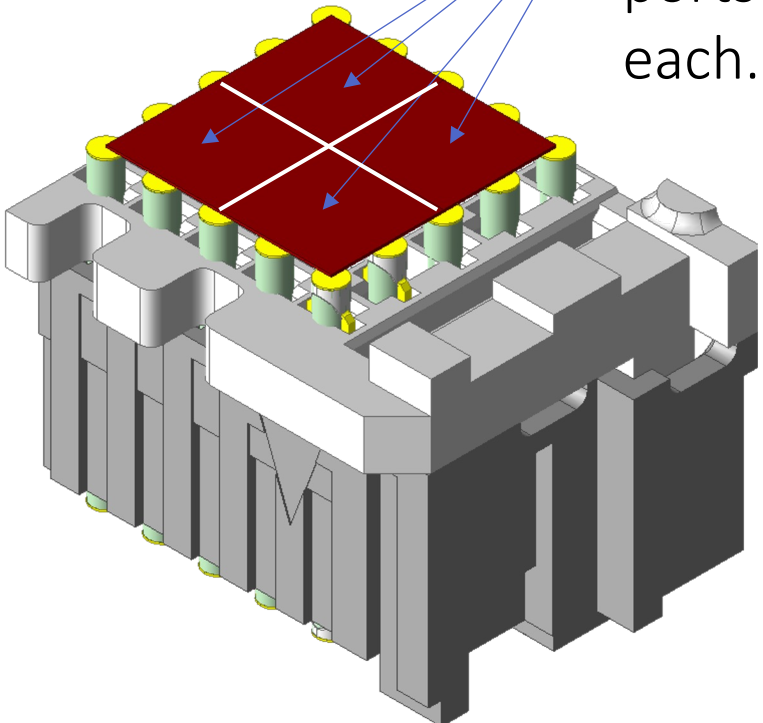
- Simulation made using rectangular ports in a 5 x 5 grid. Port boundary touches dedicated return pins
- Model 4 has a single rectangular port (9 signals) applied on each side
- Model 5 is an 8 - model. 4 ports are applied to each side

4 independent ports with 1 signal each.

Model 4



Model 5



Model 6 & 7

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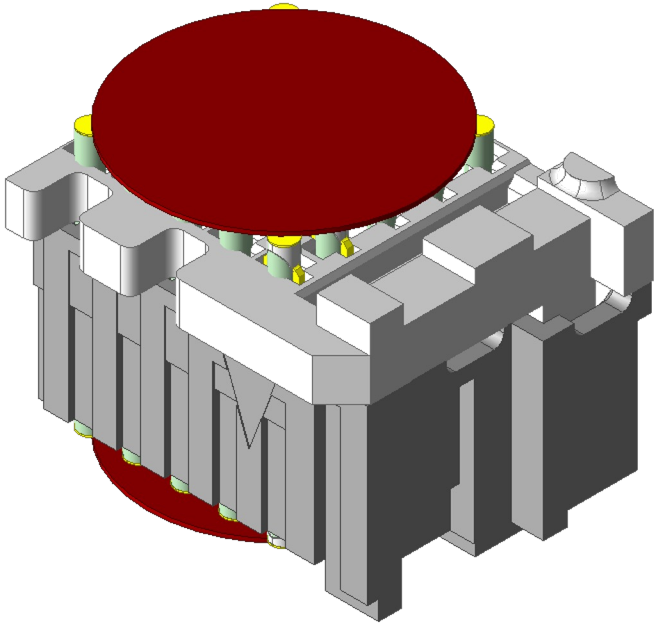
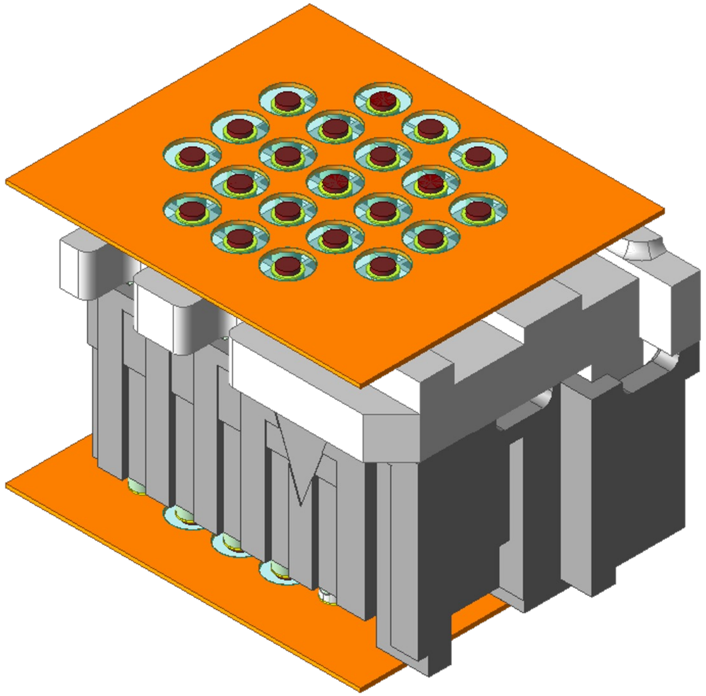
- Simulation made using circular ports in a 5 x 5 grid
- Corner pins assigned as returns
- Port partially cover the returns

Model 6



- Simulation made using coax ports in a 5 x 5 grid
- Corner pins assigned as returns

Model 7



Comparing Apples to Apples

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- Models 4-7 all simulate different number of pins
- To compare apples to apples, all the simulation results were post processed. Example shown below. Ports in each SP file were terminated to GND so that only 4 signals remained

	Simulation output	Post processed Touchstone
Model 4	G G G G G G S S S G G S S S G G S S S G G G G G G	G G G G G G S G S G G G G G G G S G S G G G G G G
Model 6 & 7	G S S S G S S S S S S S S S S S S S S S G S S S G	G G G G G G S G S G G G G G G G S G S G G G G G G

- Resulting reduced touchstone files are compared on the next slides

Model 4, 5, 6, & 7 - Results

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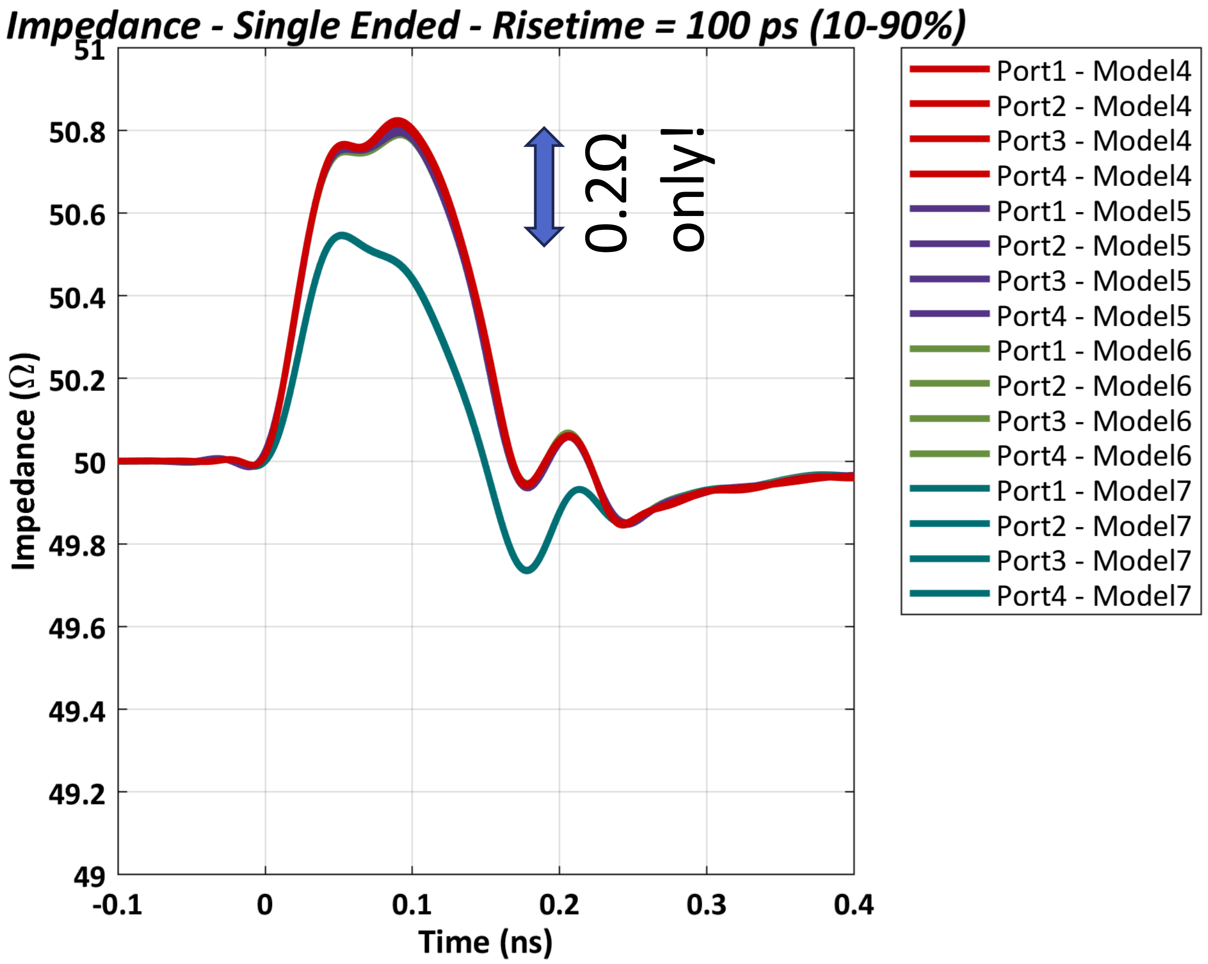
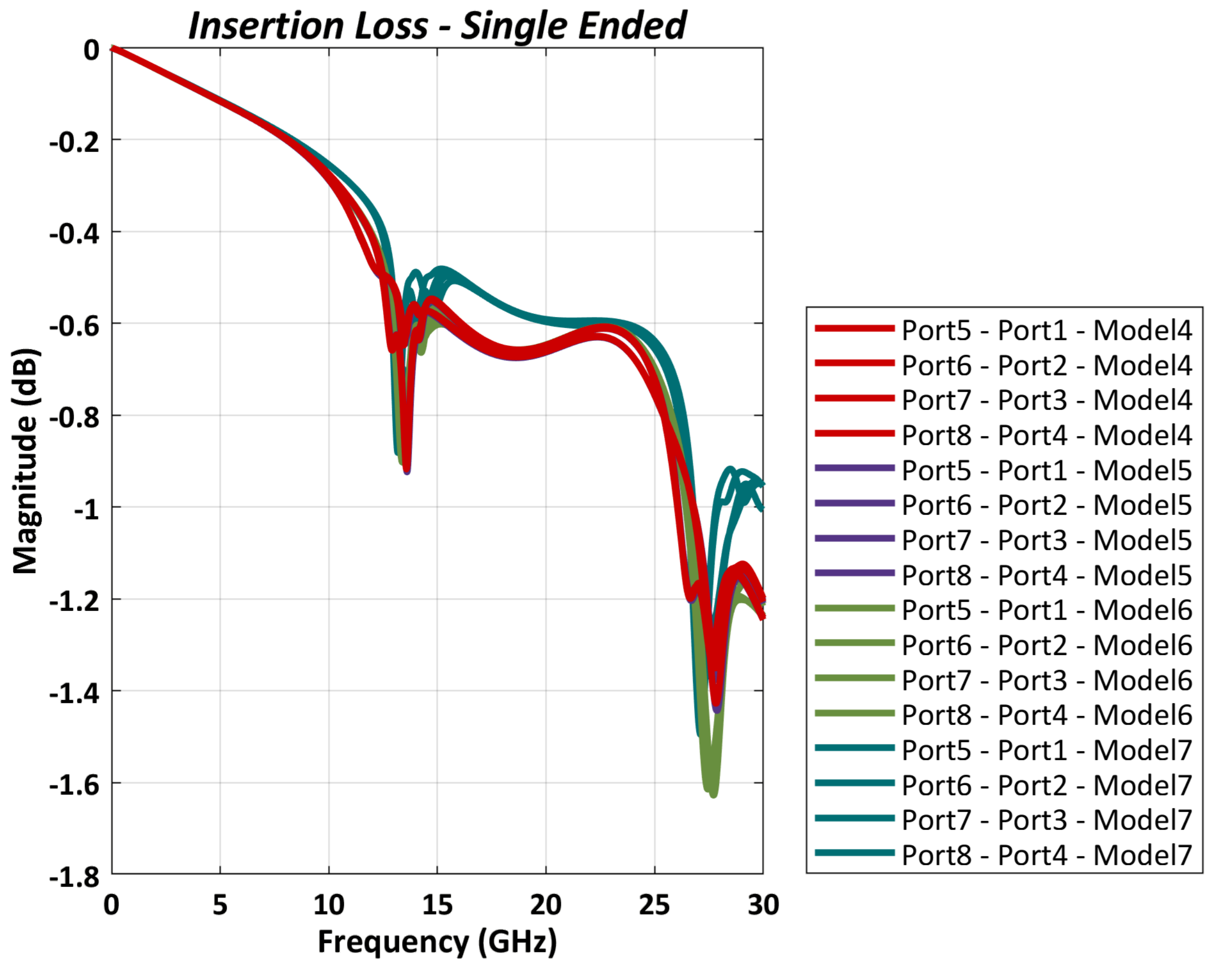
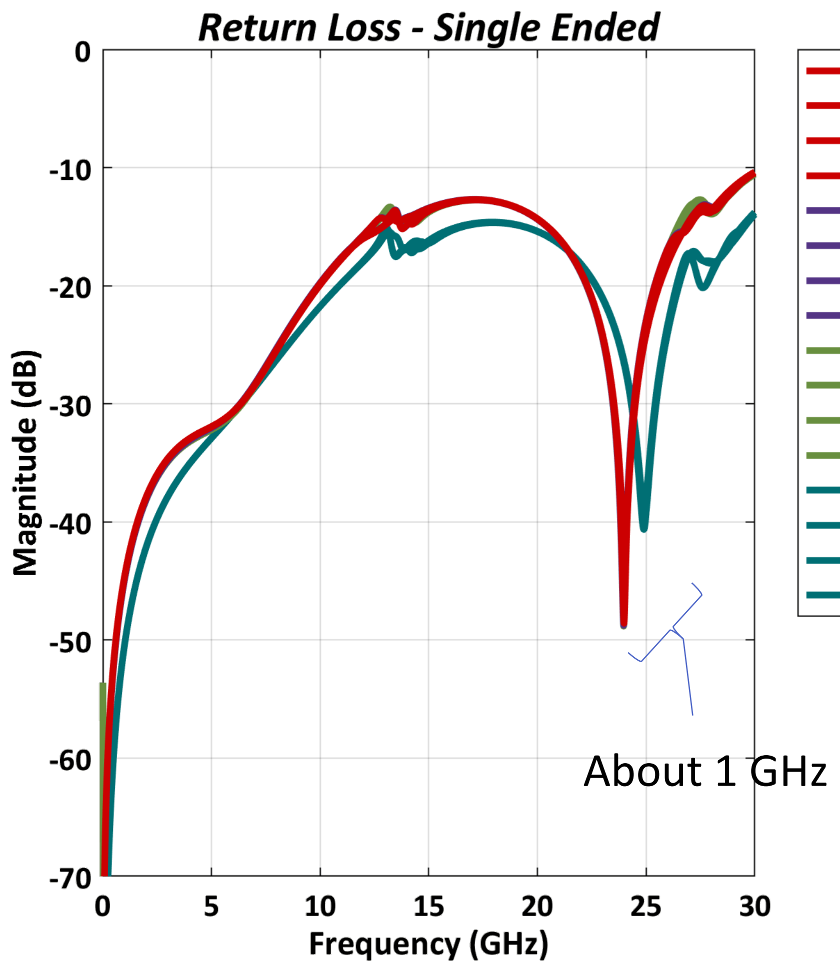
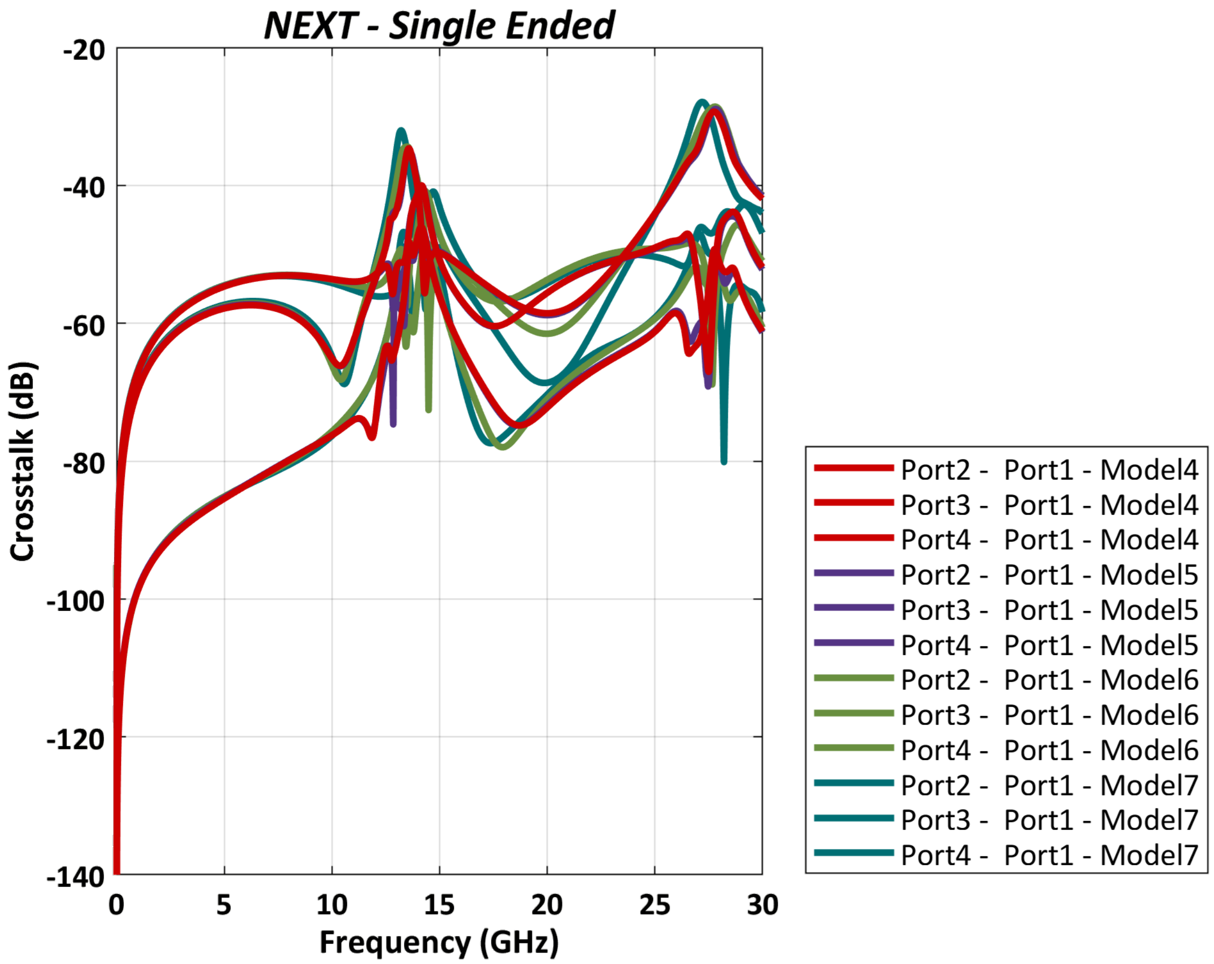




Model 4, 5, 6, & 7 - Results





Model 4, 5, 6, & 7 - Results

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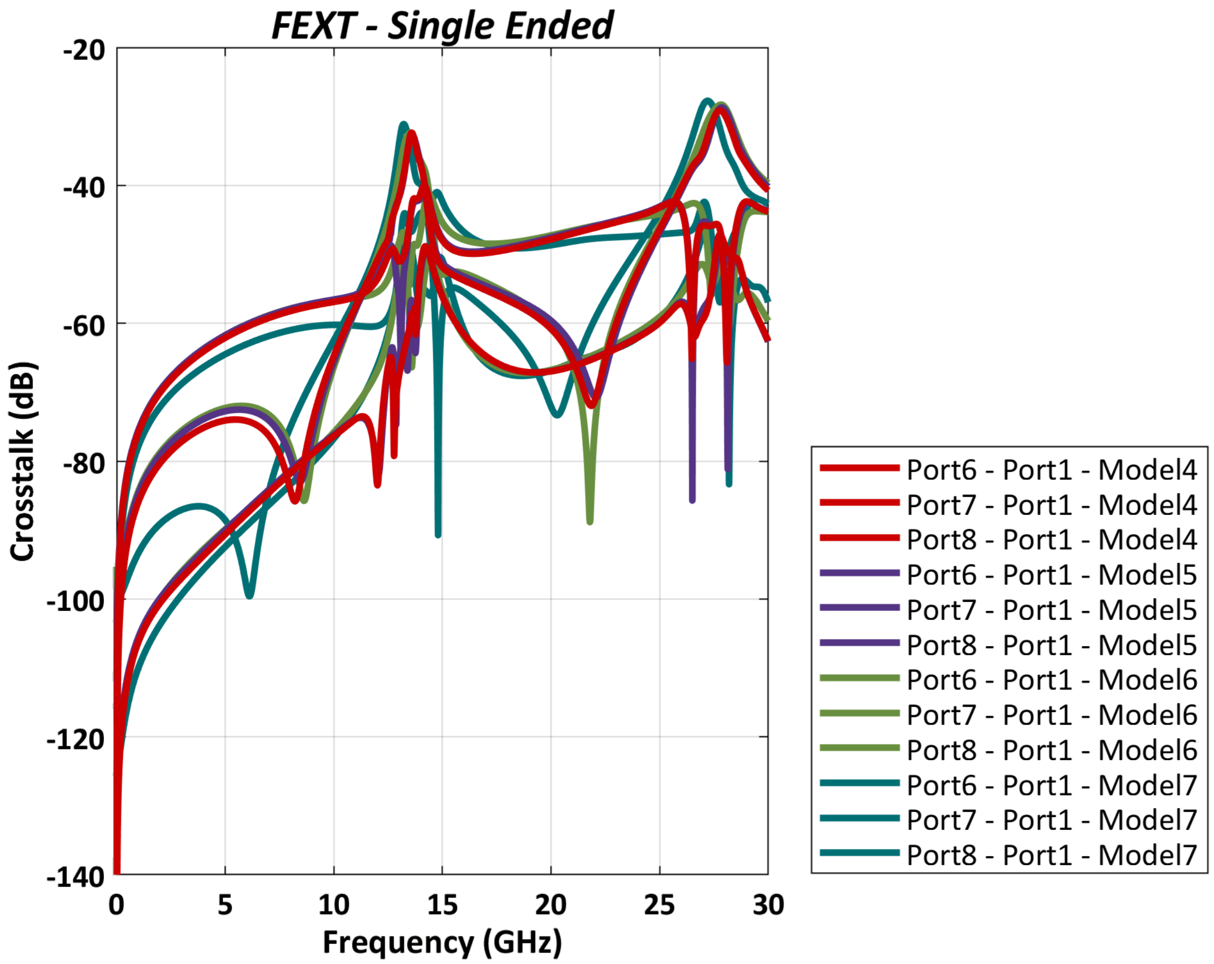

Models 4-7 takeaway:

Minor differences.

→Not addressing absolute accuracy yet, just consistency.

→Goal is to make a single model that can address all signal assignments up to ~20GHz. How do we apply this learning toward that goal?

Towards "All Signal" – Step 3

- Open pin connectors have a large number of pins.
  - For example, SEARAY™ can have up to 560 pins (14 x 40 configuration of VITA 57.4 FMC+)
- Want to make a fairly large pin count model to make this method useful
- Model 7 (each pin excited with a coax) provides a path to get there.
  - Some dedicated return pins will still be required.
  - See next slide for details.

What Have We Learned So Far?

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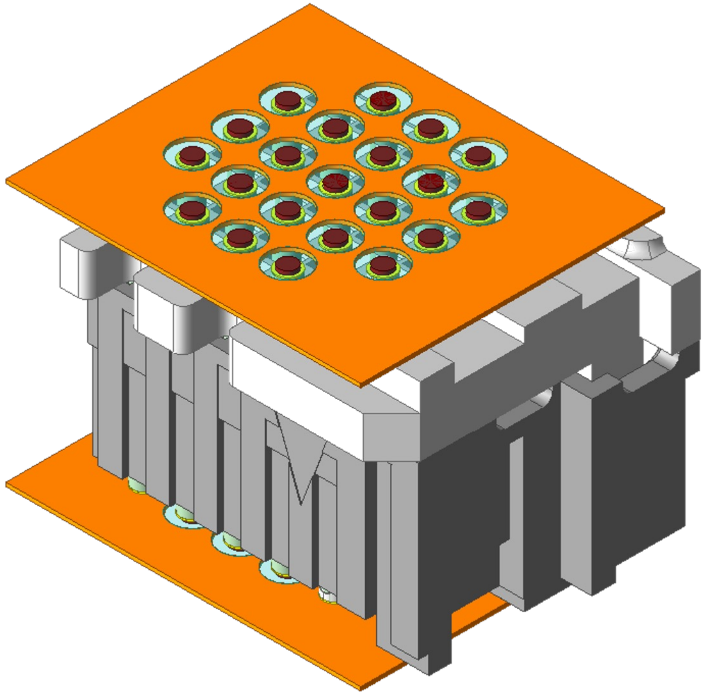

- With some pins assigned as dedicated returns, it is possible to simulate all the remaining pins of the open pin field connector.

- GND pin assignments can then be made by taking the resulting S-parameters and connecting the relevant pins to Spice GND.

- Addressed next: How accurate is this?

Accuracy Check

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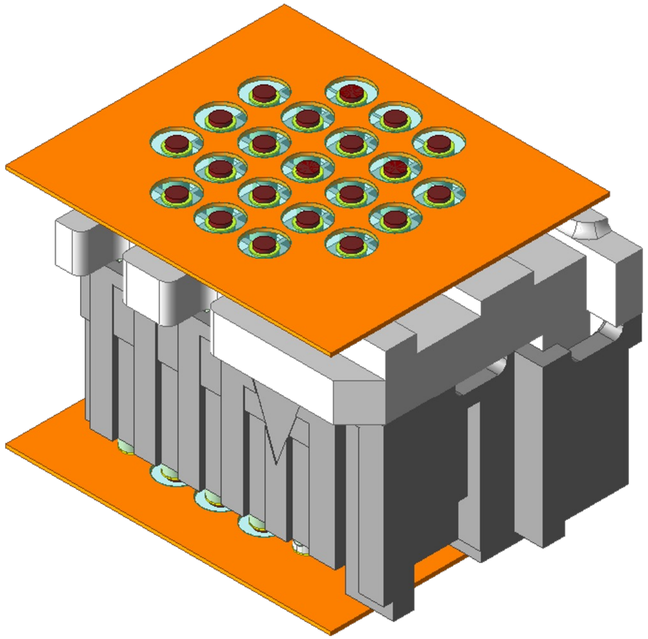
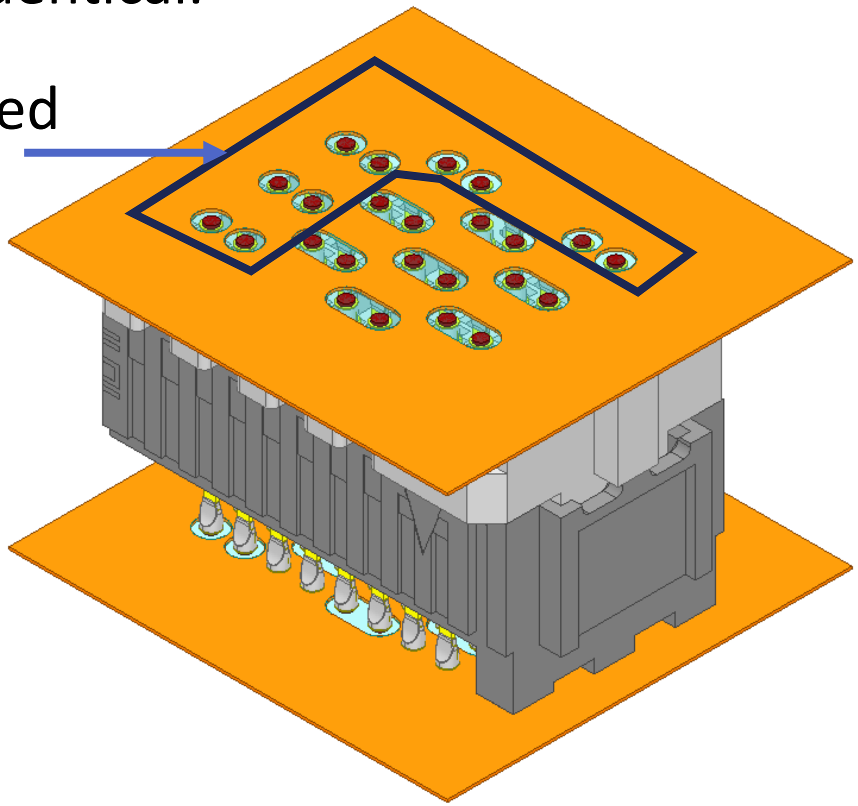
10 mm SEARAY™ simulated with 2 different types of port assignments. All other simulation conditions are identical.



Simulation A: All signal model

Pins terminated to 50 Ohms



Simulation B: Diff signal port assigned model

TDR & Return loss

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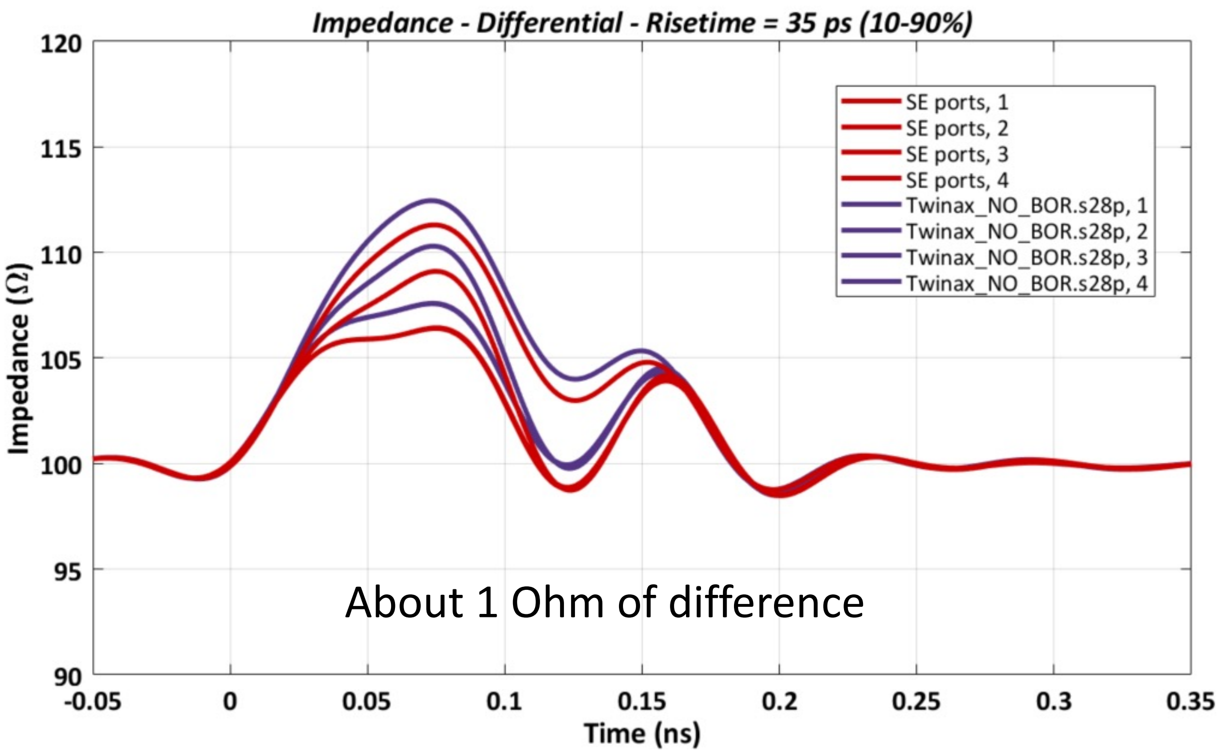

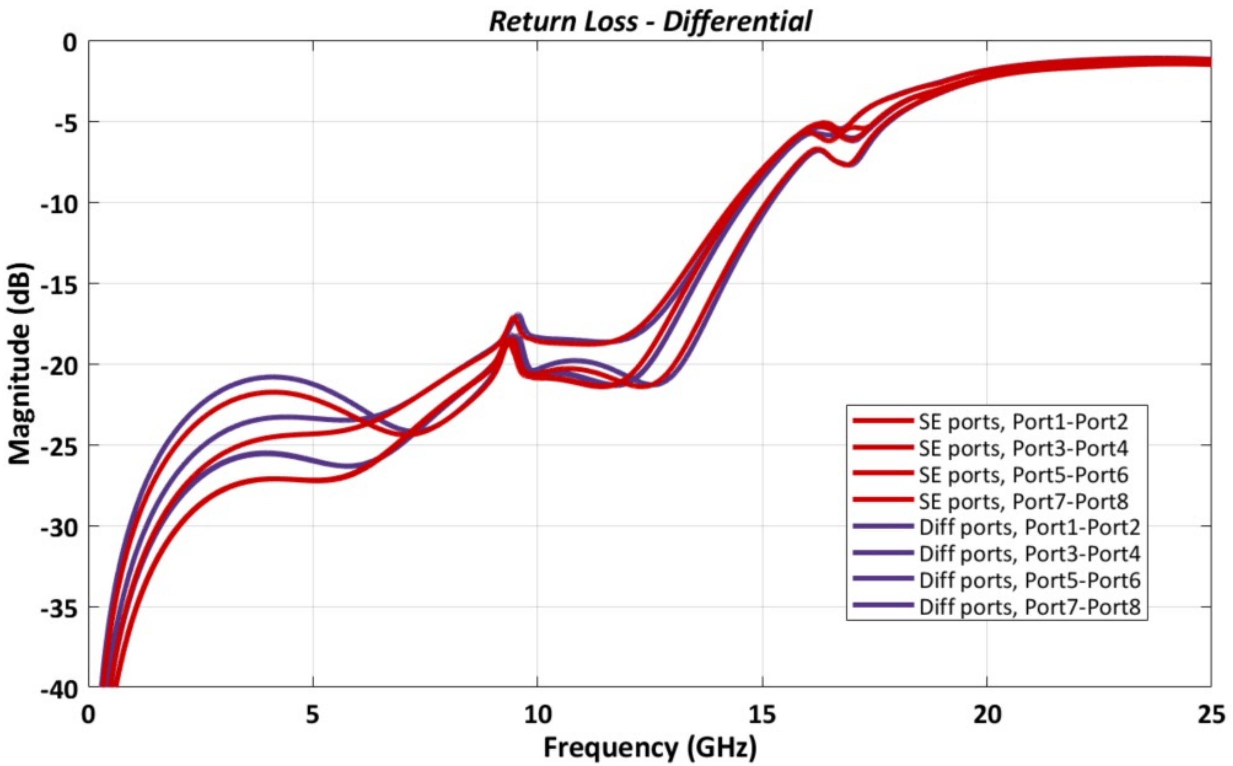

Insertion Loss

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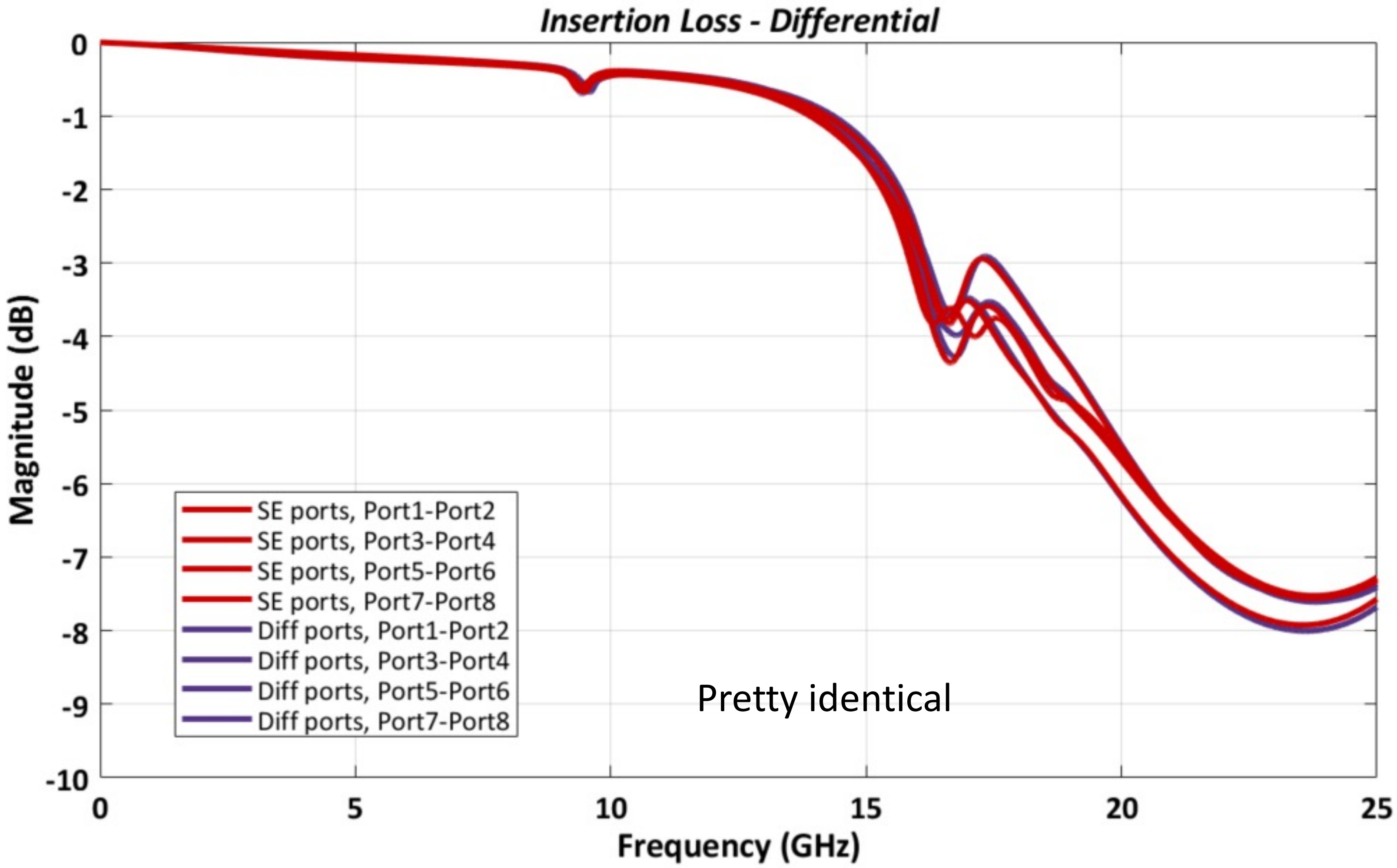

Pretty identical

NEXT & FEXT

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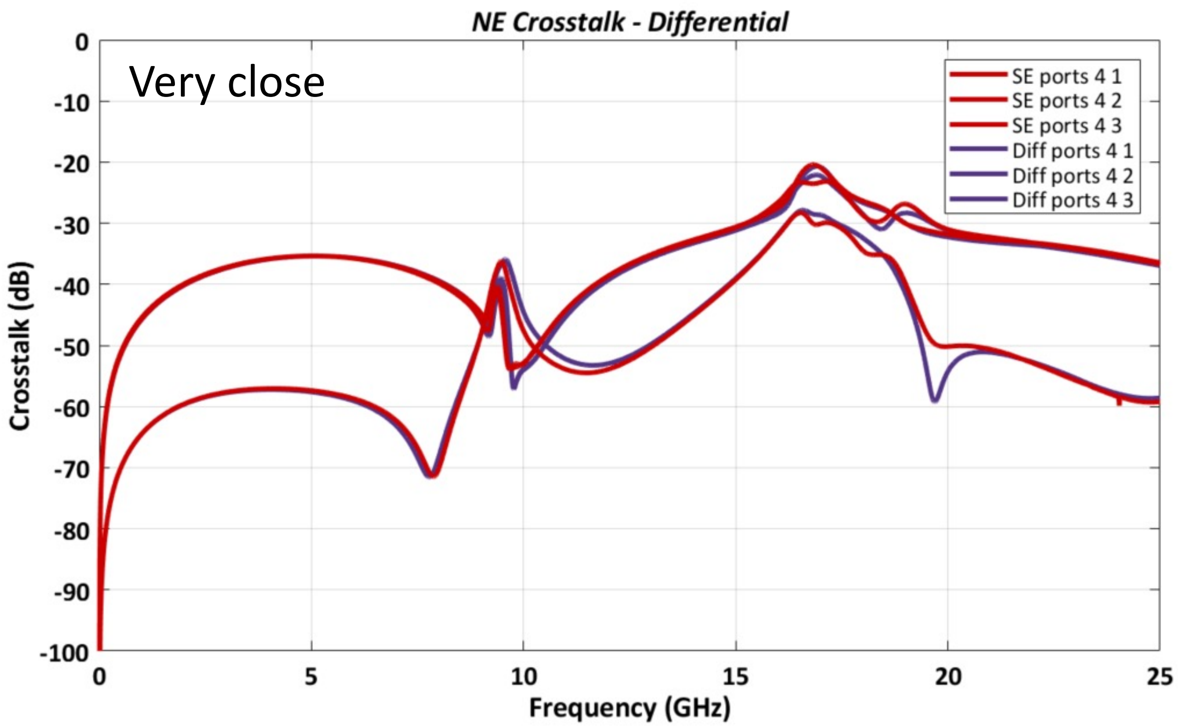

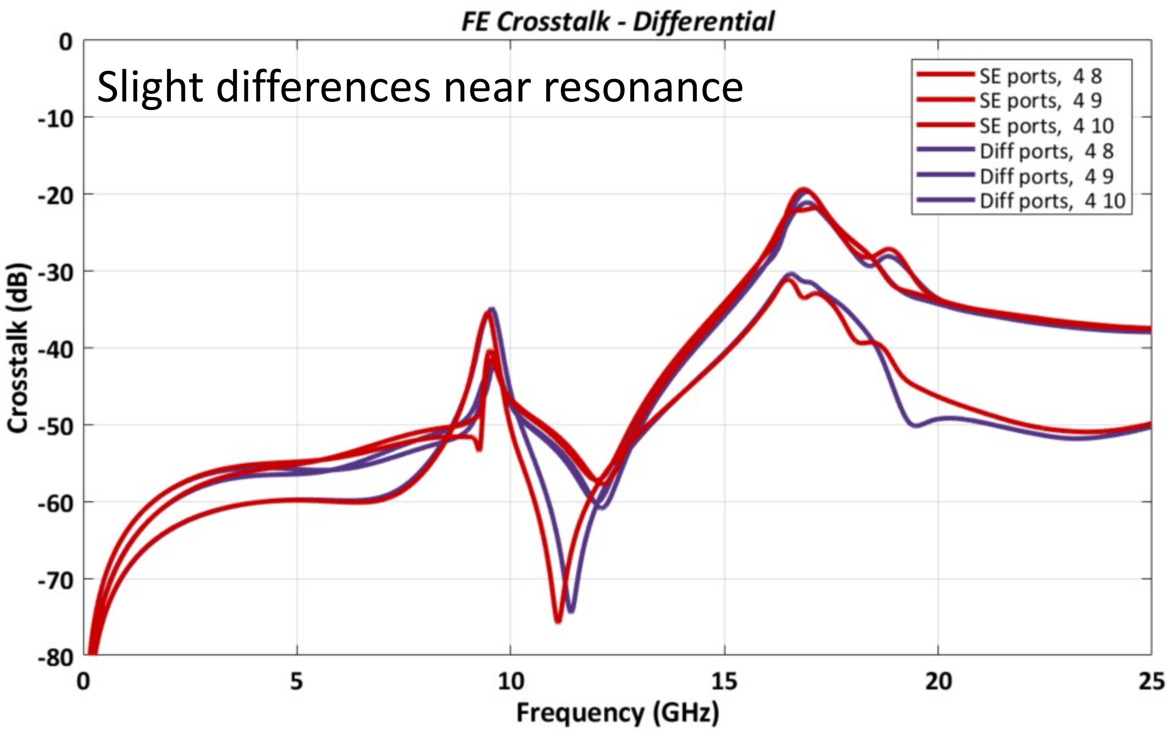

Accuracy Check - Takeaways

What was compared:

- Model with correct differential excitation to a model with SE excitations that was post processed to have differential excitation.

Goal:

- Have a model that is good to ~20 GHz BW, not fundamental signal frequency.

Results:

- IL looks nearly identical.
- RL is very close. About 1 Ohm difference seen in TDR with 35ps rise time.
- NEXT and FEXT magnitudes are very close except near connector resonances.

Overall, the “All Signal” methodology shows promise for the goals it is targeted for.

Conclusions

Up to 20 GHz bandwidth (not fundamental), an “All Signal” model can be very useful for analysis

More work being looked at on individual connector basis to make sure the methodology continues to hold true.

At a higher level, this methodology provides a way to filter down the list of things to focus on at an early design stage, when there are a number of possibilities on the table.

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