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Samtec SI Experts at DesignCon 2024

"The SI Team" | Samtec, Inc.

Thursday, January 18, 2024

Samtec SI Experts at DesignCon 2024

- Scott McMorrow
- Gustavo Blando
- Istvan Novak
- Richard Mellitz
- Brandon Gore
- Andrew Josephson
- Robert Branson
- Greylan Smoak
- Sandeep Sankararaman
- Shawn Tucker
- Adam Gregory
- Steve Krooswyk
- Anthony Fellbaum

How to Develop Advanced PCB Component Launches

Scott McMorrow | Samtec, Inc.
Matt Commens | Ansys, Inc.

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SPEAKERS

Scott McMorrow

Strategic Technologist, Samtec

Scott McMorrow serves as a Strategic Technologist for Samtec, Inc. As a consultant for years too numerous to mention, Scott has helped many companies develop high performance products, while training signal integrity engineers. Today he works for "the man," where he continues being a problem solver, a change agent and "betting his job" every day.

Matt Commens

Senior Manager, Product Management, Ansys

Responsible for the strategic product direction of the Ansys electronics software portfolio; including products HFSS, Maxwell, SIwave, and Icepak, and is a recognized expert in the application of computational electromagnetics.

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PART 1 - Periodically Loaded Transmission Lines (a.k.a. Via Launches)

Whereby we discuss the Systematic Process of Optimizing launches with vias in six "Simple" steps

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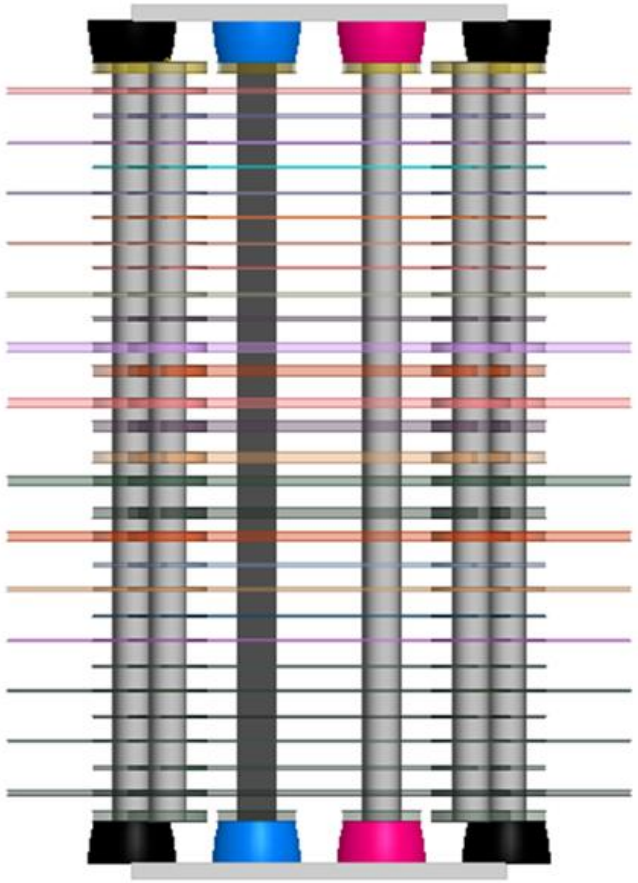
Zones of Control



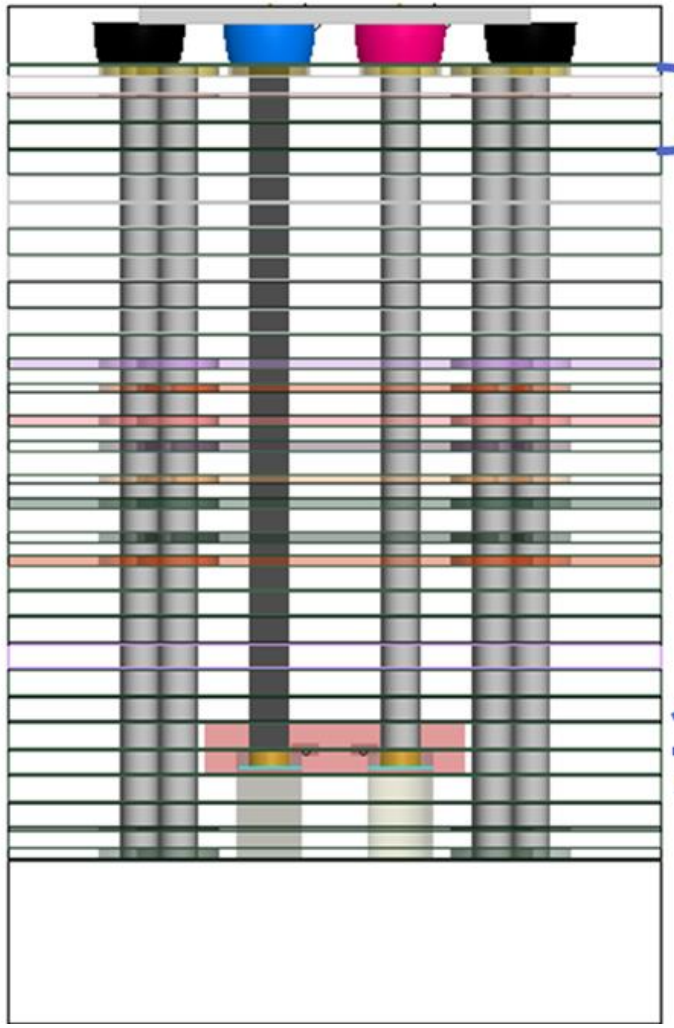
PlanesBelowTop

ThinTraceLayers

ThickPowerPlaneLayers

ThinTraceLayers

BackdrillLayers



Electromagnetic Shadow

PlaneAboveTrace

Trace

PlaneBelowTrace

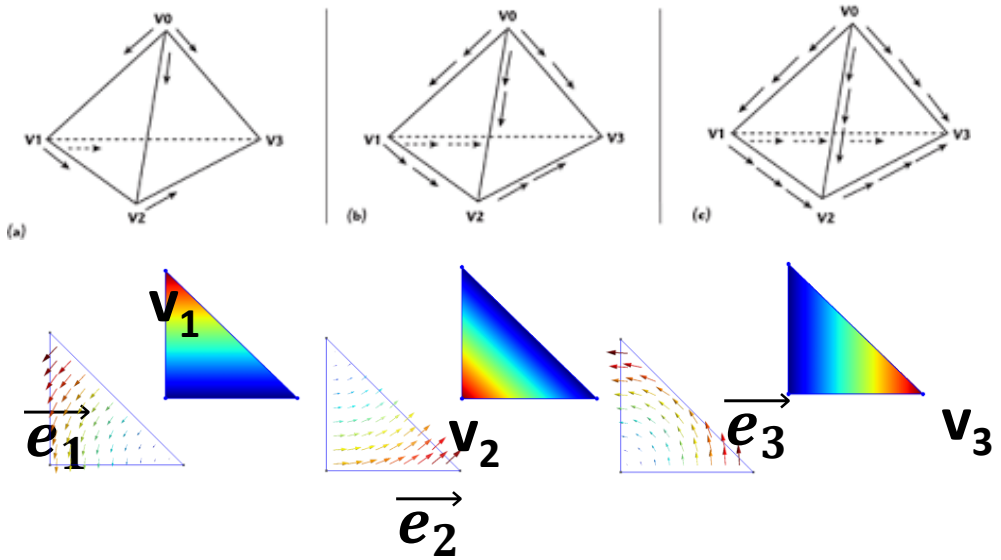
INTERREGNUM - The Finite Element Method in Electromagnetics

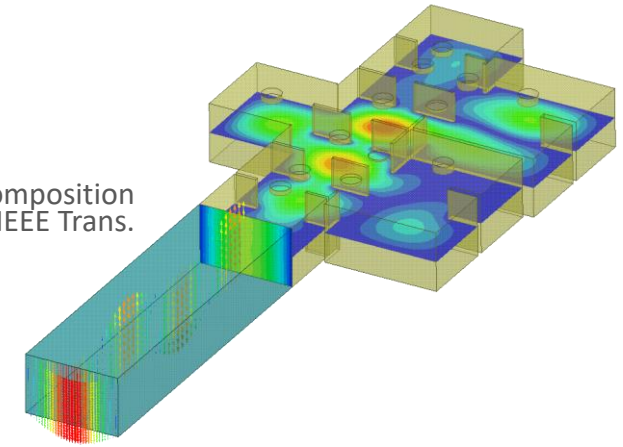
Background on the FEM Simulation Technique

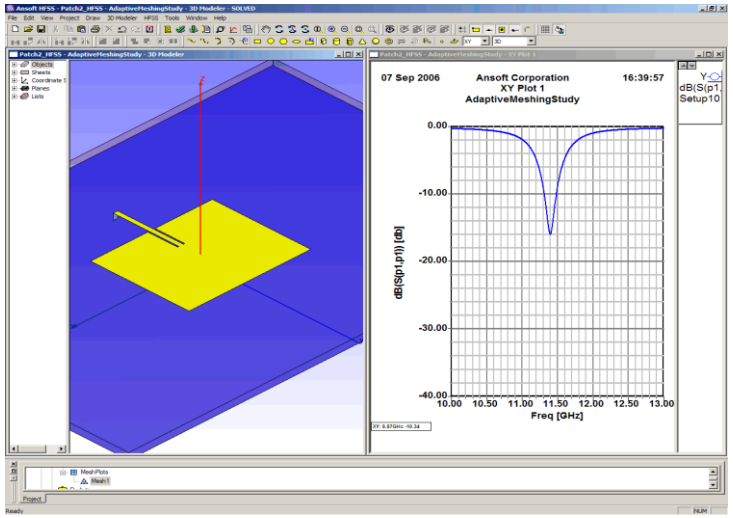
Discuss the Finite Element Method and the Key underlying technologies developed to enable it for 3D Full-Wave Electromagnetic Simulation and Network (S,Y,Z) Parameter Extractions

Key Technologies for Electromagnetic FEM

- Spurious Free Vector Basis Functions:
  - Reliable FEM solutions of Maxwell's Equations
    - M. L. Barton, Z. J. Cendes, "New vector finite elements for three-dimensional magnetic field computation", J. Appl. Phys., vol. 61, no. 8, pp. 3919-3921, 1987
- Automatic Adaptive Meshing:
  - Accurate, efficient, and reliable results
    - Z. J. Cendes and D.N. Shenton, "Adaptive mesh refinement in the finite element computation of magnetic field", IEEE Trans. Magn., vol. MAG-21, pp. 1811-1816, Sept. 1985
- Transfinite Element Method:
  - Accurate and efficient extraction of S,Y,Z parameter
    - Z. J. Cendes and J. F. Lee, "The transfinite element method for modelling MMIC devices", IEEE Trans. on Microwave Theory and Techniques, vol. 36, no. 12, pp. 1639-1649, December 1988
- Domain Decomposition Method:
  - Distributed memory computing and key for many advanced solver features
    - M. N. Vouvakis, Z. J. Cendes, and Jin-Fa Lee, "A FEM domain decomposition method for photonic and electromagnetic band gap structures", IEEE Trans. Antennas Propag., vol. 54, no. 2, pp. 721-733, February 2006







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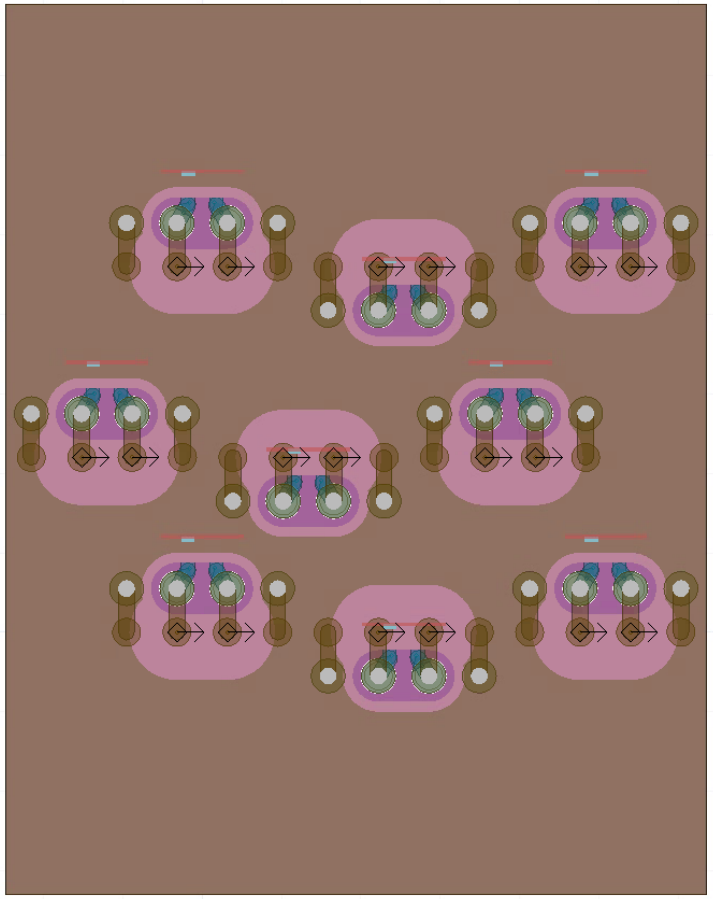
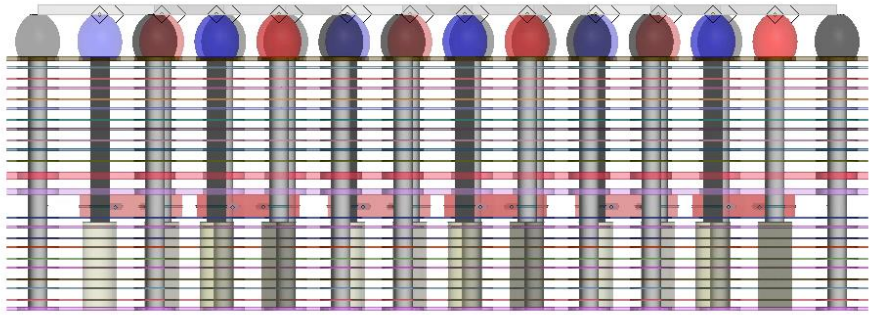
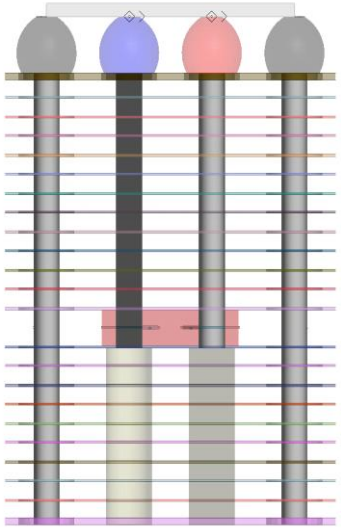
PART 2 – The Tool

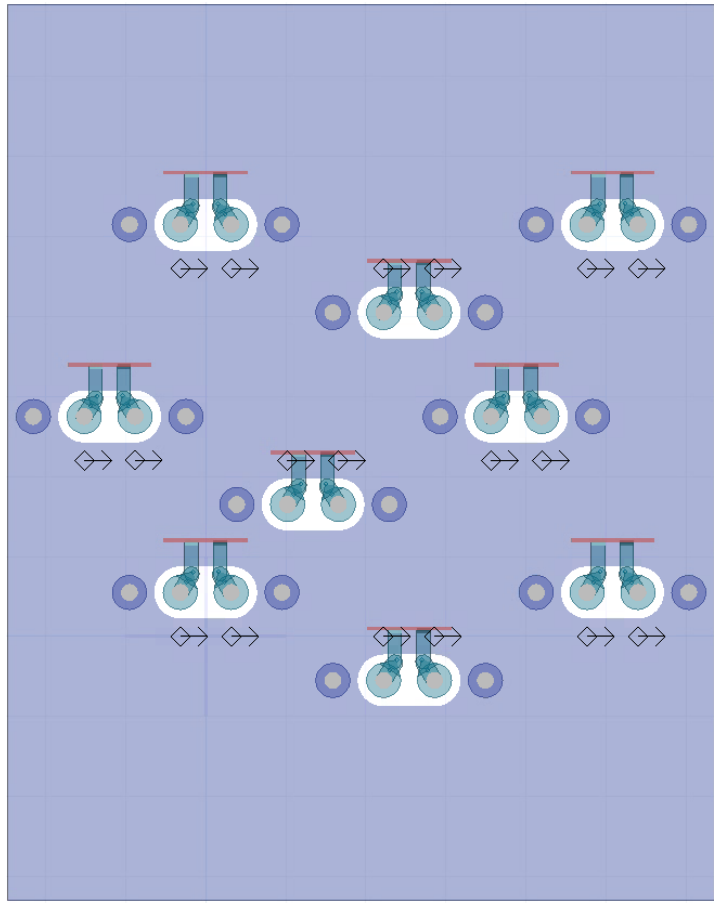
Whereby we show a tool which can be used to Generate, Visualize, Optimize, and Develop PCB Package and Component launches

The Tools









Considerations for Achieving 200 Gb/s Signaling per Electrical Lane Over 1 m of Twinaxial Copper Cable

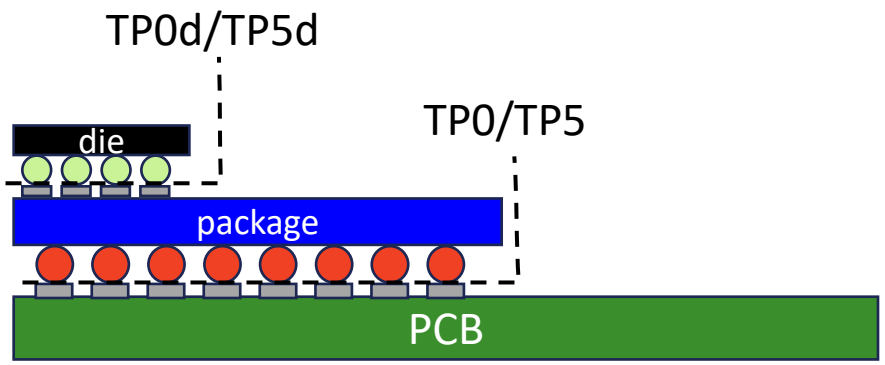
Speakers: Christopher DiMinico; MC Communications/PHY-SI/SenTekse; Mike Klempa, Alphawave Semi; Rick Rabinovich, Keysight

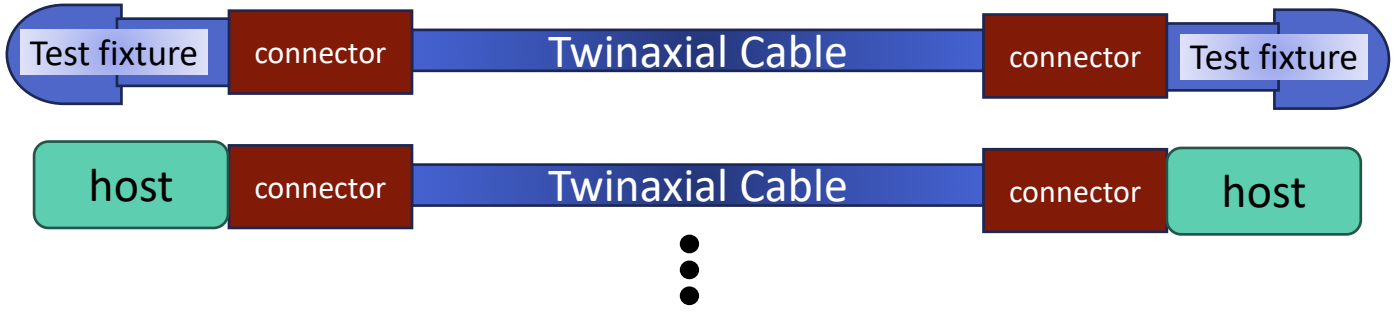
Authors: Christopher DiMinico, MC Communications/PHY-SI/SenTekse Mike Resso, Keysight; Curtis Donahue, Rohde & Schwarz; Mike Klempa, Alphawave Semi; Mike Rowland, Amphenol ICC; O.J. Danzy, Keysight; Richard Mellitz, Samtec; Adee Ran, Cisco Systems; Rick Rabinovich, Keysight

200 Gb/s PAM4 1 Meter DAC Overview

A Direct Attach Cable (DAC) assembly is a connectorized twinaxial copper cable

- Continuation DesignCon 2022 paper
  - "Validation for achieving 200 Gb/s signaling per electrical lane over 1 meter of passive twinaxial copper cable"
- Evolving 200 G landscape
  - IEEE802.3dj and OIF 224G
  - 224 G publications and demos
- What's changed
  - Loss objective moved to die to die... 40 dB at 53.125 GHz
  - New test points tp0d and tp5d
- What's proposed and discussed
  - Test fixture loss budgets
  - 1 meter DAC system budgets
  - Host loss budgets
- COM still used to qualify a DAC





200 Gb/s PAM4 1 Meter DAC Directions

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Other Considerations

- Discission of frequency range of s-parameter measurements for COM
- Result of the Die-to-Die Loss requirement result in:
  - Flexible host architectures and cable assembly reach options
- Explore old ideas which need rethinking for Differential-to-Common Mode Conversion and Skew
- Challenges for building a Host Compliance board renews interest in De-embedding
- Re-exploration of SerDes requirement for Passive and Active Copper cables
  - Jitter, noise, filter, and equalization

Realistic Use Cases for Edge, Angled, and Vertical Launch Connectors up to 100 GHz

Sandeep Sankararaman | Samtec, Inc.
With Shawn Tucker, Istvan Novak
and Gus Blando

What are the Tradeoffs?

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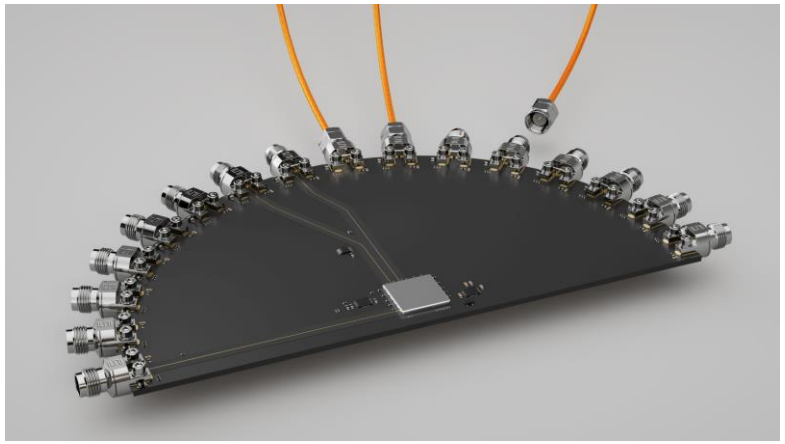
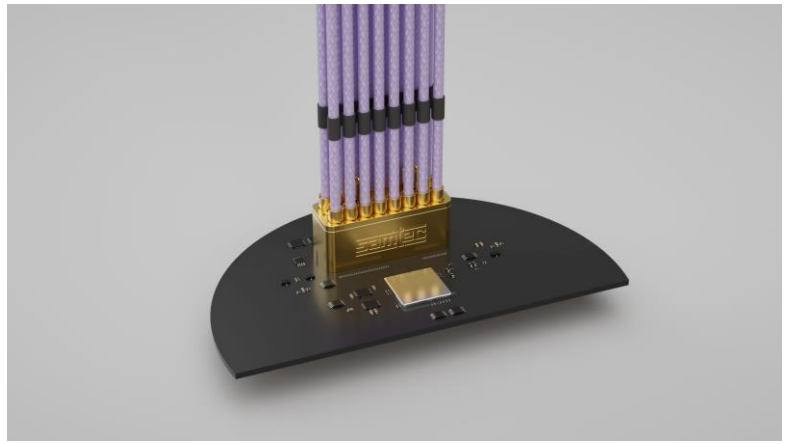


EDGE

VERTICAL / ANGLED



GANGED

Making the Right Tradeoffs

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	Edge	Angled	Vertical	Ganged
Distance to DUT				
Via transition to inner layer RL performance				
Calibration plane at the connector				
Crosstalk for ganged version				
Cost				

Will be convered during the talk

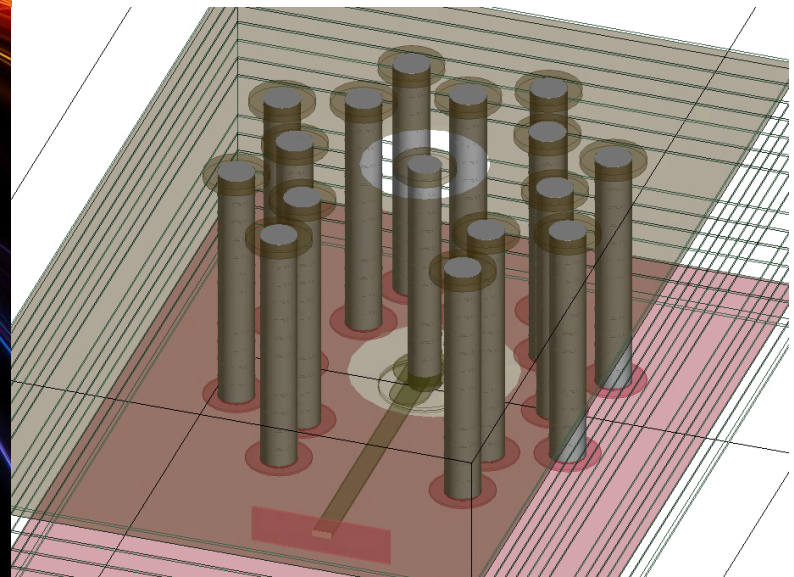
Color key

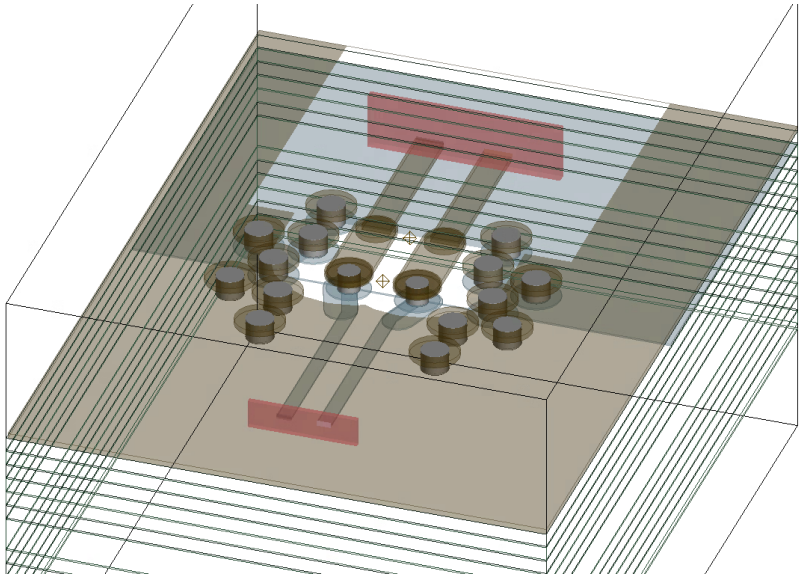
Survey on Correlation & Simulation Methodologies for PCB Structures Through 67 GHz

Robert Branson | Samtec, Inc.
Greylan Smoak | Samtec, Inc.

Introduction & Background

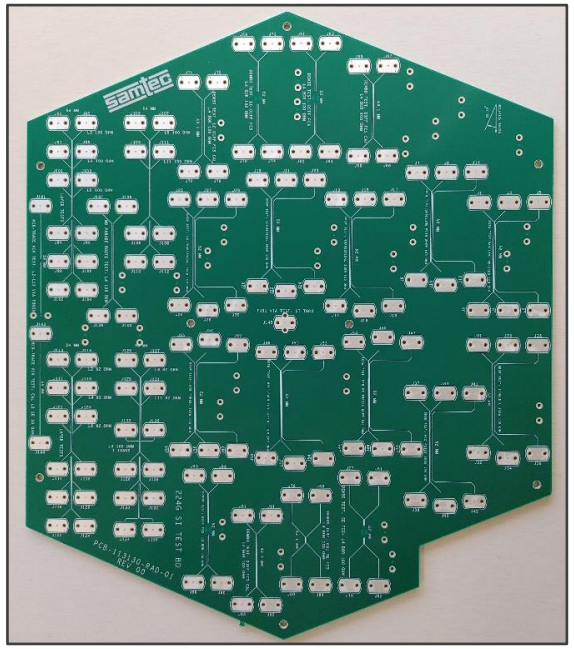
- It is difficult to build a nominal model that will correlate to final build
- Components of model correlation
  - Manufacturing Information, Manufacturing Variation, Simulation Methodology
- This paper focuses on simulation methodology characteristics:
  - Surface Roughness, Etching, Dielectric Modelling
- Paper then surveys modelling best-practices

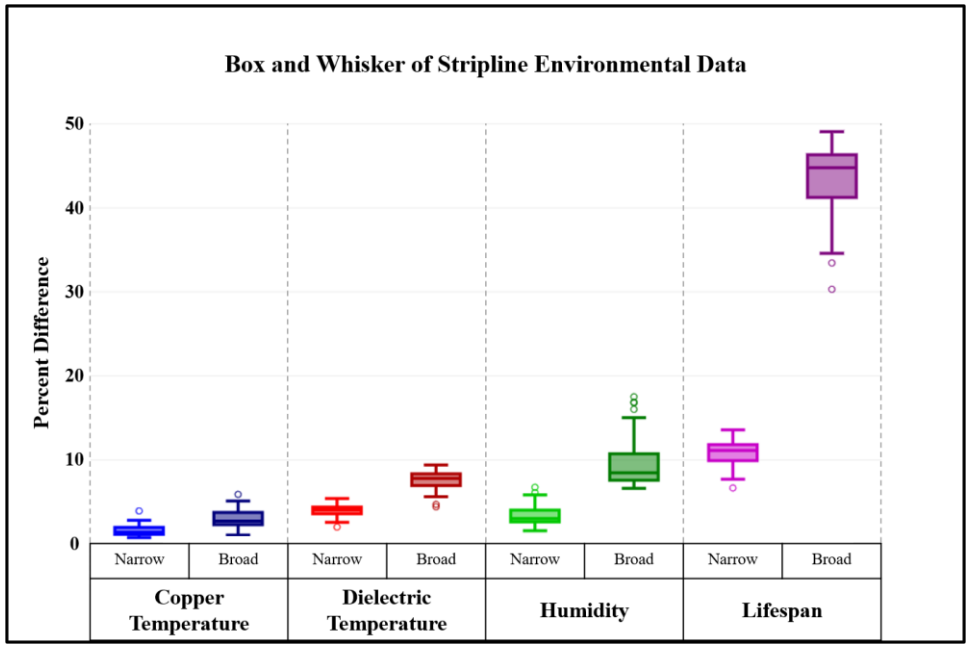




Covered Results

- Built a DOE to vary simulation methodology
  - Example of results shown in plot
- PCB characteristics compared
  - Ranking relative impact
- Custom-designed 224G-capable PCB manufactured to test conclusions
  - Measurements performed and compared to simulation data



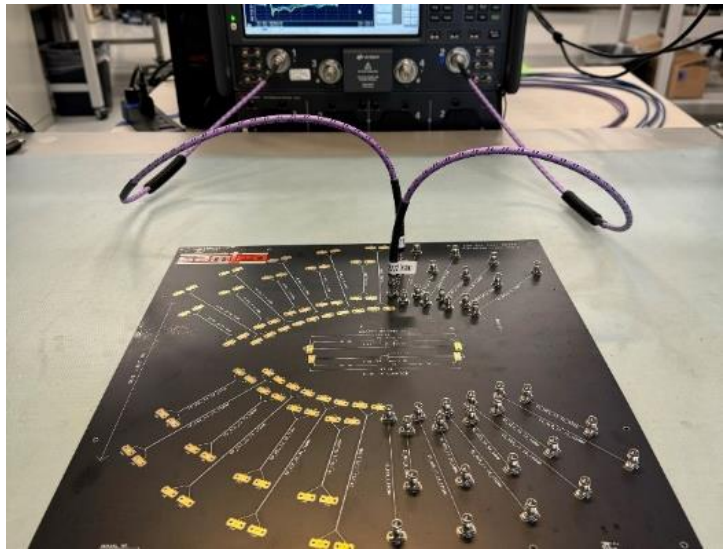


Are Precision RF 1.0 mm Connectors Really Required for 224 Gbps PAM4?

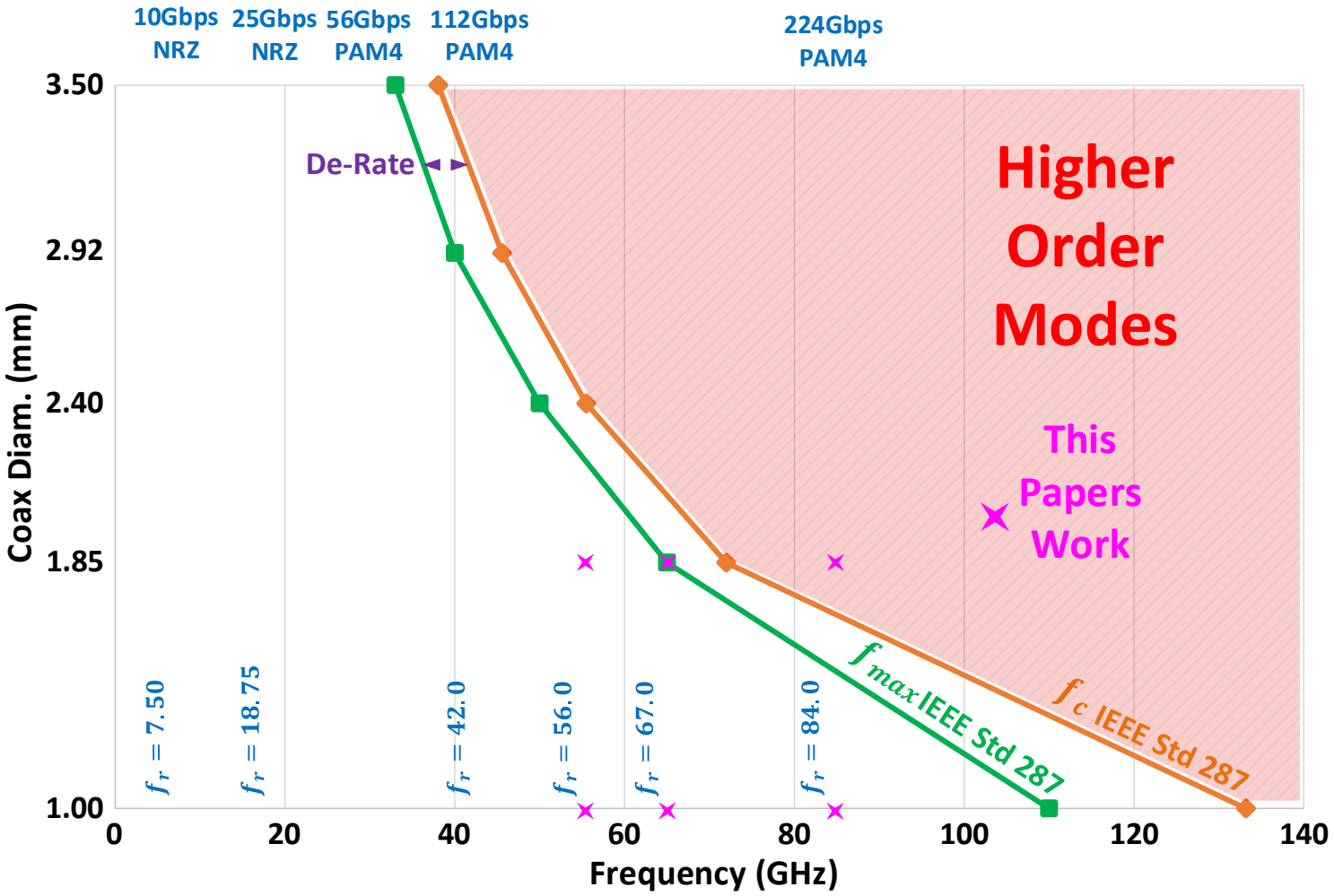
Brandon Gore | Samtec, Inc.

Topics Explored

- How IEEE handles required Rx Bandwidth:
  - 4th Butterworth filter cutoff (f_r)
  - Component verification vs noise verification
- Modal Theory and RF Cable Assembly considerations:
  - Higher Order Mode Cutoff (f_c) as Figure of Merit
  - 1.85 mm (V-band) vs 1.0 mm (W-band)
- Measurement Case Studies (1.85 mm vs 1.0 mm):
  - Stripline DUT with Vertical Mount RF Connectors (Top Right)
  - Ganged, cabled RF connectors Passing 224Gb/s PAM4 Signaling (Bottom Right)



Cutoff Frequency (f_c) Mapped to Usable Bandwidth

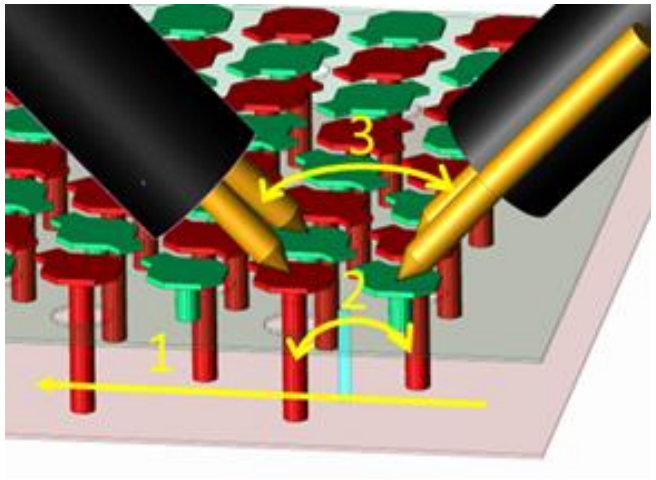


Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization

Gustavo Blando, Istvan Novak | Samtec, Inc.

Outline, Background

- Background and Impedance Definitions
- Probe models
- Devices Under Test
- IEEE Benchmark board
- Production Board
- Measurement and Simulation Setup
- Correlation
- Conclusions

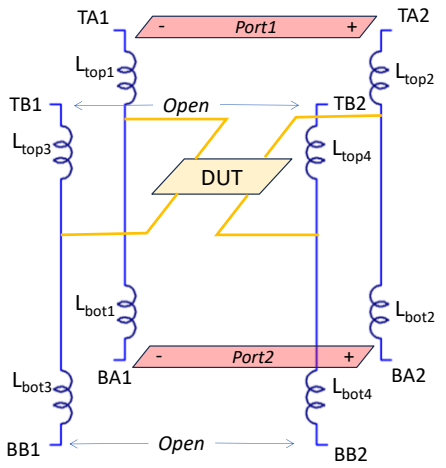


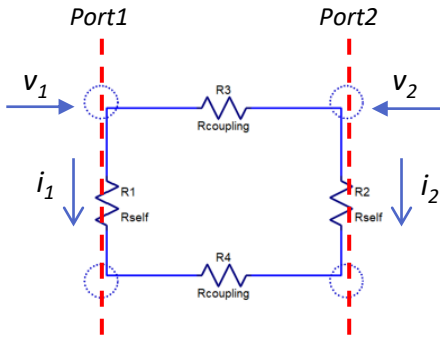
- The PDN impedance required in today's high-power electronic systems is no longer in the mΩ range, but it can be already around 100μΩ or less
- The design and measurement procedures developed in the last few decades must be re-visited and updated accordingly
- Three major aspects of PDN measurements and simulation are investigated
- The spatial effects associated with large via arrays in low-impedance PDNs (1 in figure)
- The impact of via coupling within the Device Under Test (2 in figure)
- The impact of probe-tip coupling in wafer probe calibrations and measurements (3 in figure)
- The purpose is to explore these relationships and provide insight to designers to correctly take the spatial and other 3D effects* into account to face the new level of performance needs

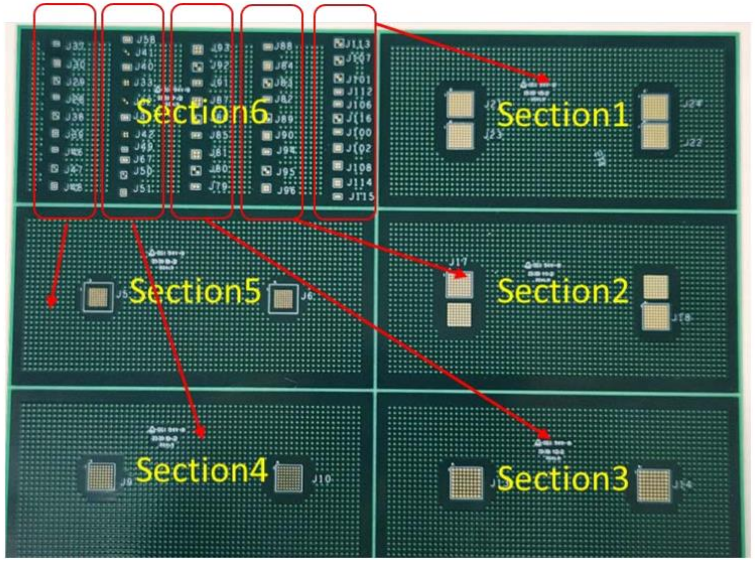
* Koether et al. "3D Connection Artifacts in PDN Measurements" DesignCon 2023

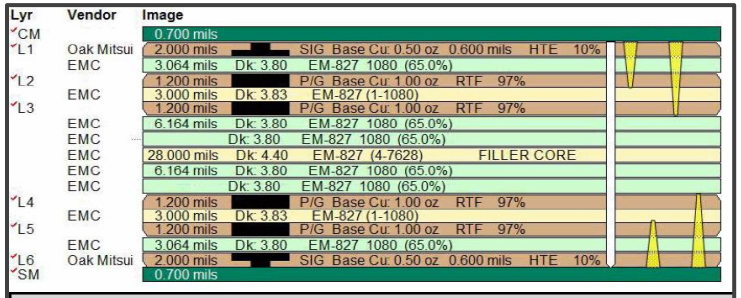
Impedance Definitions, Test Board

$$\begin{bmatrix} Z_{11n} & Z_{12n} \\ Z_{21n} & Z_{22n} \end{bmatrix} = \begin{bmatrix} \dfrac{2\Delta_1 S_{11} + S_{12}S_{21}}{4} & \dfrac{S_{12}}{2} \\ \dfrac{S_{21}}{2} & \dfrac{2\Delta_2 S_{22} + S_{12}S_{21}}{4} \end{bmatrix}$$



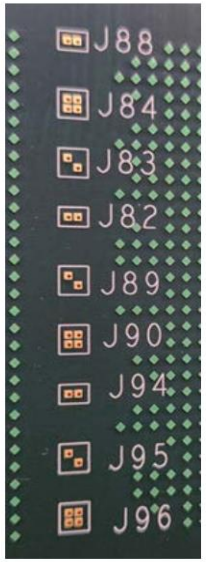






DRILL TABLE

Start Layer	End Layer	Drill Type	Plate Type	Via Fill	Stacked Via	Min Drill Size (mils)	Drill Depth (mils)
1	6	Mechanical	PTH	----	----	0.000	58.5
1	2	Laser	Micro Via	Copper Fill	No	6.000	3.7
6	5	Laser	Micro Via	Copper Fill	No	6.000	3.7
1	3	Laser	Micro Via	Copper Fill	No	10.000	7.9
6	4	Laser	Micro Via	Copper Fill	No	10.000	7.9



J88: both vias (straight) land on L3

J84: all four vias land on L2

J83: both vias (diagonal) land on L2

J82: both vias (straight) land on L2

J89: both vias (diagonal) land on L3

J90: all four vias land on L3

J94: straight pair landing on L2 and L3

J95: diagonal pair landing on L2 and L3

J96: checker-board quad landing on L2 and L3

- Reference structures containing through-hole via structures shorted to a single layer, mimicking VDD and VSS plane connections in a board's PDN
- Allows for measurement and simulation of short and long via loops without plane effects
- The shorted launch, J84, will be examined – it has both the shortest loop path on the board from the top side as well as the longest loop when measured from the bottom

Comparing the Different Metrics of Intra-Pair Skew in Tracking Channel Performance

Steve Krooswyk | Samtec, Inc.

Motivation:

- Ever-decreasing UI makes skew more important
- Skew from manufacturing is now on par with UI
  - PCB variation
  - PCB routing
  - Cable
  - Right angle connectors

Table: Different IO standards for data rate, baud rate and unit interval.

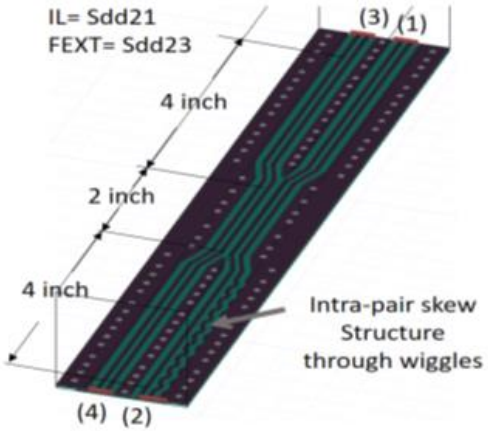
IO Standard	Signaling	Data rate [Gbps]	Baud rate [GBd]	Unit Interval [psec]
PCIe Gen 3	NRZ	8	8	125.00
10G Ethernet	NRZ	10.3125	10.3125	96.97
PCIe Gen 4	NRZ	16	16	62.50
25G Ethernet	NRZ	25.78125	25.78125	38.79
50G Ethernet	PAM4	53.125	26.5625	37.65
PCIe Gen 5	NRZ	32	32	31.25
PCIe Gen 6	PAM4	64	32	31.25
100G Ethernet	PAM4	106.25	53.125	18.82

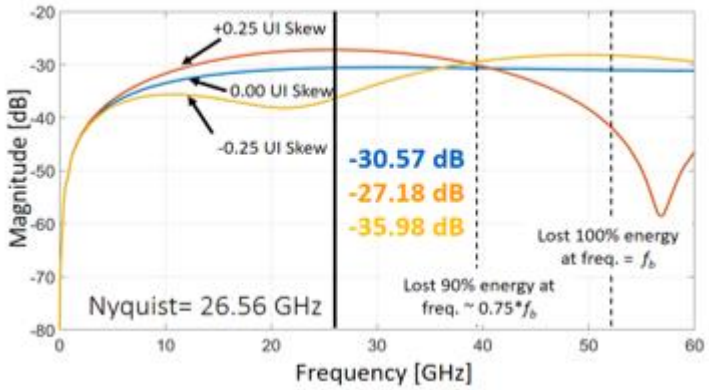
Digging Deeper into Skew

Three focal questions points to a wide problem

1. What effect does crosstalk experience due to skew?
2. How should we measure skew?
3. Should skew be standardized?

Simulations and measurements are included





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PCI Express & PAM4:
The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems

Steve Krooswyk | Samtec, Inc.

Panel Focus:

- Equalization schemes
- Channel simulation
- Modeling & correlation
- CEM, U.2, and M.2 form factor and layout updates
- Requirements for 128 GT\s TX compliance
- RX requirements and testing at 128 GT\s
- Copper cable specification
- Optical cable update

PANELISTS:

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Pegah Alavi

Sr. Solutions Engineer, Keysight Technologies

Pegah is a Senior Applications Engineer at Keysight Technologies, where she focuses on Signal Integrity and High-Speed Digital Systems and Applications. Prior to joining Keysight Technologies, Pegah worked on system level modeling of analog and mixed signal circuits in order to best predict the overall systems performance and accurately represent each component.

Tim Wig

Signal Integrity Engineer, Intel Corporation

Tim joined Intel in 2001, where he works as a Signal Integrity Engineer in a pathfinding and spec development group whose charter includes PCIe and other interconnect standards. Tim coordinates the Card ElectroMechanical (CEM) Spec document for Gen 4.0 and 5.0, and has contributed many of the Signal Integrity enablers that allowed PCIe to reach 16 and 32 GT/s. His primary focus is passive component, PCB, and channel level modeling, measurement, and optimization for PCIe CEM, though he also supports the M.2, U.2, and OCuLink standards. He holds a PhD in Engineering Science from Washington State University; and a MS and BS in Electrical Engineering and a BS in Engineering Physics from the University of North Dakota. He delivered a tutorial on PCIe Gen 4.0 to DevCon 2016.

Steve Krooswyk

Sr. Signal Integrity Engineer, Samtec, Inc.

Steve is involved in new High-Speed Connector Development and PCIe Standards at Samtec. His 20 years of Signal Integrity experience has had a focus on the design, simulation, and correlation of PCIe interconnect and I/O. Previously, Steve was the PCIe tech lead for SI in Intel's data center division during Gen3 and Gen4 development. He is an author of the book High-Speed Digital Design: Design of High-Speed Interconnects and Signaling and holds a MS degree from the University of South Carolina.

PANELISTS:

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David Bouse

PCIe Principal Technology Lead, Tektronix

David is the PCI Express Principal Technology Lead at Tektronix and has been heavily involved in PCIe Physical layer pathfinding and specification development within the PCI-SIG. His areas of focus include transmitter and receiver test methodology, test fixture design, and waveform post-processing algorithms for NRZ & PAM4. David is an active participant in the Electrical Work Group and Serial Enabling Group where he helps accelerate the pace of technology development and adoption across multiple market segments.

Madhumita Sanyal

Sr. Staff Technical Marketing Manger, Synopsys Inc.

Madhumita is a Senior Staff Technical Marketing Manager for Synopsys' High-Speed SerDes PHY IP portfolio. She has 16+ years of experience in design and application of ASIC WLAN products, logic libraries, embedded memories, and mixed-signal IP. Madhumita holds a Master of Science degree in Electrical Engineering from San Jose State University and LEAD from Stanford Graduate School of Business.

PANELISTS:

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Rick Eads

Principal PCIe Program Manager, Keysight

Rick is a principal Program Manager at Keysight Technologies with expertise in technical/industrial marketing of test & measurement tools and electronic design automation software in the computer, semi-conductor, communications, and storage industries globally. His specialty is precision product and solution definition. He provides technical leadership in driving standards within industry organizations for PCI Express, CCIX, GenZ, OCP, NVM Express, CEI 4.0, IEEE 802.3, ExpressCard, DDR, SATA, and InfiniBand. He markets test and measurement products covering oscilloscopes and associated compliance software tools, vector network analyzers, bit error ratio testers (BERTs) and EDA tools. Rick earned an MBA from the University of Colorado and holds a BSEE from Brigham Young University with an emphasis on digital design and computer architecture. Rick contributes to the development of the PCIe physical layer BASE, CEM, and Test Specs, leading electrical Gold Suite testing at PCI-SIG workshops globally since 2004.

Sam Kocsis

Director of Standards and Technology, Amphenol

Sam currently holds the role of Director of Standards and Technology at Amphenol, focusing on the proliferation of innovative interconnect solutions. Sam coordinates Amphenol's engagement strategies in various industry standards and consortiums across networking, server/storage, optics, and commercial markets. He is active in IEEE 802.3, OIF, and OCP projects, and is currently a co-chair of the OSFP MSA and chairman of the PCI-SIG Cabling Workgroup. Sam holds BSEE and MSEE degrees from the University of Rochester, in Rochester, New York.

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Samtec Experts at DesignCon 2024

Samtec Experts at DesignCon - Tuesday

- **Tutorial:** How to Develop Advanced PCB Component Launches
  - Scott McMorrow and Matt Commens, ANSYS, Inc.
  - Tuesday, 30 January, 9AM, Ballroom B

- **Panel:** Extreme Confidence Simulation for 400-800G Signal Integrity Design
  - Scott McMorrow
  - Tuesday, 30 January, 4:45-6PM, Ballroom B.

- DesignCon Welcome (To The Jungle) Reception
  - Tuesday, January 30, 6:00 – 8:00PM
  - Santa Clara Ballroom, Hyatt Regency Santa Clara

Samtec Experts at DesignCon - Wednesday

- **Paper:** Comparing the Different Metrics of Intra-Pair Skew in Tracking Channel Performance
  - Richard Mellitz, Adam Gregory, Steve Krooswyk et al.
  - Wednesday, 31 January, 11:15AM, Ballroom E.
- **Paper:** Realistic Use Cases for Edge, Angled, and Vertical Launch Connectors up to 100 GHz
  - Sandeep Sankararaman, Gustavo Blando, Istvan Novak, Shawn Tucker
  - Wednesday, 31 January, 12:15PM Ballroom F.
- **Paper:** 200 Gbps Signaling Per Electric Lane Over 1 Meter of Passive Twinaxial Copper Cable
  - Richard Mellitz et al.
  - Wednesday, 31 January, 12:15PM, Ballroom C.
- **Sponsored Session**: Simulation-to-Measurement Correlation of Multi-port devices with four-port VNAs
  - Anthony Fellbaum and Jason Ellison, Rohde & Schwarz
  - Wednesday, 31 January, 3:00PM, Great America Ballroom 2
- **Panel:** PCI Express: Pathway to 128 GT/s and Interoperability at 64 GT/s (PAM4)
  - Steve Krooswyk et al.,
  - Wednesday, 31 January, 4:00PM, Ballroom C.

Samtec Experts at DesignCon - Thursday

- **Paper:** Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization
  - Istvan Novak, Gustavo Blando, et al.
  - Thursday, 1 February, 9:00AM, Ballroom E
  - **[Best Paper Award Finalist!]**
- **Paper:** Are 1.0mm Precision RF Connectors Really Required for 224 Gbps PAM4 Verification?
  - Brandon Gore, Richard Mellitz, Andrew Josephson, et al.
  - Thursday, 1 February, 11:15AM, Ballroom F
  - **[Best Paper Award Finalist!]**
- **Paper:** Survey on Correlation and Simulation Methodologies for PCB Structures through 67 GHz,
  - Robert Branson, Greylan Smoak, Steve Krooswyk, Scott McMorrow
  - Thursday, 1 February, 2:00PM, Ballroom C.
- **Sponsored Session**: 112 Gbps PAM4 Interconnect Models Simplify Channel-Wide Modeling and Simulation
  - Anthony Fellbaum
  - Thursday, 31 January, 3:00PM, Great America Ballroom J

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