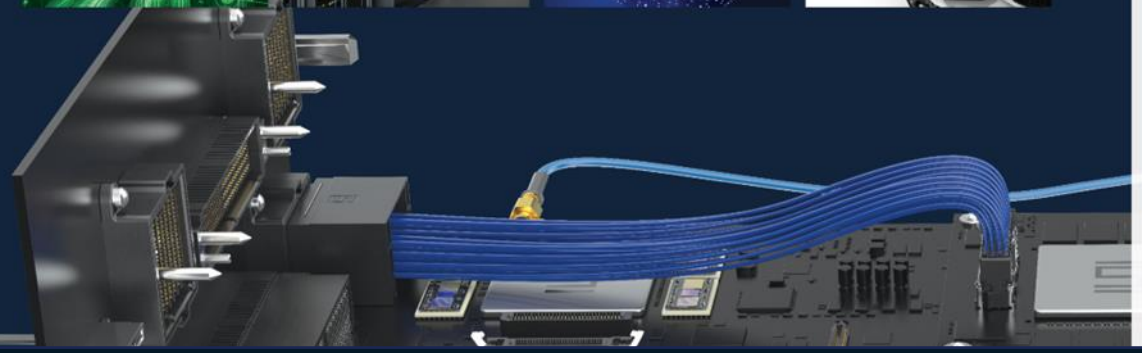
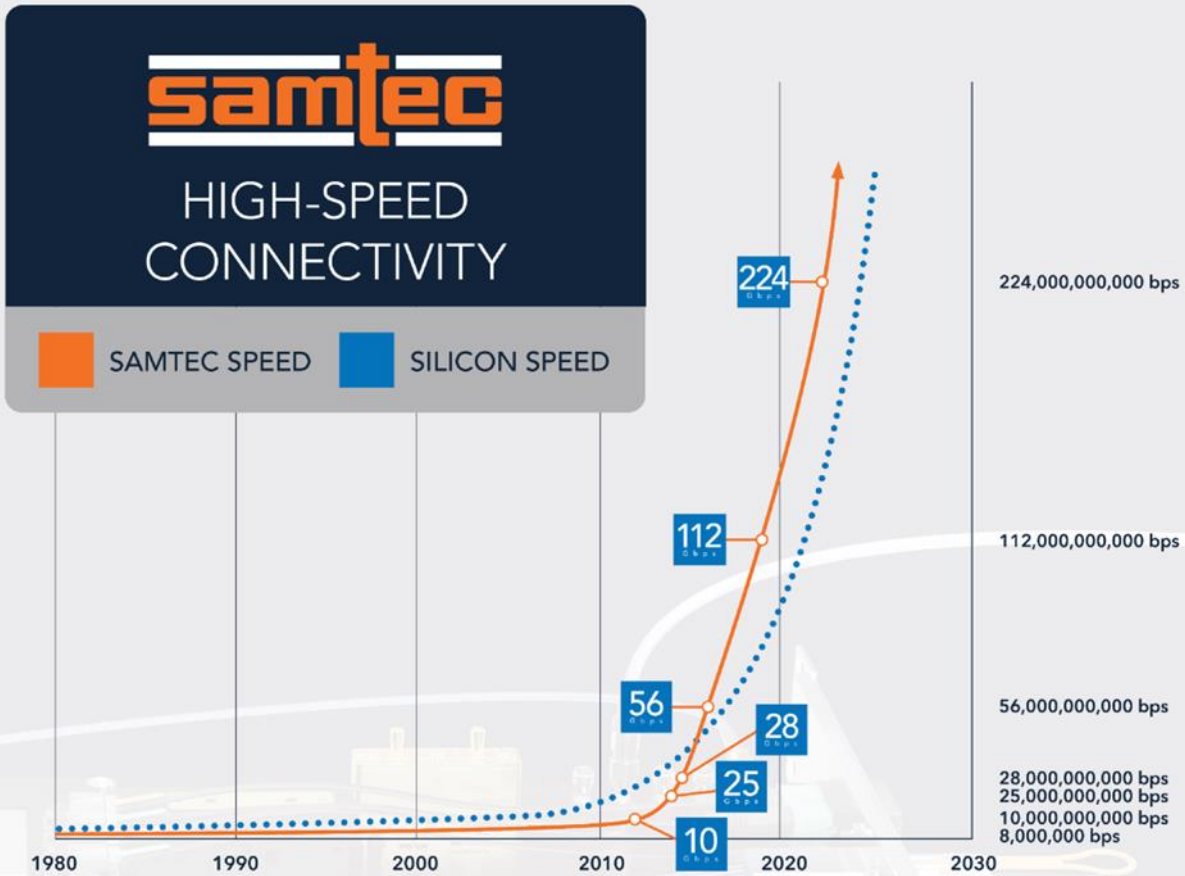
S-parameter in Keysight ADS

Ted Wang | Samtec, Inc.

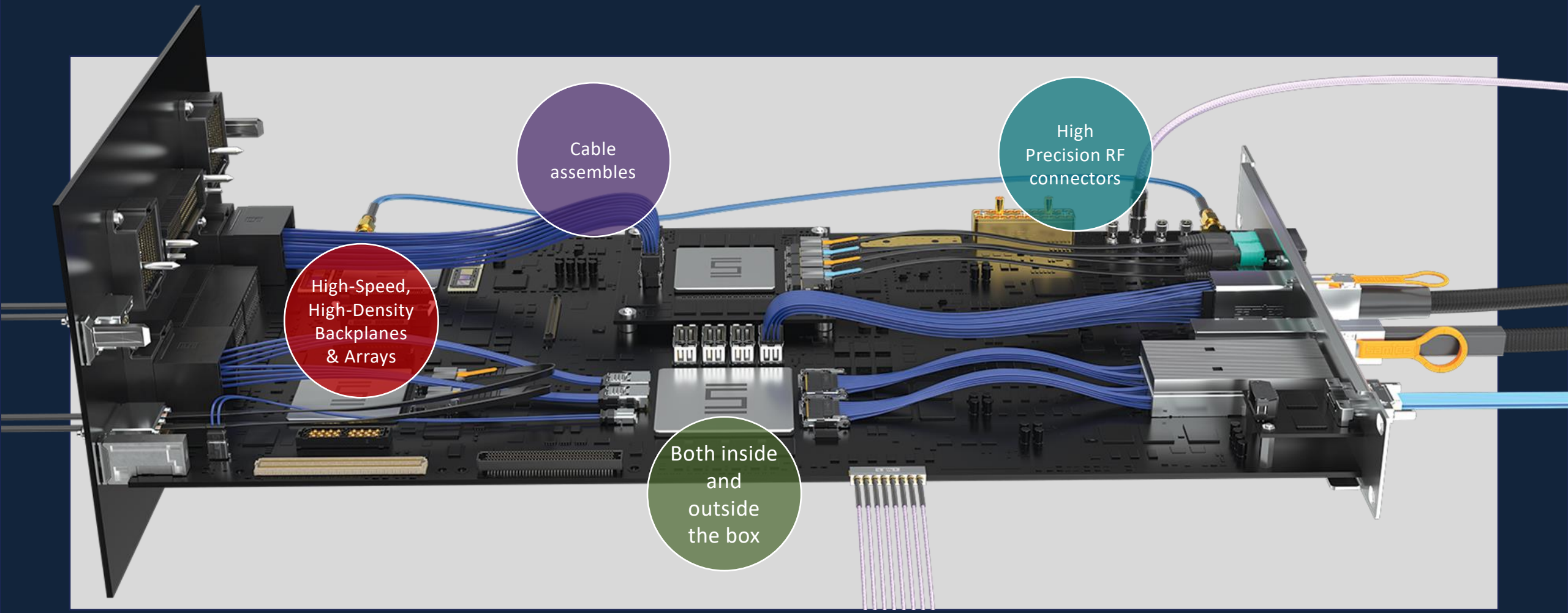
Design Challenge

- Varieties of Applications
- Rapidly increased Data Rate
- High System Cost
- Short Developing Time





Interconnect in System Designs



Solution!

Simulation - *S-parameter*

Quick

Most of the simulation could be completed In an hour

Accuracy

Correlated to measurements

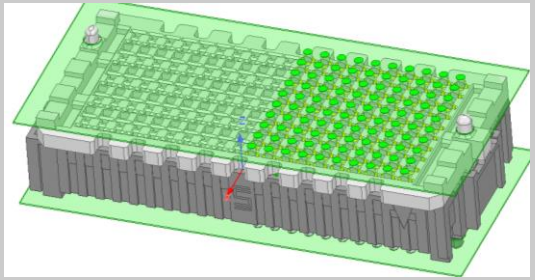
Cost

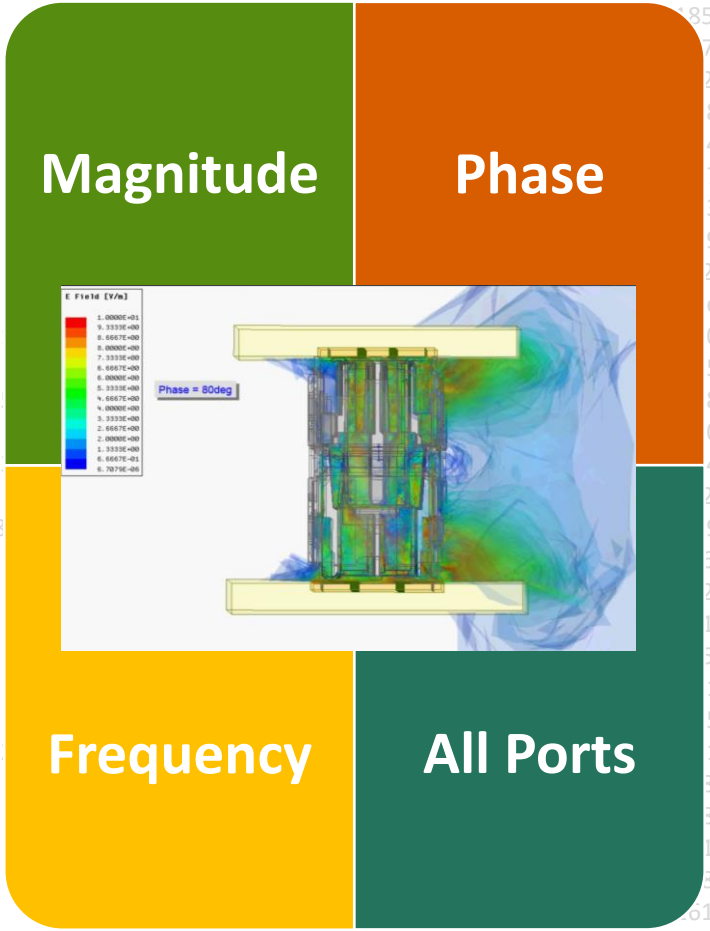
$ = 0, EDA tools are still relatively cheap

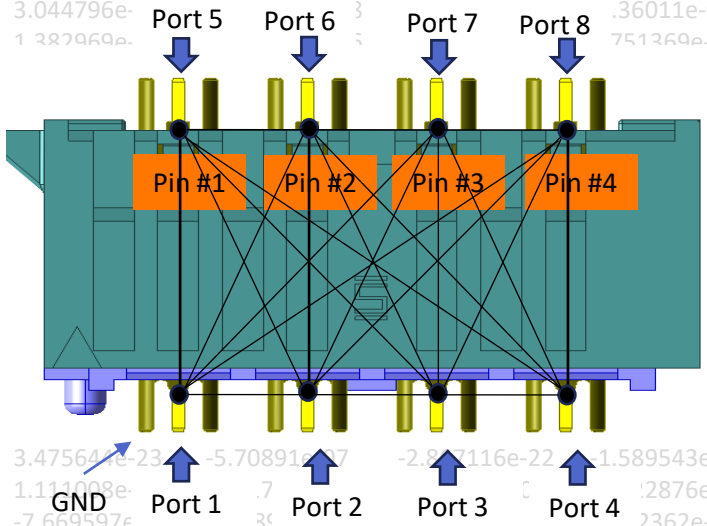
Flexibility

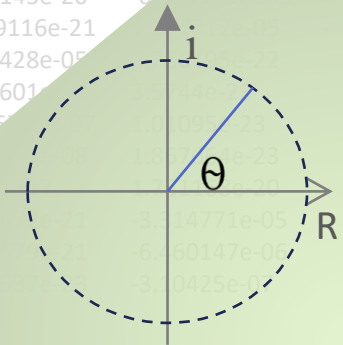
Model cascading, time /frequency domain

How Samtec Builds S-parameter Models









What You Should Care About S-parameter Models

samtec

Model Bandwidth

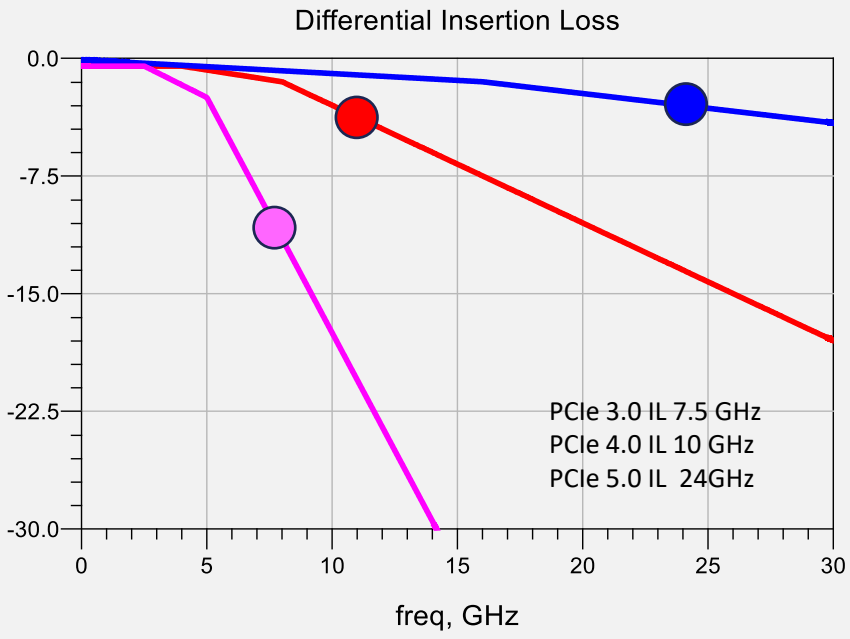
Signal Mapping

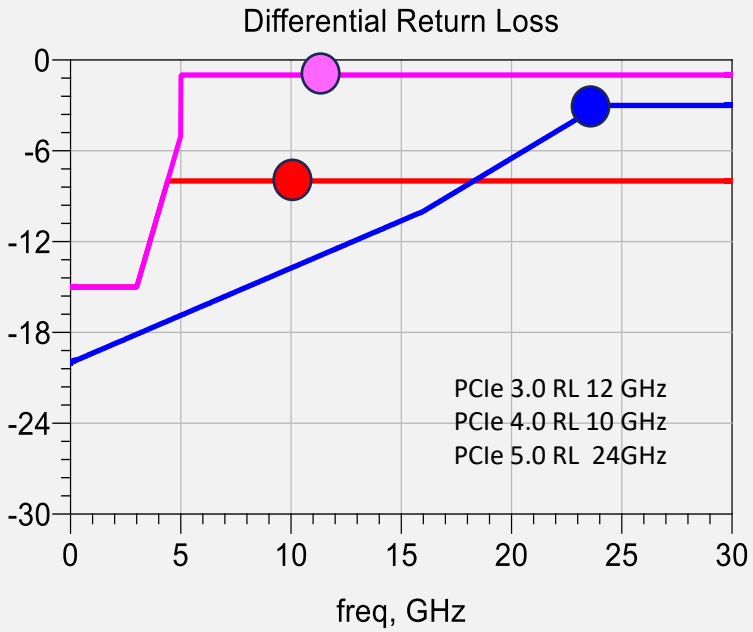
Port Count

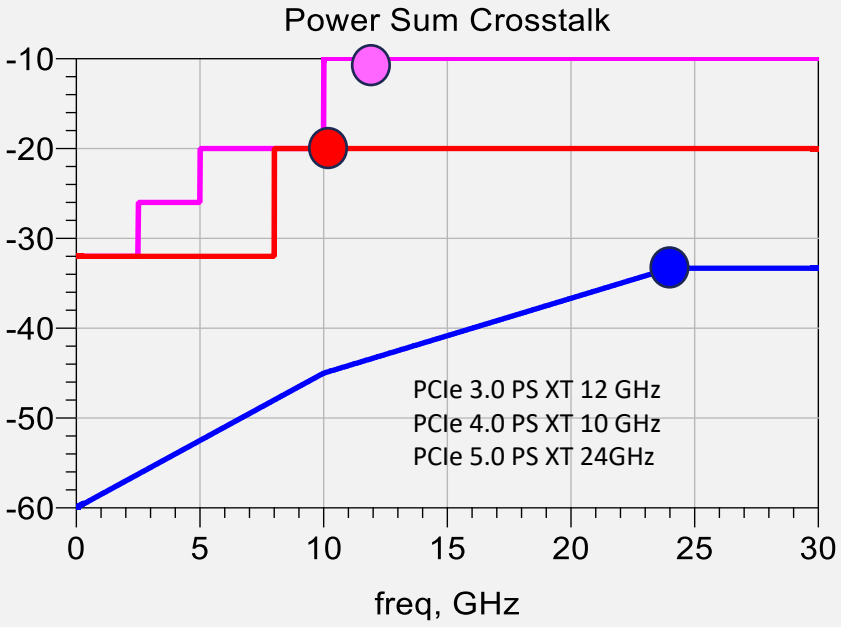
Model Boundary

Model Bandwidth

PCIe 3.0 PCIe 4.0 PCIe 5.0

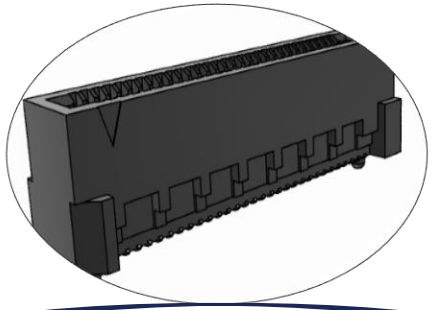






How high the model bandwidth do you need?

Port Mapping and Port Counts

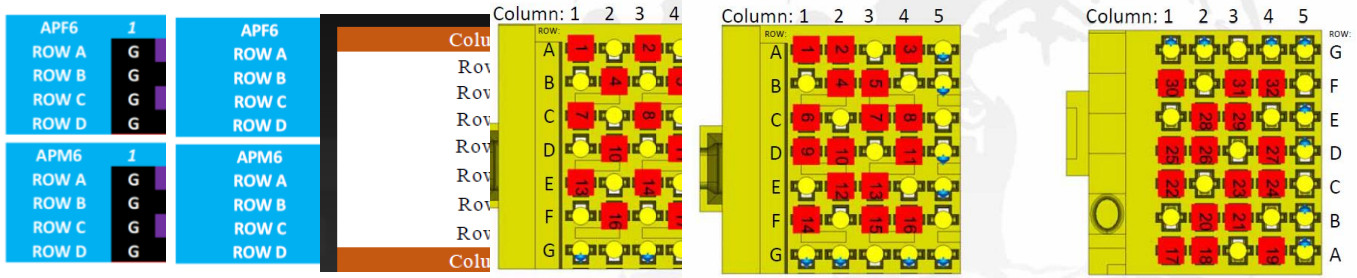


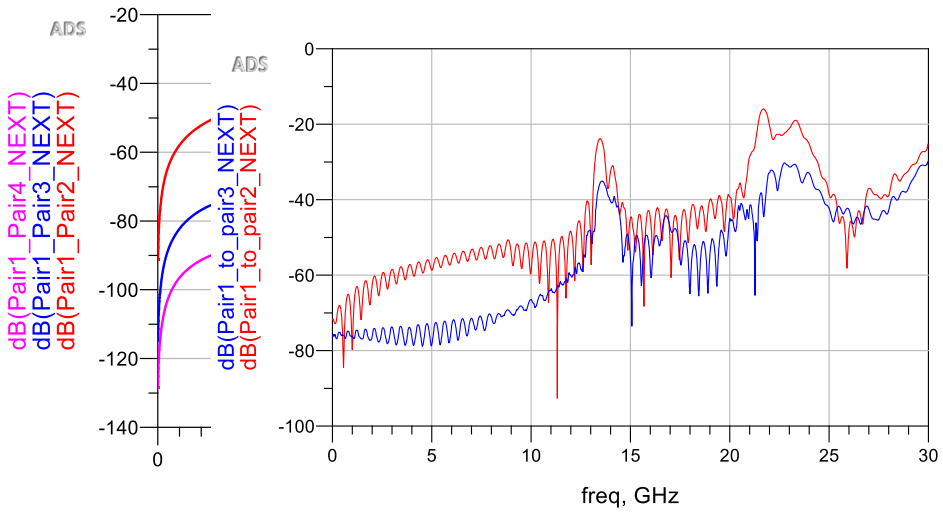
Pair 1 Pair 2 Pair 3 Pair 4

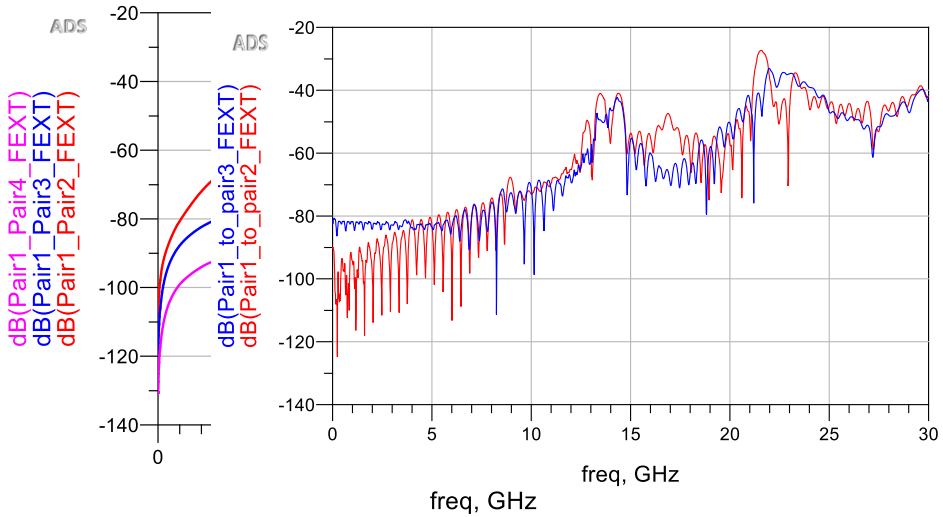
GND	Signal 1	Signal 2	GND	Signal 3	Signal 4	GND	Signal 5	Signal 6	GND	Signal 7	Signal 8	GND

GND	GND	Signal 1	Signal 2	GND	GND	Signal 3	Signal 4	GND	GND	Signal 5	Signal 6	GND	GND

Port/Pin D Pin/Port Definition



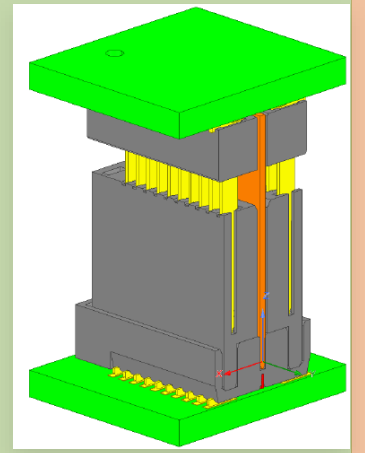


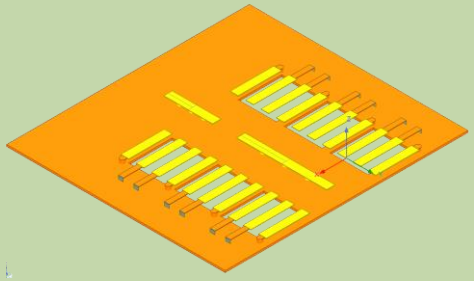


Model Boundary

Two Row Connector

- Pin definition simulated
  - Pin Mapping: GSSG
- PCB effects
  - IT180 w/ 1mm of microstrip trace on each side
    - 2mm in total
  - Antipad under signal pads
- Bandwidth: 0 GHz - 20 GHz
  - Linear Steps: 10 MHz (2001 points)
  - Max Delta S: 0.01
  - Number of passes: 30
- Sweep type: Interpolating



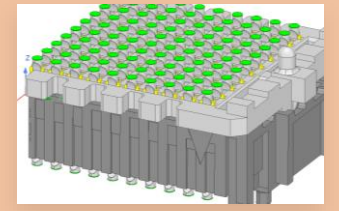


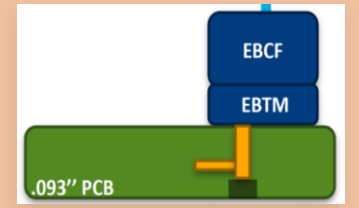
PIN	2	4	6	8	10	12	14	16	18	20
QTE		19	20		21	22		23	24	
QSE		7	8		9	10		11	12	
Assembly Row 2	G	S	S	G	S	S	G	S	S	G
Assembly Row 1	G	S	S	G	S	S	G	S	S	G
QSE		1	2		3	4		5	6	
QTE		13	14		15	16		17	18	
PIN	1	3	5	7	9	11	13	15	17	19

Array Connector

- Pin definition simulated
  - Pin Mapping: GGSSGG
- PCB effects
  - No PCB effect
- Bandwidth: 0 GHz- 30 GHz
  - Linear Steps: 10 MHz (2001 points)
  - Max Delta S: 0.0075
  - Number of passes: 30
- Sweep type: Interpolating

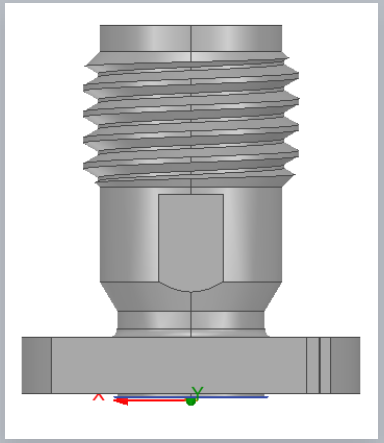
- Footprint Details (Layer 9 (of 14)
- 65mil thru
- 8 mil stub (back
- drilled)
- ~2.5mm low loss lead in trace

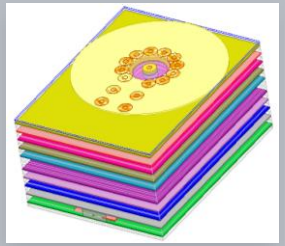


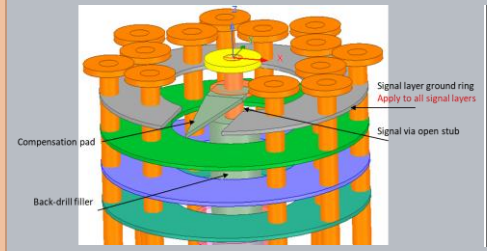


Column	1	2	3	4	5	6	7
Row Y	G	S	S	G	G	S	S
Row Z	T	G	G	S	S	G	G
Row A	G	S	S	G	G	S	S
Row B	T	G	G	S	S	G	G
Row C	G	T	T	G	G	T	T
Column	1	2	3	4	5	6	7

High Precision RF







Anti-Pad diameter for different layers				
Escape Layer	L3	L5	L18	L20
L1	42mil	42mil	42mil	42mil
L2	47mil	37mil	40mil	40mil
L3	47mil	37mil	40mil	40mil
L4	40mil	37mil	40mil	40mil
L5	40mil	47mil	40mil	40mil
L6	40mil	40mil	40mil	40mil
L7	40mil	40mil	40mil	40mil
L8	40mil	40mil	40mil	40mil
L9	40mil	40mil	40mil	40mil
L10	26mil	26mil	44mil	44mil

Keysight ADS

S-parameter in Keysight ADS

SParamChecker

S-PARAMETERS

S_Param

TRANSIENT

Tran

ChannelSim

ChannelSim

Simulators

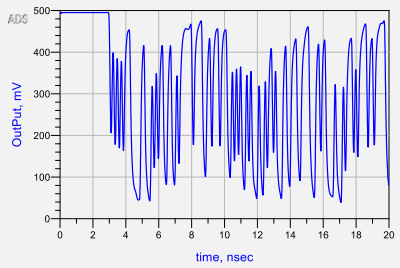
Loss characteristics

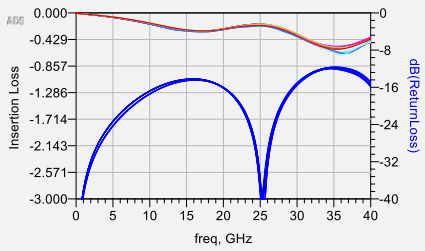
TDR

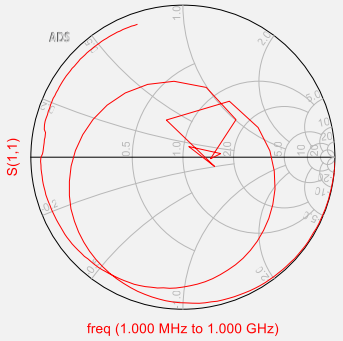
Circuit

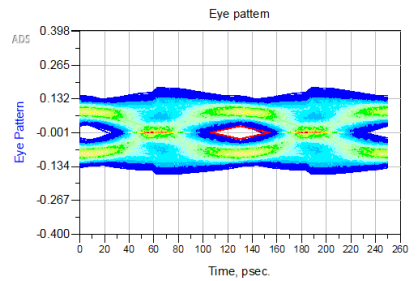
Eye Diagram

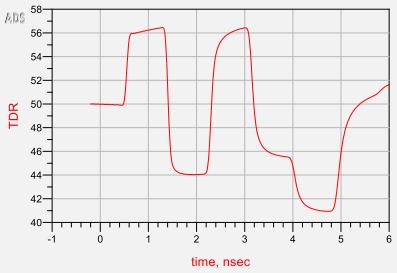
Functions











Results

S-parameter Tool Kit

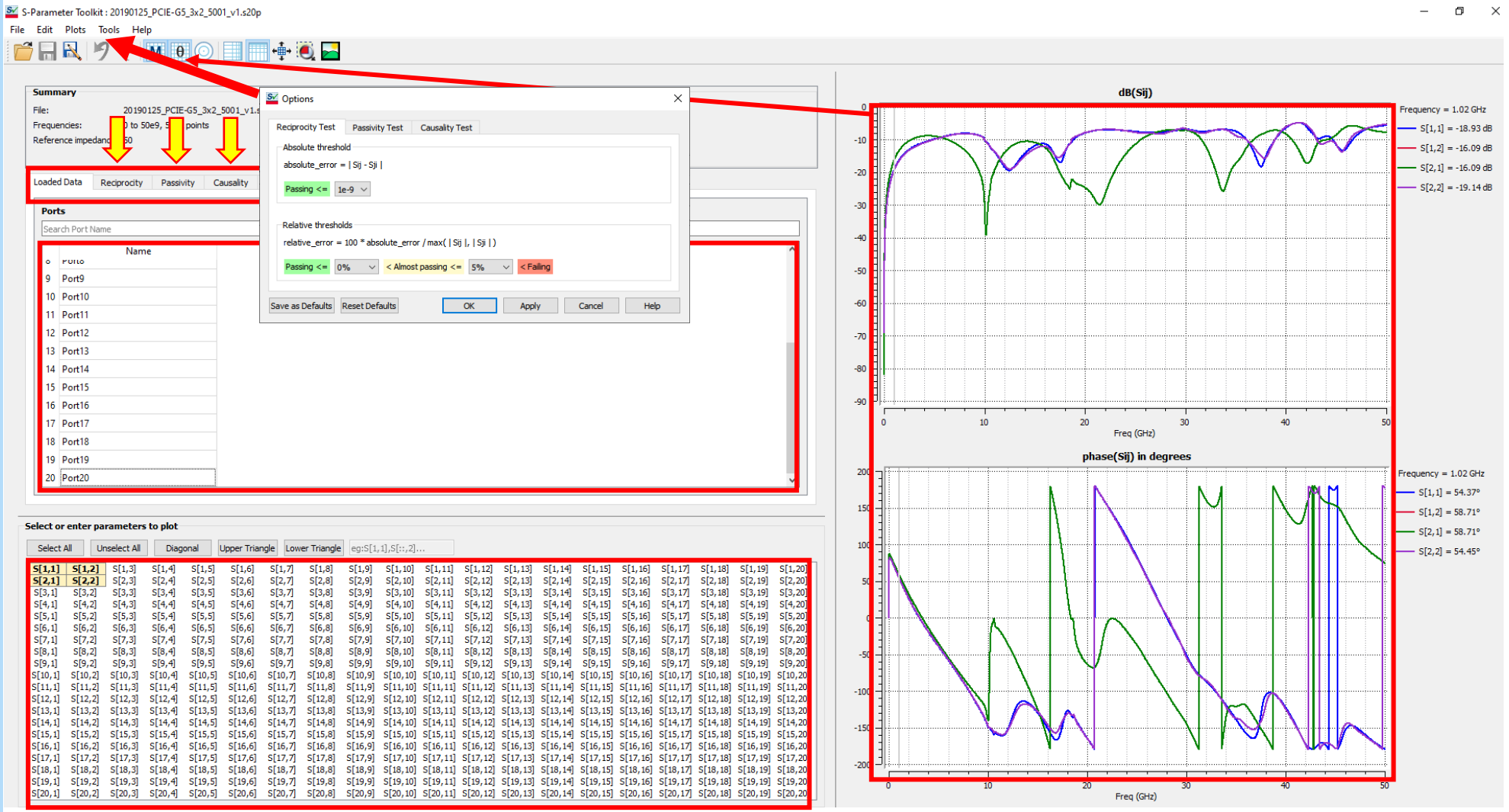
gEEk spEEk

One Model Only

Frequency Domain

TDR/TDT

Model Quality



S-parameter Tool Kit - Port Mapping

gEEk spEEk

S-Parameter Toolkit : 20190125_PCIE-G5_3x2_5001_v1.s20p*

File Edit Plots Tools Help

Summary

File: 20190125_PCIE-G5_3x2_5001_v1.s20p
Frequencies: 0 to 50e9, 5001 points
Reference impedance: 50
S-parameters: 20x20
Reciprocity: Almost
Passivity: Yes
Causality: No data available

Loaded Data | Reciprocity | Passivity | Causality | Single-Ended | Differential | TDR/TDT

Assign Through Ports | Reload Through Ports Info | Remove All

Side 1 Baseboard

Diff Port #	Pin Name	Port #
1	16A	1
	17A	2
2	21A	3
	22A	4
3	25A	5
	A26	6
4	14B	7
	15B	8
5	19B	9
	20B	10
6	23B	11
	24B	12

S-Parameters

Side 2 Edge Card

Port #	Pin Name	Diff Port #
13	16A	7
14	17A	
15	21A	8
16	22A	
17	25A	9
18	A26	
19	14B	10
20	15B	
21	19B	11
22	20B	
23	23B	12
24	24B	

Connector Port Mapping

Select or enter

Select All

Assign Through Ports

Select Ports | Setup Through Ports

How are the ports paired between two sides?

- (●) Fixed port configuration
  - ( ) 1 | 2, 3 | 4, 5 | 6, 7 | 8
  - (●) 1 | 5, 2 | 6, 3 | 7, 4 | 8
  - ( ) 1 | 8, 2 | 7, 3 | 6, 4 | 5
- ( ) Power-flow detection configuration (choose a topology arrangement below)
  - ( ) Odd/Even
  - ( ) Contiguous
- ( ) Custom

	Side A	Side B
1	Port1	Port11
2	Port2	Port12
3	Port3	Port13
4	Port4	Port14
5	Port5	Port15
6	Port6	Port16
7	Port7	Port17
8	Port8	Port18
9	Port9	Port19
10	Port10	Port20

< Back | Finish | Cancel | Help

Assign Differential Ports

Select two through ports to make a differential pair.

Make Differential Pair | Remove Differential Pair(s) | Remove All

Differential Pairs	Through Ports #	Side A	Side B
1	1	Port1	Port11
	2	Port2	Port12
2	3	Port3	Port13
	4	Port4	Port14
	5	Port5	Port15
	6	Port6	Port16
	7	Port7	Port17
	8	Port8	Port18
	9	Port9	Port19
	10	Port10	Port20

OK | Cancel | Help

S-parameter Tool Kit - Frequency Domain

gEEk spEEk

S-Parameter Toolkit : 20190125_PCIE-G5_3x2_5001_v1.s20p*

File Edit Plots Tools Help

Summary

File: 20190125_PCIE-G5_3x2_5001_v1.s20p S-parameters: 20x20
Frequencies: 0 to 50e9, 5001 points Reciprocity: Almost
Reference impedance: 50 Passivity: Yes
Causality: No data a

Loaded Data | Reciprocity | Passivity | Causality | Single-Ended | Differential

Assign Through Ports | Reload Through Ports Info | Remove All

Through Ports

Search Port Name

	Side A	Side B
1	Port1	Port11
2	Port2	Port12
3	Port3	Port13
4	Port4	Port14
5	Port5	Port15
6	Port6	Port16
7	Port7	Port17
8	Port8	Port18
9	Port9	Port19
10	Port10	Port20

Select or enter parameters to plot

Select All | Unselect All | Diagonal | Upper Triangle | Lower Triangle | eg:S[1

S[1,1]	S[1,2]	S[1,3]	S[1,4]	S[1,5]	S[1,6]	S[1,7]	S[1,8]	S[1,9]
S[2,1]	S[2,2]	S[2,3]	S[2,4]	S[2,5]	S[2,6]	S[2,7]	S[2,8]	S[2,9]
S[3,1]	S[3,2]	S[3,3]	S[3,4]	S[3,5]	S[3,6]	S[3,7]	S[3,8]	S[3,9]
S[4,1]	S[4,2]	S[4,3]	S[4,4]	S[4,5]	S[4,6]	S[4,7]	S[4,8]	S[4,9]
S[5,1]	S[5,2]	S[5,3]	S[5,4]	S[5,5]	S[5,6]	S[5,7]	S[5,8]	S[5,9]
S[6,1]	S[6,2]	S[6,3]	S[6,4]	S[6,5]	S[6,6]	S[6,7]	S[6,8]	S[6,9]
S[7,1]	S[7,2]	S[7,3]	S[7,4]	S[7,5]	S[7,6]	S[7,7]	S[7,8]	S[7,9]
S[8,1]	S[8,2]	S[8,3]	S[8,4]	S[8,5]	S[8,6]	S[8,7]	S[8,8]	S[8,9]
S[9,1]	S[9,2]	S[9,3]	S[9,4]	S[9,5]	S[9,6]	S[9,7]	S[9,8]	S[9,9]
S[10,1]	S[10,2]	S[10,3]	S[10,4]	S[10,5]	S[10,6]	S[10,7]	S[10,8]	S[10,9]
S[11,1]	S[11,2]	S[11,3]	S[11,4]	S[11,5]	S[11,6]	S[11,7]	S[11,8]	S[11,9]
S[12,1]	S[12,2]	S[12,3]	S[12,4]	S[12,5]	S[12,6]	S[12,7]	S[12,8]	S[12,9]
S[13,1]	S[13,2]	S[13,3]	S[13,4]	S[13,5]	S[13,6]	S[13,7]	S[13,8]	S[13,9]
S[14,1]	S[14,2]	S[14,3]	S[14,4]	S[14,5]	S[14,6]	S[14,7]	S[14,8]	S[14,9]
S[15,1]	S[15,2]	S[15,3]	S[15,4]	S[15,5]	S[15,6]	S[15,7]	S[15,8]	S[15,9]
S[16,1]	S[16,2]	S[16,3]	S[16,4]	S[16,5]	S[16,6]	S[16,7]	S[16,8]	S[16,9]
S[17,1]	S[17,2]	S[17,3]	S[17,4]	S[17,5]	S[17,6]	S[17,7]	S[17,8]	S[17,9]
S[18,1]	S[18,2]	S[18,3]	S[18,4]	S[18,5]	S[18,6]	S[18,7]	S[18,8]	S[18,9]
S[19,1]	S[19,2]	S[19,3]	S[19,4]	S[19,5]	S[19,6]	S[19,7]	S[19,8]	S[19,9]
S[20,1]	S[20,2]	S[20,3]	S[20,4]	S[20,5]	S[20,6]	S[20,7]	S[20,8]	S[20,9]

S-Parameter Toolkit : 20190125_PCIE-G5_3x2_5001_v1.s20p*

File Edit Plots Tools Help

Summary

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Frequencies: 0 to 50e9, 5001 points Reciprocity: Almost
Reference impedance: 50 Passivity: Yes
Causality: No data available

Loaded Data | Reciprocity | Passivity | Causality | Single-Ended | Differential | TDR/TDT

Assign Differential Ports | Calculate Differential Data | Reload Differential Pair Info | Remove All

Through Ports

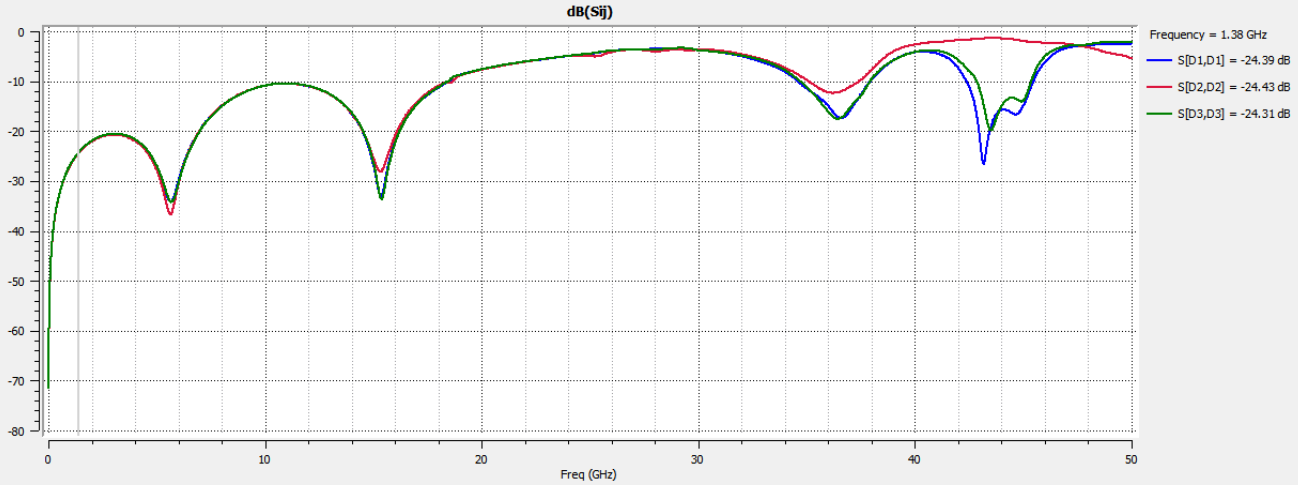
Search Port Name

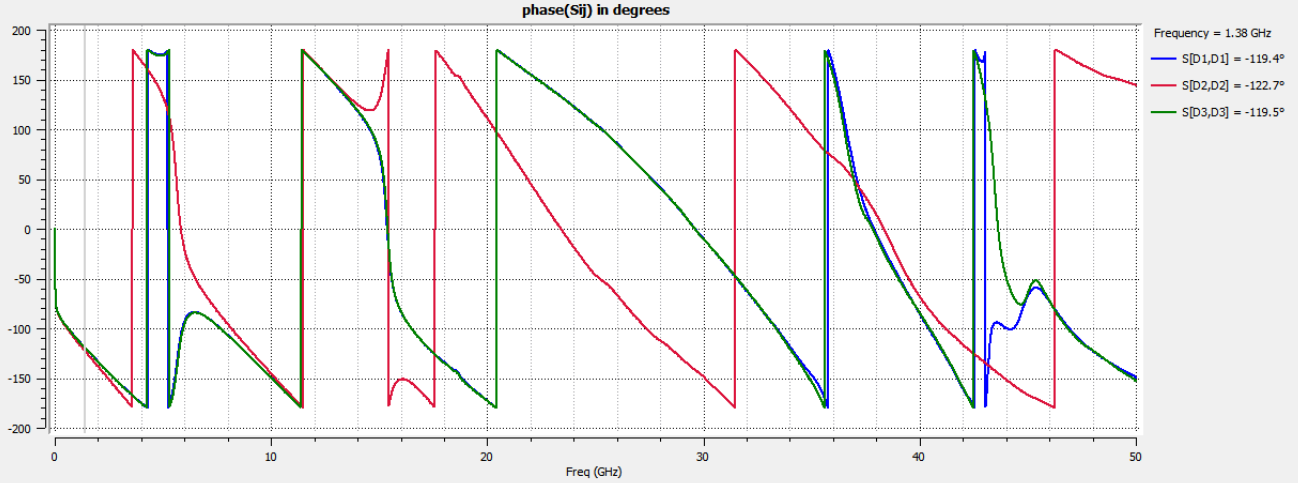
	Side A	Side B
1	Diff. Port 1: (Port1,Port2)	Diff. Port 2: (Port11,Port12)
2	Diff. Port 3: (Port3,Port4)	Diff. Port 4: (Port13,Port14)
3	Diff. Port 5: (Port5,Port6)	Diff. Port 6: (Port15,Port16)
4	Diff. Port 7: (Port7,Port8)	Diff. Port 8: (Port17,Port18)
5	Diff. Port 9: (Port9,Port10)	Diff. Port 10: (Port19,Port20)

Select or enter parameters to plot

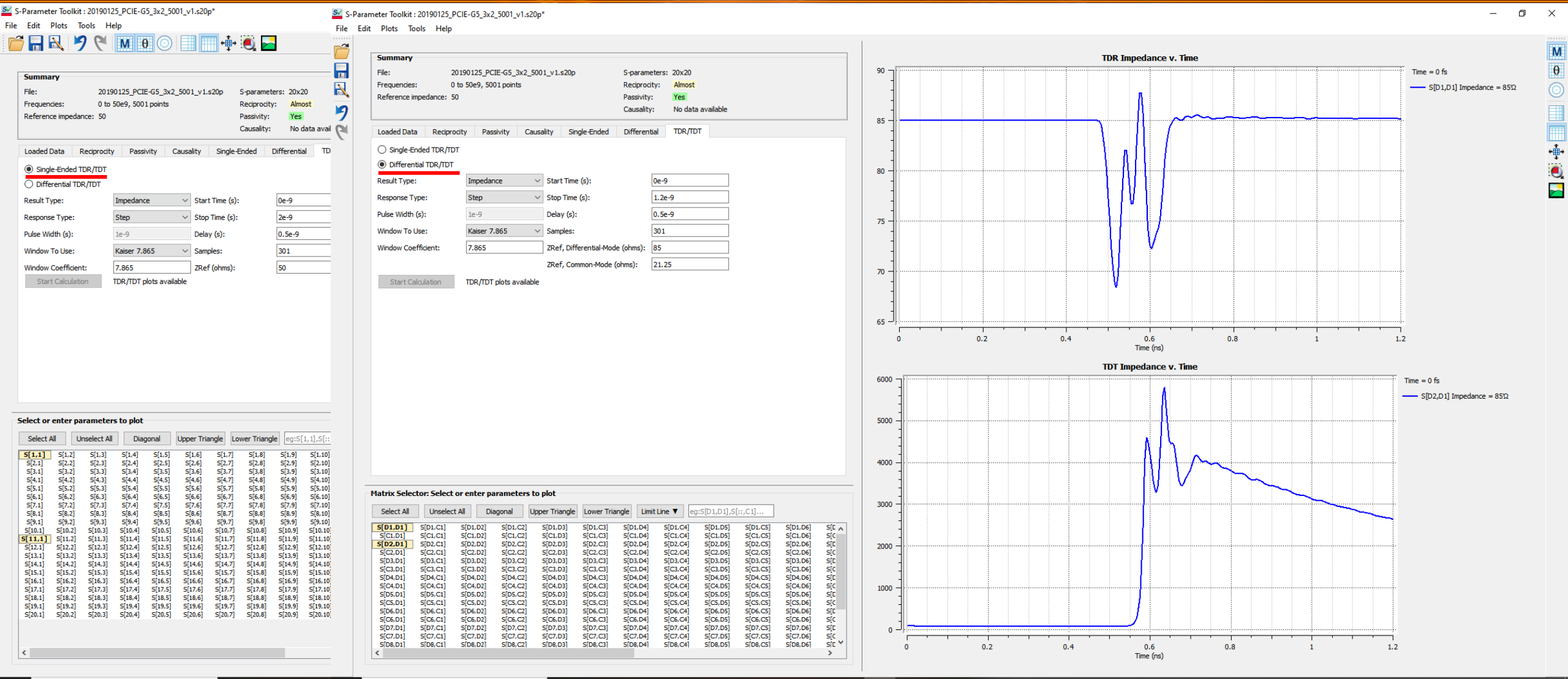
Select All | Unselect All | Diagonal | Upper Triangle | Lower Triangle | eg:S[D1,D1],S[::,C1]...

S[D1,D1]	S[D1,C1]	S[D1,D2]	S[D1,C2]	S[D1,D3]	S[D1,C3]	S[D1,D4]	S[D1,C4]	S[D1,D5]
S[C1,D1]	S[C1,C1]	S[C1,D2]	S[C1,C2]	S[C1,D3]	S[C1,C3]	S[C1,D4]	S[C1,C4]	S[C1,D5]
S[D2,D1]	S[D2,C1]	S[D2,D2]	S[D2,C2]	S[D2,D3]	S[D2,C3]	S[D2,D4]	S[D2,C4]	S[D2,D5]
S[C2,D1]	S[C2,C1]	S[C2,D2]	S[C2,C2]	S[C2,D3]	S[C2,C3]	S[C2,D4]	S[C2,C4]	S[C2,D5]
S[D3,D1]	S[D3,C1]	S[D3,D2]	S[D3,C2]	S[D3,D3]	S[D3,C3]	S[D3,D4]	S[D3,C4]	S[D3,D5]
S[C3,D1]	S[C3,C1]	S[C3,D2]	S[C3,C2]	S[C3,D3]	S[C3,C3]	S[C3,D4]	S[C3,C4]	S[C3,D5]
S[D4,D1]	S[D4,C1]	S[D4,D2]	S[D4,C2]	S[D4,D3]	S[D4,C3]	S[D4,D4]	S[D4,C4]	S[D4,D5]
S[C4,D1]	S[C4,C1]	S[C4,D2]	S[C4,C2]	S[C4,D3]	S[C4,C3]	S[C4,D4]	S[C4,C4]	S[C4,D5]
S[D5,D1]	S[D5,C1]	S[D5,D2]	S[D5,C2]	S[D5,D3]	S[D5,C3]	S[D5,D4]	S[D5,C4]	S[D5,D5]
S[C5,D1]	S[C5,C1]	S[C5,D2]	S[C5,C2]	S[C5,D3]	S[C5,C3]	S[C5,D4]	S[C5,C4]	S[C5,D5]
S[D6,D1]	S[D6,C1]	S[D6,D2]	S[D6,C2]	S[D6,D3]	S[D6,C3]	S[D6,D4]	S[D6,C4]	S[D6,D5]
S[C6,D1]	S[C6,C1]	S[C6,D2]	S[C6,C2]	S[C6,D3]	S[C6,C3]	S[C6,D4]	S[C6,C4]	S[C6,D5]
S[D7,D1]	S[D7,C1]	S[D7,D2]	S[D7,C2]	S[D7,D3]	S[D7,C3]	S[D7,D4]	S[D7,C4]	S[D7,D5]
S[C7,D1]	S[C7,C1]	S[C7,D2]	S[C7,C2]	S[C7,D3]	S[C7,C3]	S[C7,D4]	S[C7,C4]	S[C7,D5]
S[D8,D1]	S[D8,C1]	S[D8,D2]	S[D8,C2]	S[D8,D3]	S[D8,C3]	S[D8,D4]	S[D8,C4]	S[D8,D5]
S[C8,D1]	S[C8,C1]	S[C8,D2]	S[C8,C2]	S[C8,D3]	S[C8,C3]	S[C8,D4]	S[C8,C4]	S[C8,D5]
S[D9,D1]	S[D9,C1]	S[D9,D2]	S[D9,C2]	S[D9,D3]	S[D9,C3]	S[D9,D4]	S[D9,C4]	S[D9,D5]
S[C9,D1]	S[C9,C1]	S[C9,D2]	S[C9,C2]	S[C9,D3]	S[C9,C3]	S[C9,D4]	S[C9,C4]	S[C9,D5]
S[D10,D1]	S[D10,C1]	S[D10,D2]	S[D10,C2]	S[D10,D3]	S[D10,C3]	S[D10,D4]	S[D10,C4]	S[D10,D5]
S[C10,D1]	S[C10,C1]	S[C10,D2]	S[C10,C2]	S[C10,D3]	S[C10,C3]	S[C10,D4]	S[C10,C4]	S[C10,D5]



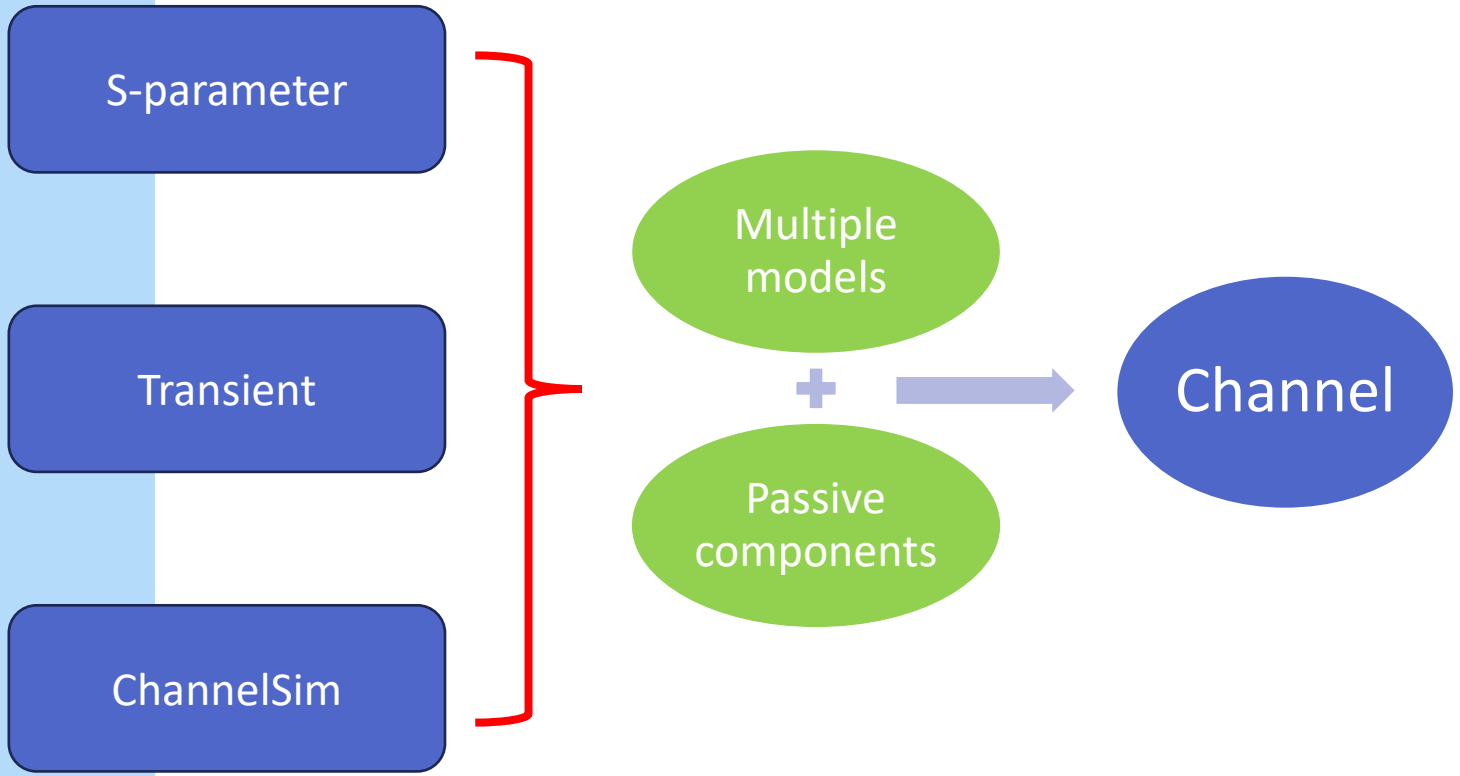


S-parameter Tool Kit - TDR/TDT



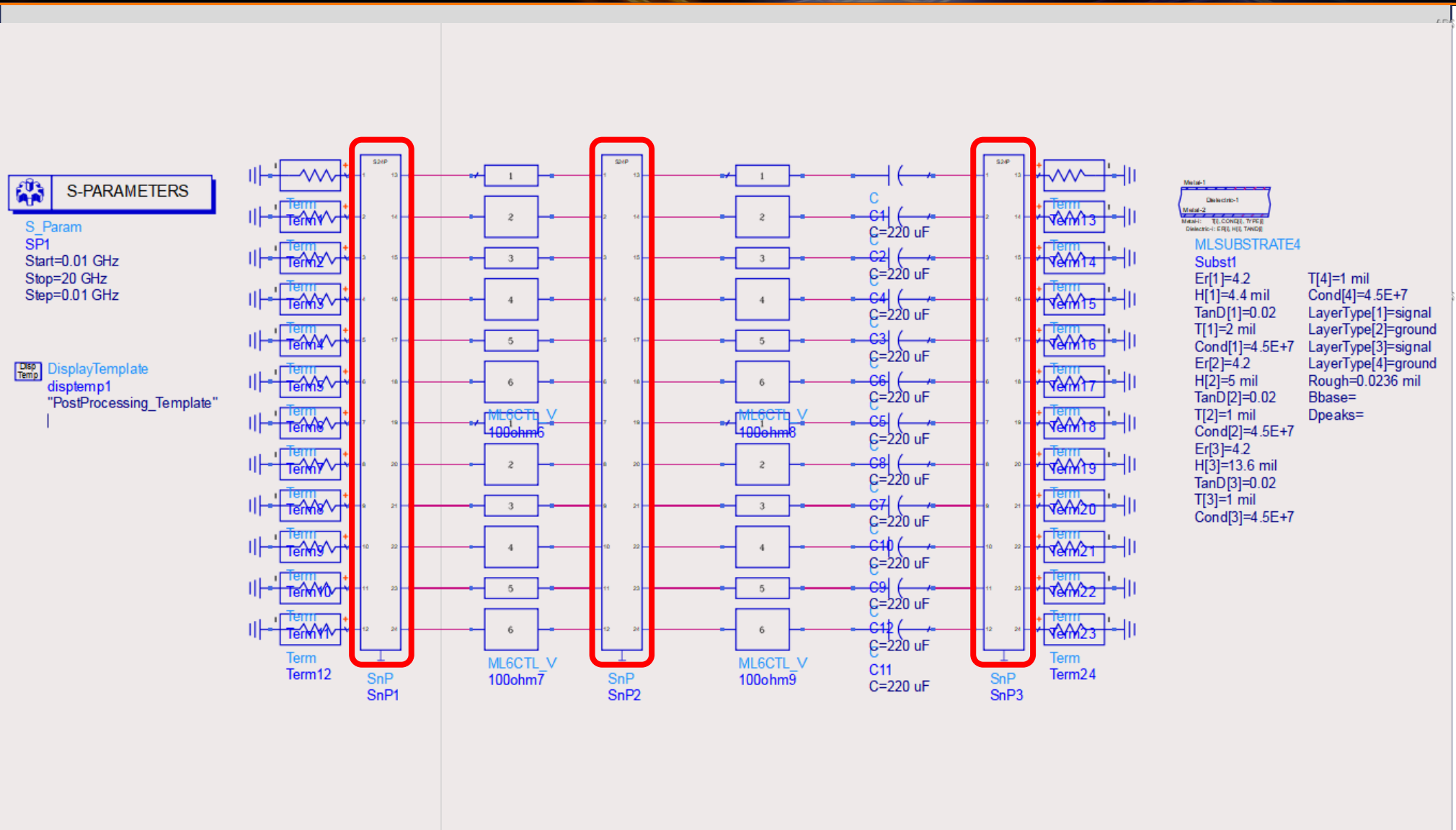
Simulators in ADS

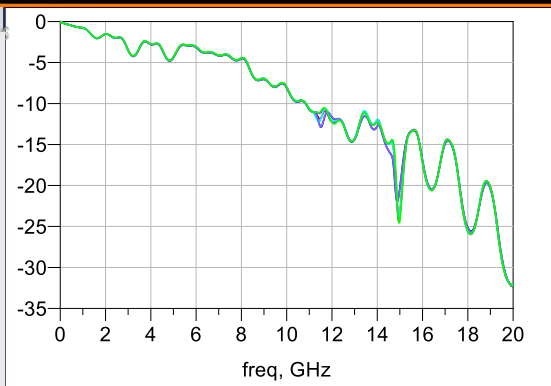
PATHWAVE
Advanced Design System

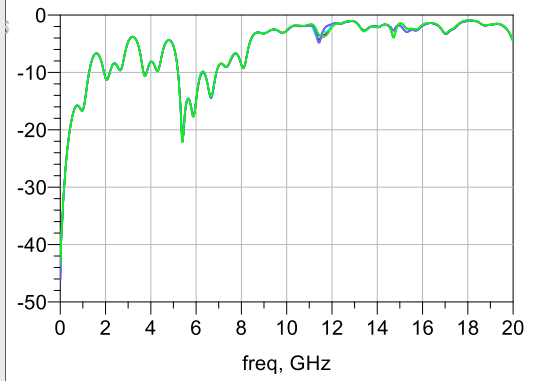


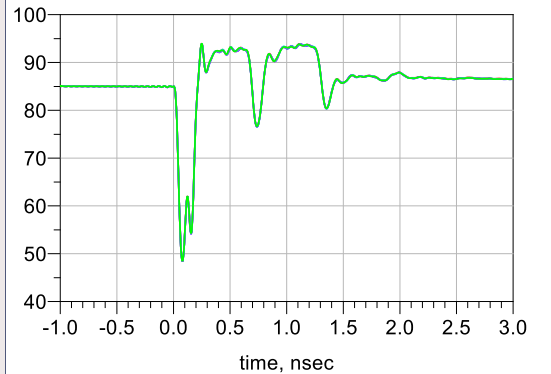
- **Short Simulation time**
- **Compliance Simulation**
- **Loss Contribution for Each component**
- **Find the "Good Enough"**

Simulators - Frequency Domain Simulation

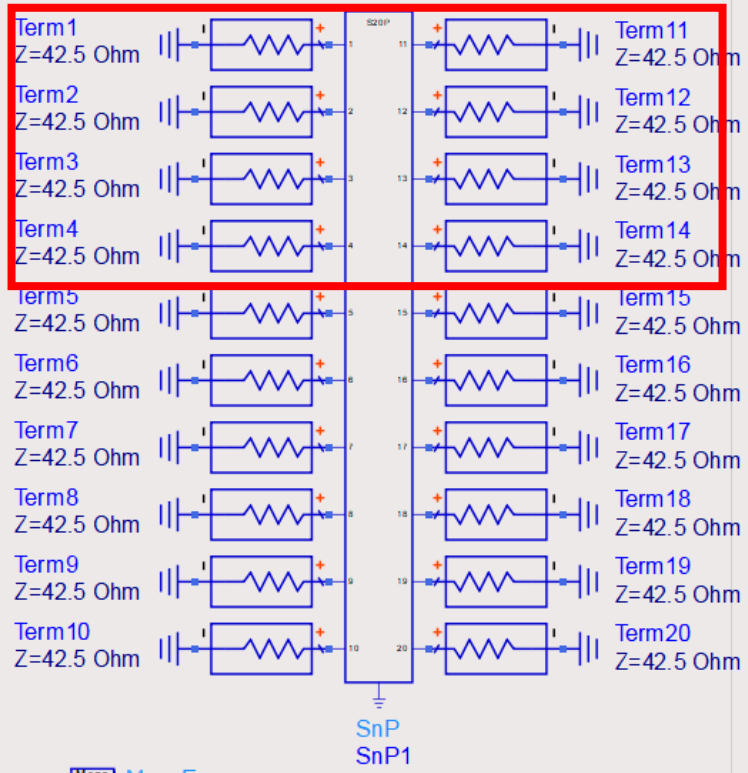




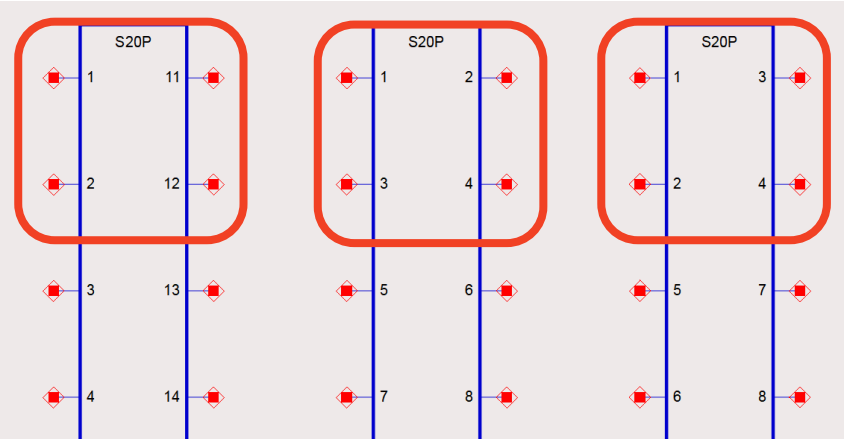




S-parameter - The Port Mapping!



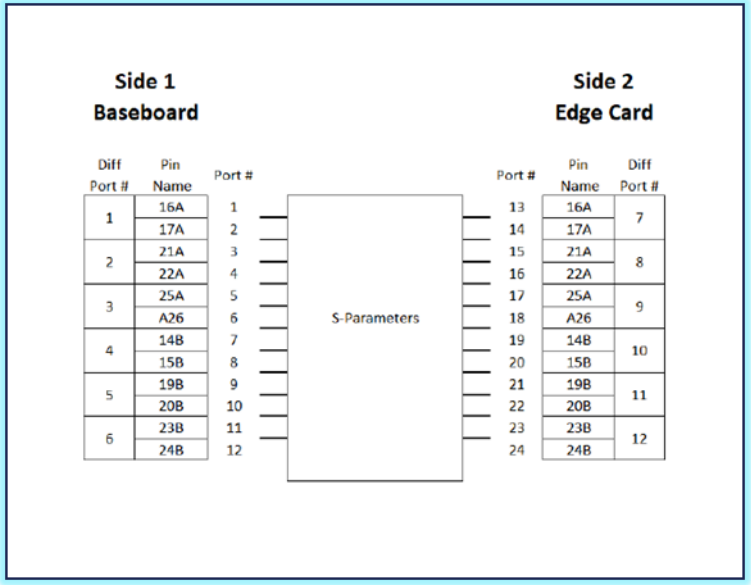
MeasEqn
Meas1
Pair1_SDD11=0.5*(S(1,1)-S(2,2)-S(2,1)+S(1,2))
Pair1_SDD22=0.5*(S(11,11)-S(12,12)-S(12,11)+S(11,12))
Pair1_SDD21=0.5*(S(11,1)-S(11,2)-S(12,1)+S(12,2))
Pair1_SDD12=0.5*(S(1,11)-S(12,1)-S(11,2)+S(2,12))



Single-ended port configuration

DD Quadrant

Eqn SDD11=0.5*(S(1,1)-S(1,3)-S(3,1)+S(3,3))
Eqn SDD12=0.5*(S(1,2)-S(1,4)-S(3,2)+S(3,4))
Eqn SDD21=0.5*(S(2,1)-S(2,3)-S(4,1)+S(4,3))
Eqn SDD22=0.5*(S(2,2)-S(2,4)-S(4,2)+S(4,4))



Connector Port Mapping

S-parameter Simulator - Mode Conversion

For single-ended S-parameters:

an=(1/(2*sqrt(Re(Zn))))*(Vn+(In*Zn))

bn=(1/(2*sqrt(Re(Zn))))*(Vn-(In*Zn))

S=b/a

(where a=stimulus, b=response)

S port resp., port stim

For mixed-mode S-parameters:

	Differential	Common
Voltage	Vd=Van - Vbn	Vc= 0.5 * (Van + Vbn)
Current	Id=0.5 * (Ian - Ibn)	Ic=Ian + Ibn
Impedance	Zdn = Vd+/Id+	Zcn = Vc+/Ic+

adn=(1/(2*sqrt(Re(Zdn))))*(Vdn+(Idn*Zdn))
acn=(1/(2*sqrt(Re(Zcn))))*(Vcn+(Icn*Zcn))
bdn=(1/(2*sqrt(Re(Zdn))))*(Vdn-(Idn*Zdn))
bcn=(1/(2*sqrt(Re(Zcn))))*(Vcn-(Icn*Zcn))

S=b/a

(where a=stimulus, b=response)

S mode resp., mode stim., port resp., port stim

Single-ended port configuration

Mixed-mode port configuration

Mixed-Mode S-Matrix
(derived from single-ended S-Matrix)

DD Quadrant

Eqn SDD11=0.5*(S(1,1)-S(1,3)-S(3,1)+S(3,3))
Eqn SDD12=0.5*(S(1,2)-S(1,4)-S(3,2)+S(3,4))
Eqn SDD21=0.5*(S(2,1)-S(2,3)-S(4,1)+S(4,3))
Eqn SDD22=0.5*(S(2,2)-S(2,4)-S(4,2)+S(4,4))

DC Quadrant

Eqn SDC11=0.5*(S(1,1)+S(1,3)-S(3,1)-S(3,3))
Eqn SDC12=0.5*(S(1,2)+S(1,4)-S(3,2)-S(3,4))
Eqn SDC21=0.5*(S(2,1)+S(2,3)-S(4,1)-S(4,3))
Eqn SDC22=0.5*(S(2,2)+S(2,4)-S(4,2)-S(4,4))

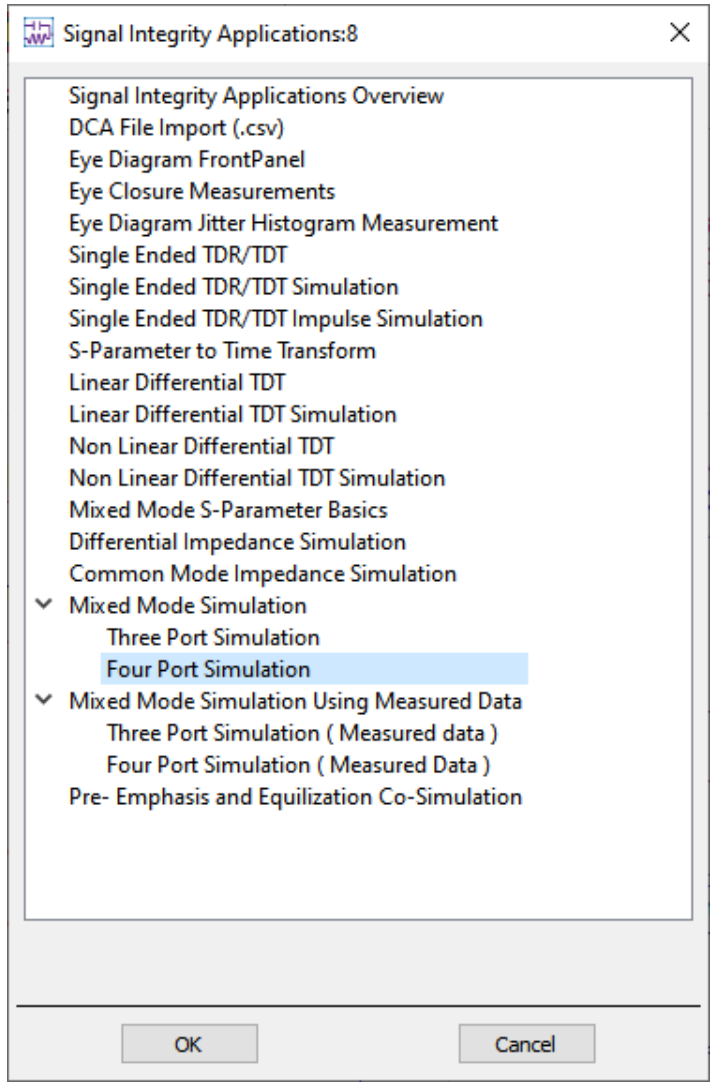
Eqn SCD11=0.5*(S(1,1)-S(1,3)+S(3,1)-S(3,3))
Eqn SCD12=0.5*(S(1,2)-S(1,4)+S(3,2)-S(3,4))
Eqn SCD21=0.5*(S(2,1)-S(2,3)+S(4,1)-S(4,3))
Eqn SCD22=0.5*(S(2,2)-S(2,4)+S(4,2)-S(4,4))

CD Quadrant

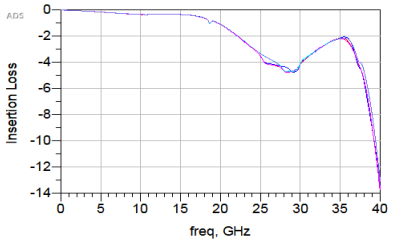
Eqn SCC11=0.5*(S(1,1)+S(1,3)+S(3,1)+S(3,3))
Eqn SCC12=0.5*(S(1,2)+S(1,4)+S(3,2)+S(3,4))
Eqn SCC21=0.5*(S(2,1)+S(2,3)+S(4,1)+S(4,3))
Eqn SCC22=0.5*(S(2,2)+S(2,4)+S(4,2)+S(4,4))

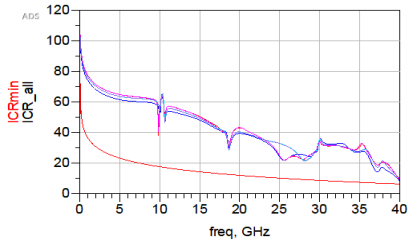
CC Quadrant

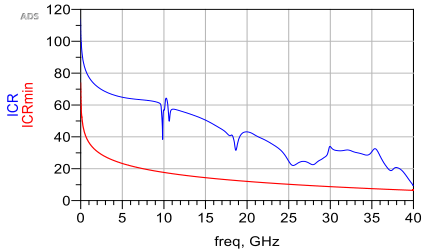
DD Quadrant: Pure Differential Quadrant
CC Quadrant: Pure Common-mode Quadrant
CD Quadrant: Differential stimulus, Common-mode response (related to generation of EMI)
DC Quadrant: Common-mode stimulus, Differential response (related to susceptibility to EMI)

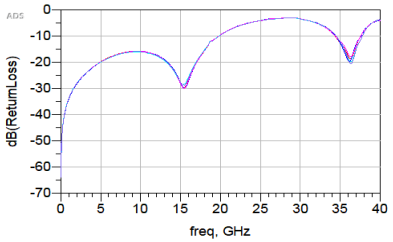


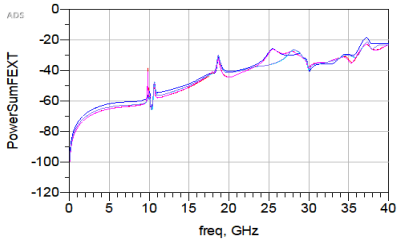
S-parameter Simulator - Display Template

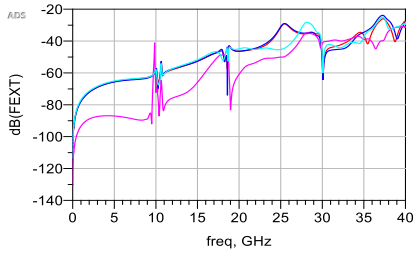


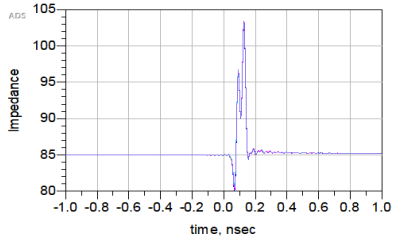


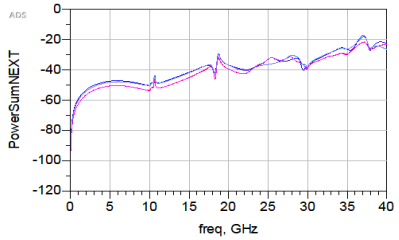


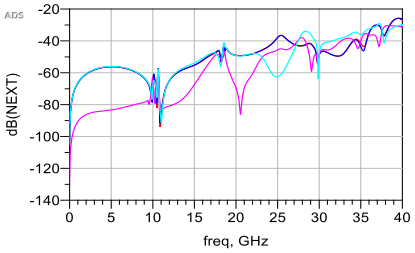


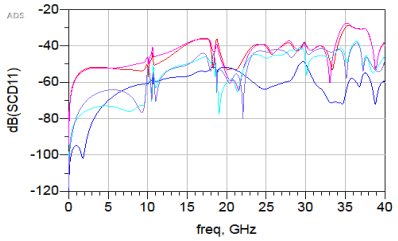


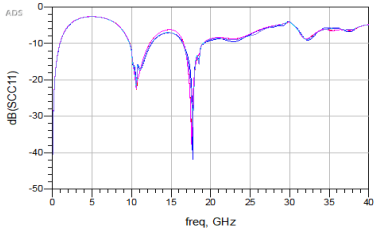










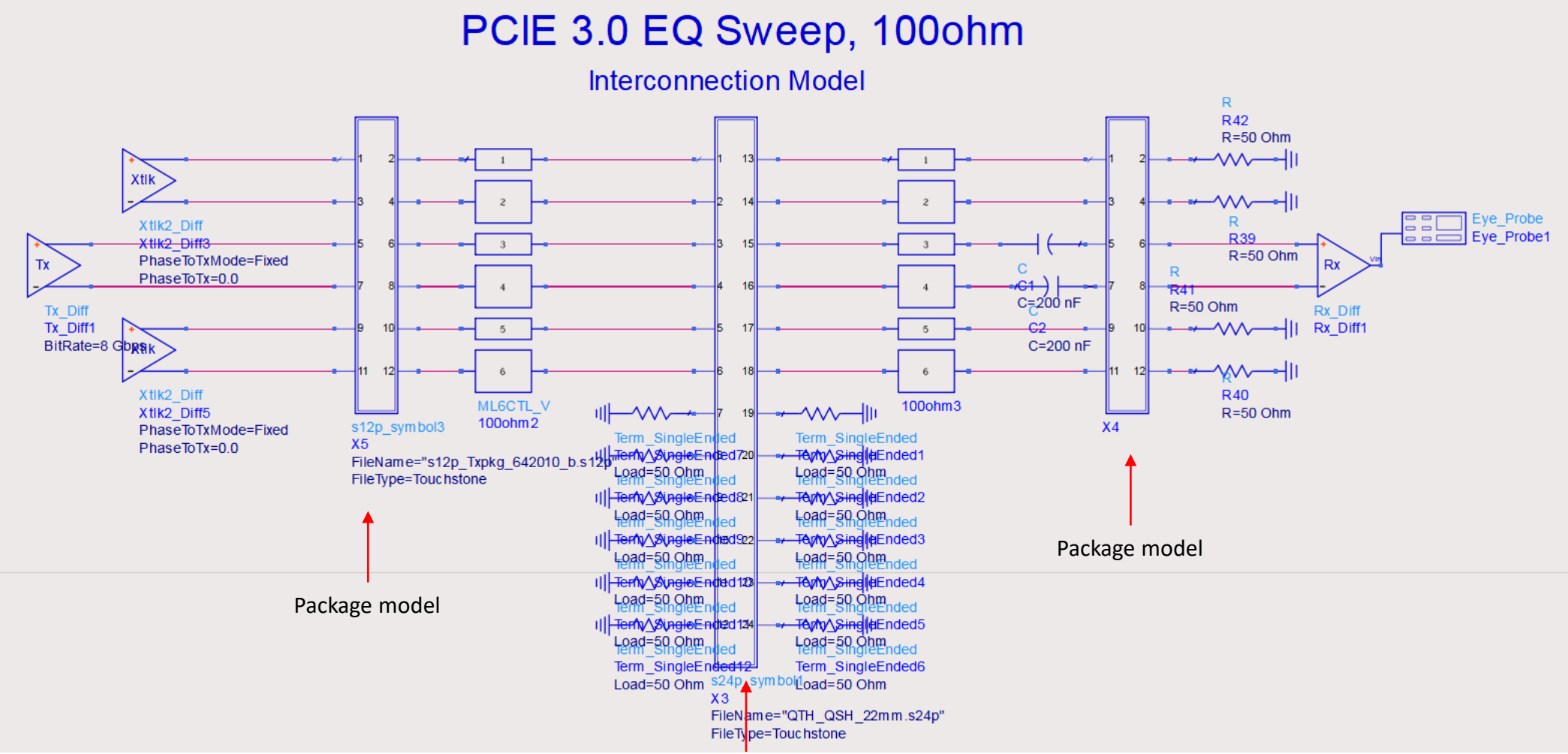



```
Eqn ICR=dB(InsertionLoss)(m1_index+1)-PowerSumFEXT(m1_index+1)
Eqn ICR_all=dB(InsertionLoss)-PowerSumFEXT
Eqn ICRmin=23.3-18.7*log(freq/(5*10**9))
Eqn NEXT=NEXTDP(S,PortMapping)
Eqn FEXT=FEXTDP(S,PortMapping)
Eqn Impedance=ImpedDP(ReturnLoss,RefZ,ImpedStopTime)
Eqn PairIndex=[1::size(InsertionLoss)]

Eqn PowerSumFEXT=10*log((PSFEXT(S,PortMapping)))
Eqn PowerSumNEXT=10*log((PSNEXT(S,PortMapping)))

Eqn VoltageSumFEXT=10*log((VSFEXT(S,PortMapping)))
Eqn SCC11=SCC11T(S,PortMapping)
Eqn SCD11=SCD11T(S,PortMapping)
```

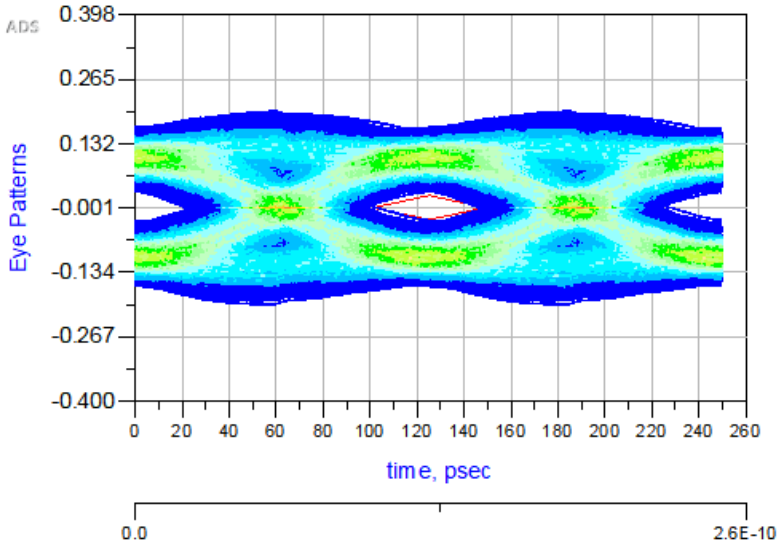
ChannelSim - Eye Diagram



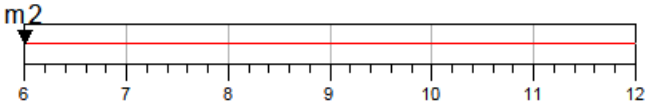
samtec

gEEk spEEk

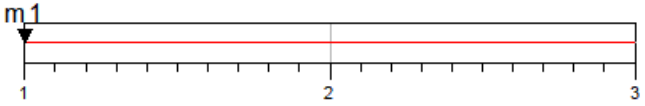
Eyes



[101.25 psec+shift,125 psec +shift,148.75 psec+shift]



m2
ADC_db=6.000



m1
batchNumber=1

Eye width and height requirement

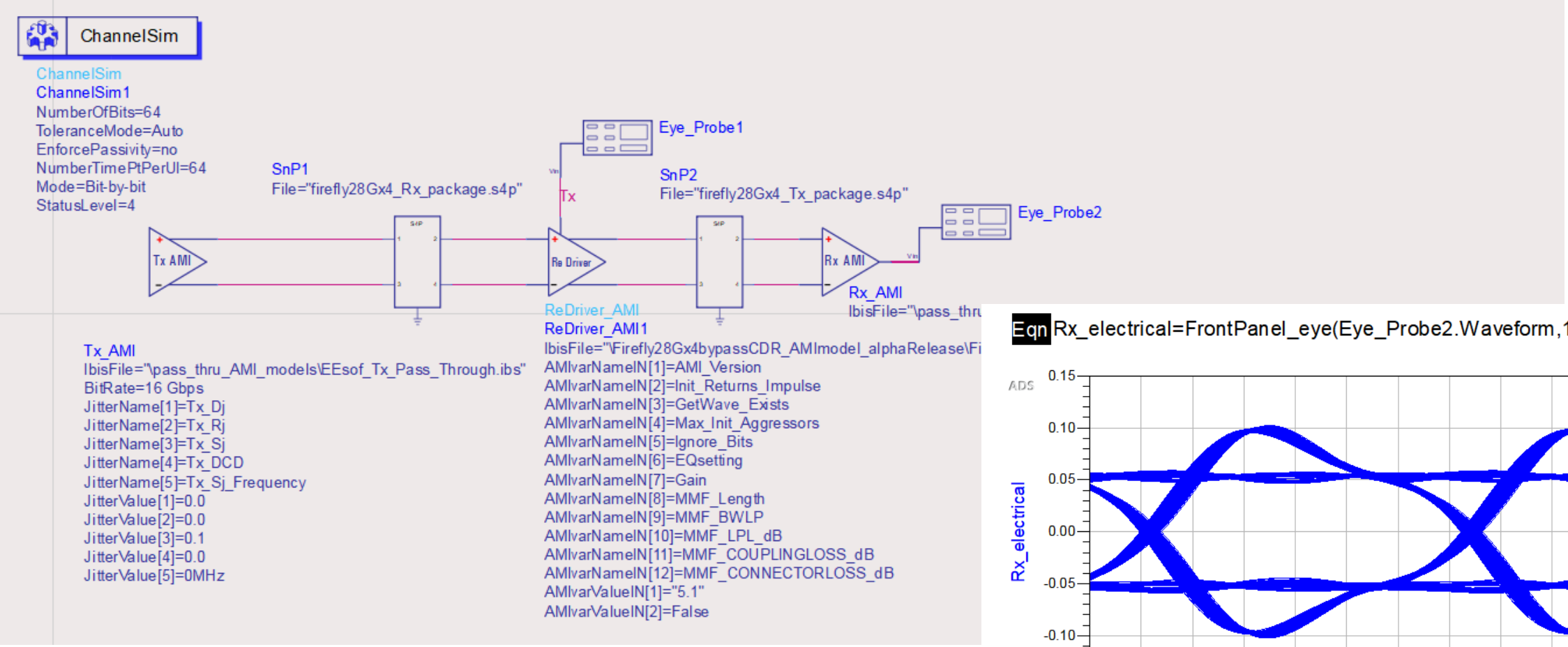
Eqn height=50mV Eqn width=3.75e-11

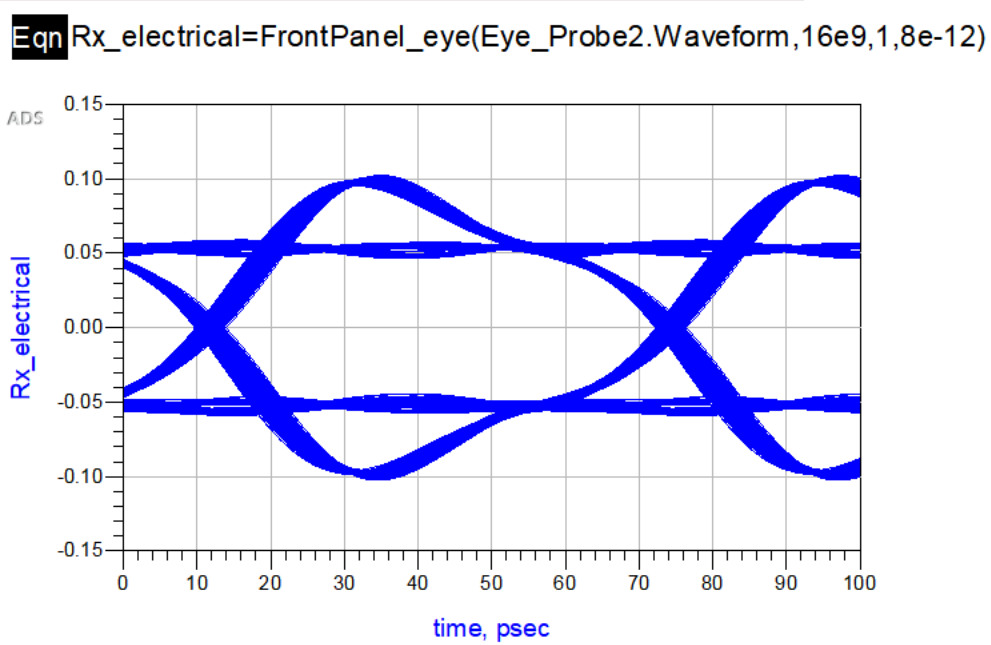
Preset1_Height	Preset1_Width	Preset1_result
0.058	4.688E-11	Pass
0.057	4.656E-11	Pass
0.057	4.625E-11	Pass
0.055	4.531E-11	Pass
0.052	4.469E-11	Pass
0.051	4.312E-11	Pass
0.048	4.125E-11	Fail

Preset8_Height	Preset8_Width	Preset8_result
0.066	4.406E-11	Pass
0.064	4.437E-11	Pass
0.063	4.406E-11	Pass
0.059	4.312E-11	Pass
0.056	4.250E-11	Pass
0.053	4.094E-11	Pass
0.051	4.000E-11	Pass

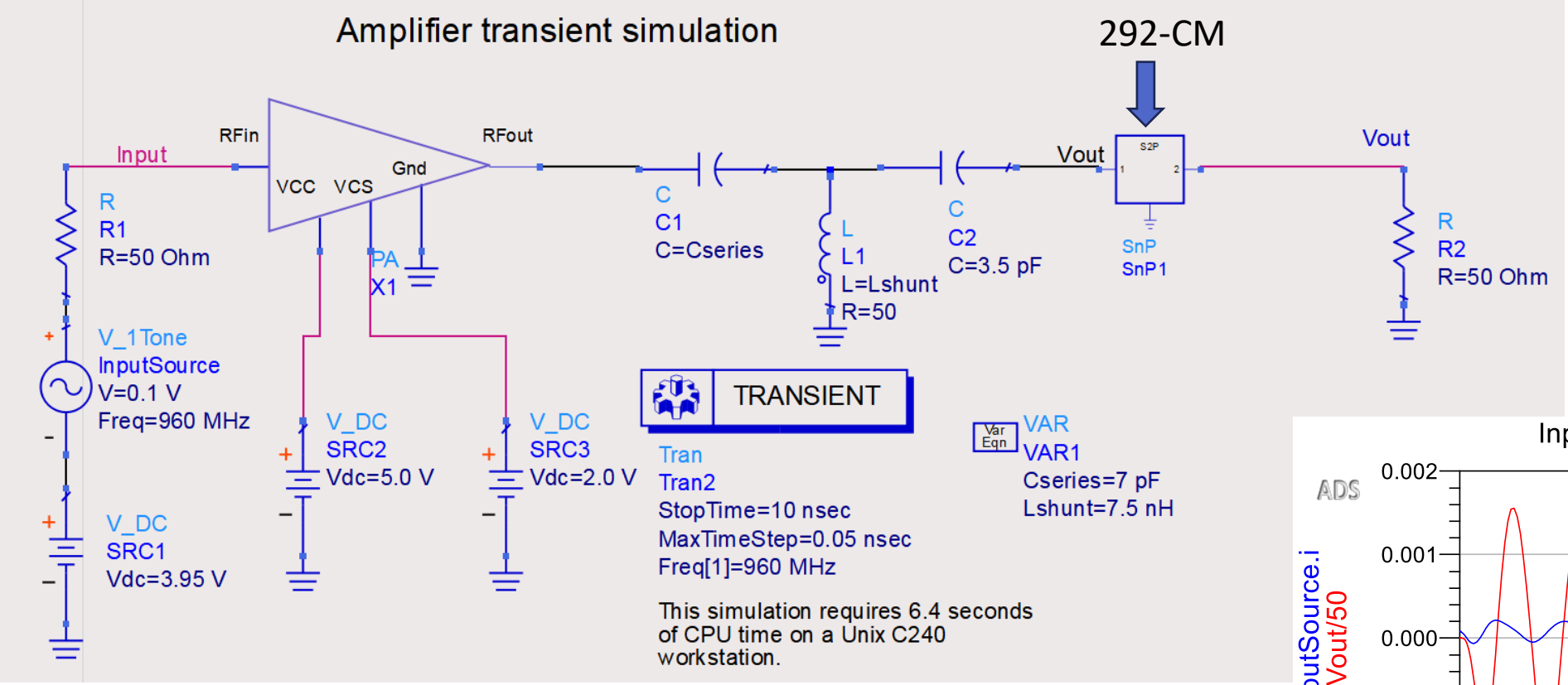
Preset7_Height	Preset7_Width	Preset7_result
0.062	4.375E-11	Pass
0.059	4.344E-11	Pass
0.056	4.156E-11	Pass
0.054	4.125E-11	Pass
0.051	4.062E-11	Pass
0.048	4.000E-11	Fail
0.046	3.875E-11	Fail

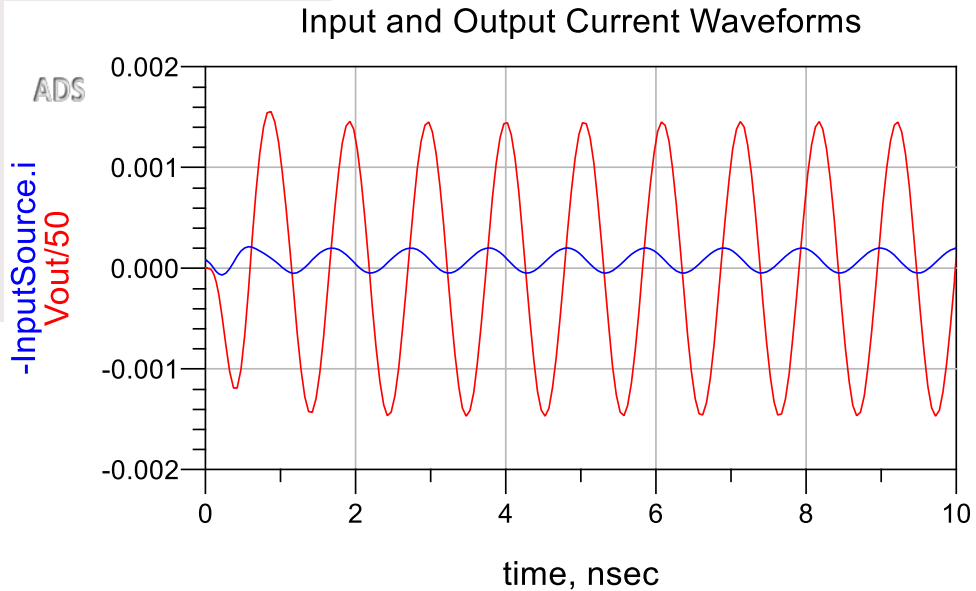
ChannelSim - Eye Diagram (IBIS AMI)





Transient - Circuit





Summary

- Frequency dependent
- Accurate
- Easy to use
- Short simulation time
- Good for both frequency and time domain
- Good for different EDA tools
- Available for most of the connectors & Cables

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