



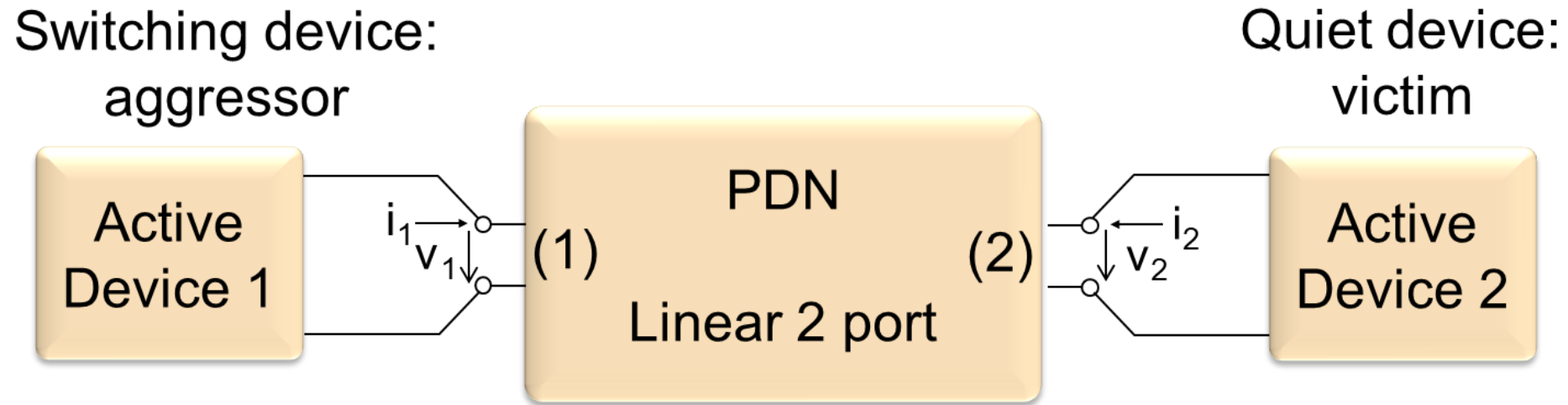
How to Measure Low PDN Impedance

Istvan Novak | Samtec, Inc.
March 16, 2023

Outline

- Why impedance?
- What values do we need to measure?
- One-port impedance measurement
- Two-port shunt-through impedance measurement
- The cable braid error
- Reducing cable braid error
- Dynamic range requirement
- New challenges
- Good measurement practices

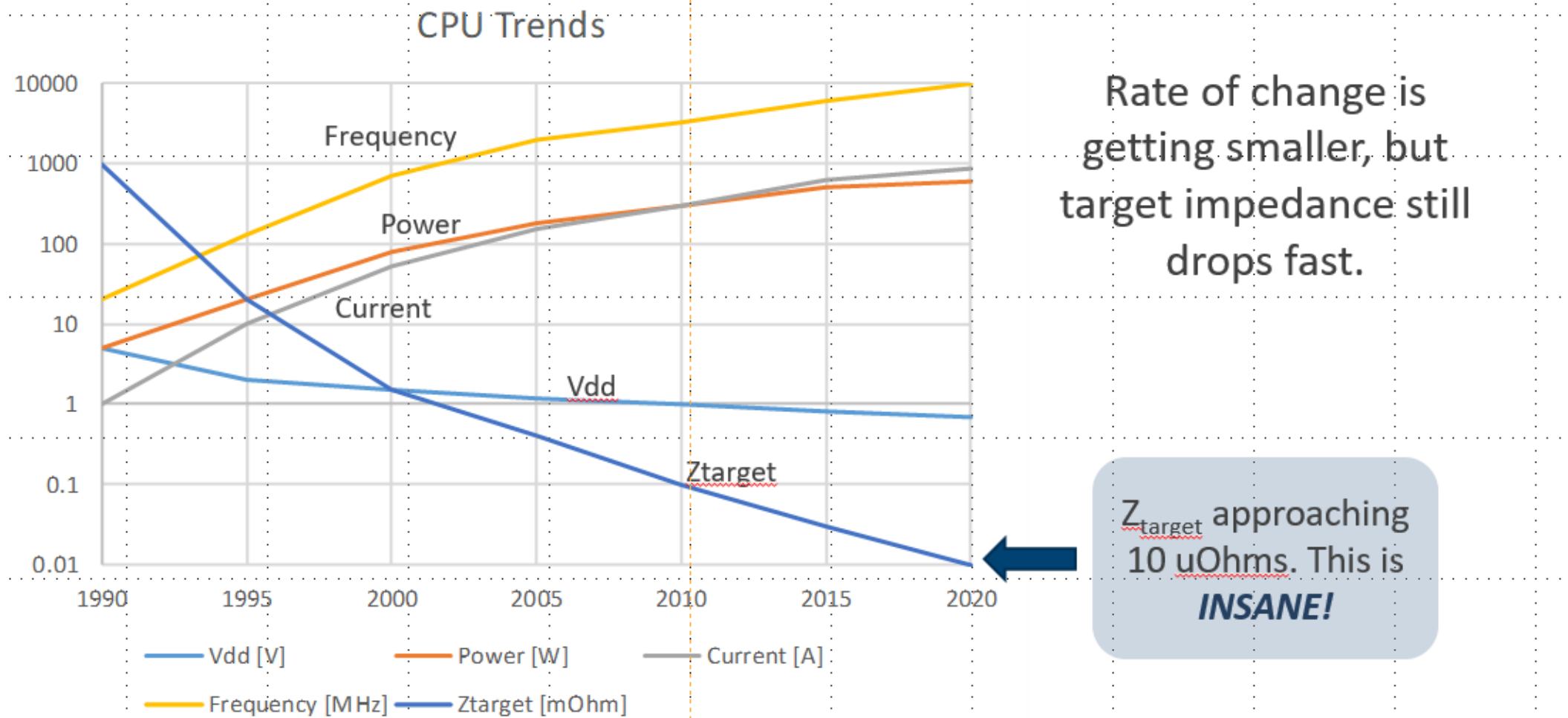
Why Impedance?



Transfer function for self-inflicted noise: $v_1/i_1 = Z_{11}$, while $I_2 = 0 \gg$ Self impedance

Transfer function for propagated noise: $v_2/i_1 = Z_{21}$, while $I_2 = 0 \gg$ Transfer impedance

What Values Do We Need to Measure?



Can We Measure μOhms Based on Reflection?

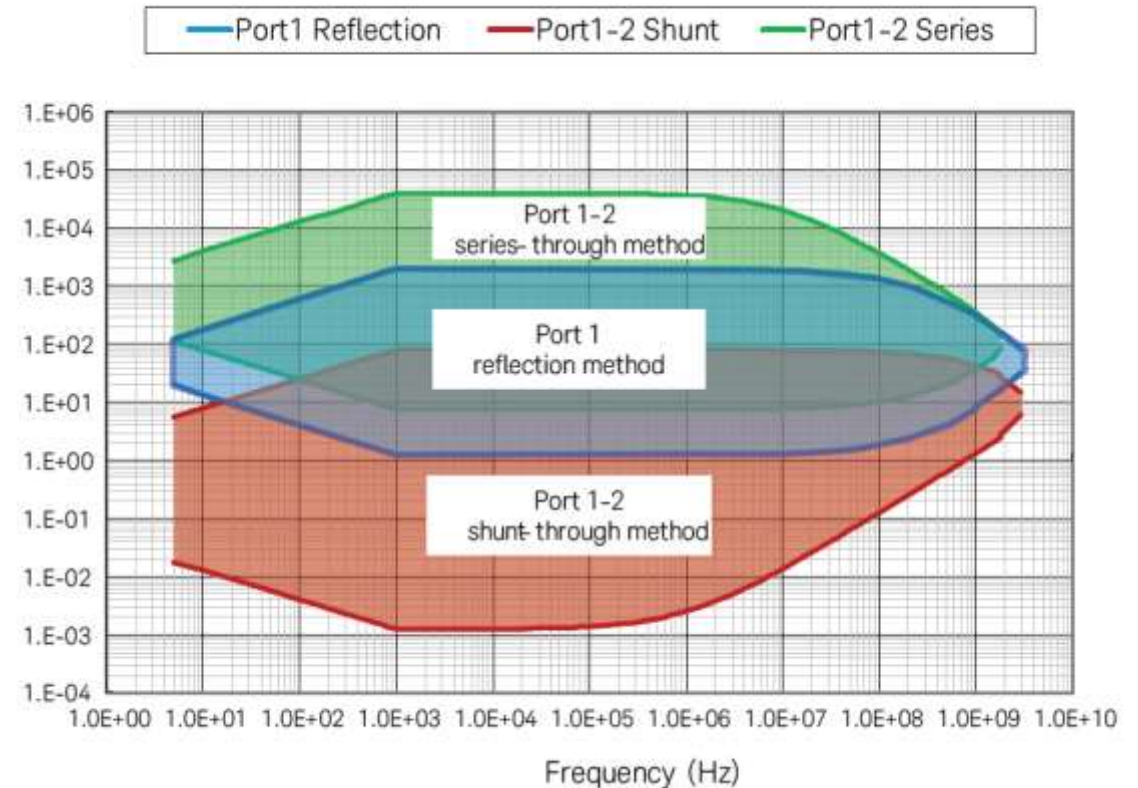


Terminal adapter on Port1
Recommended impedance range:
1 Ohm to 10 kOhm



Keysight Application Note 5991-0213A

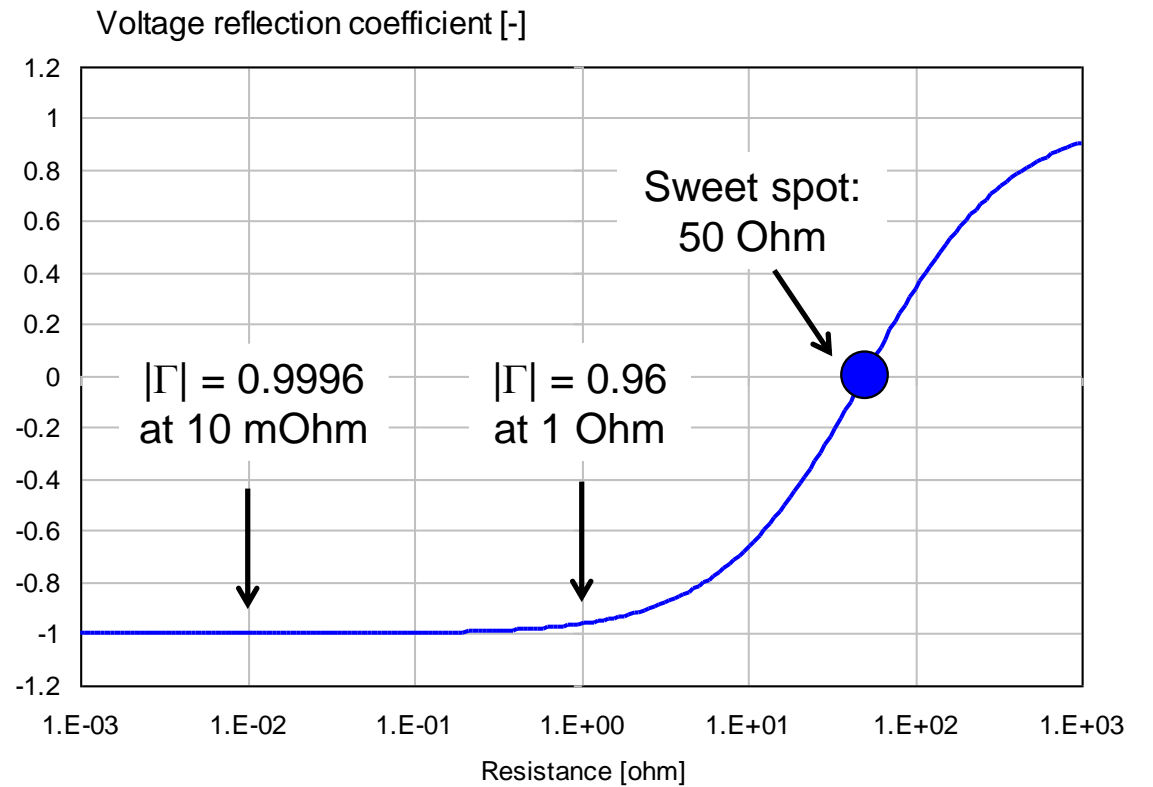
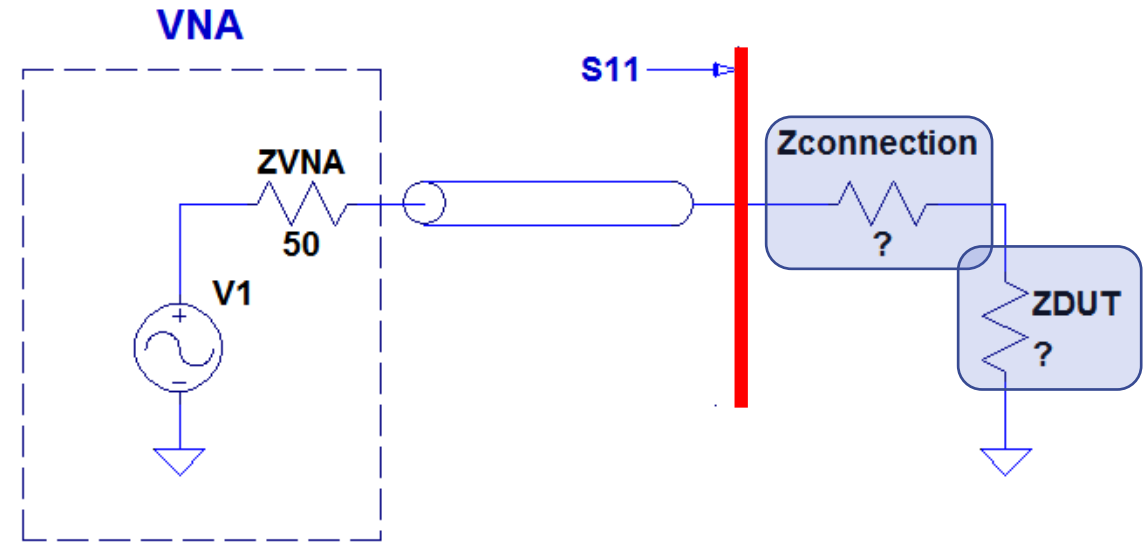
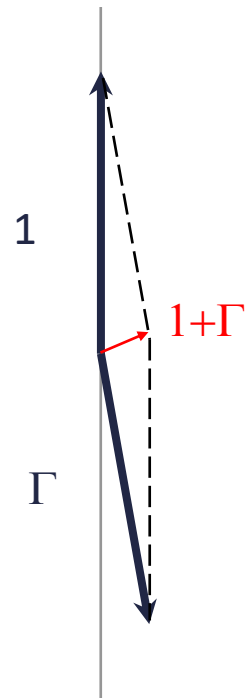
Port1 Reflection dynamic range: 1 : 10,000



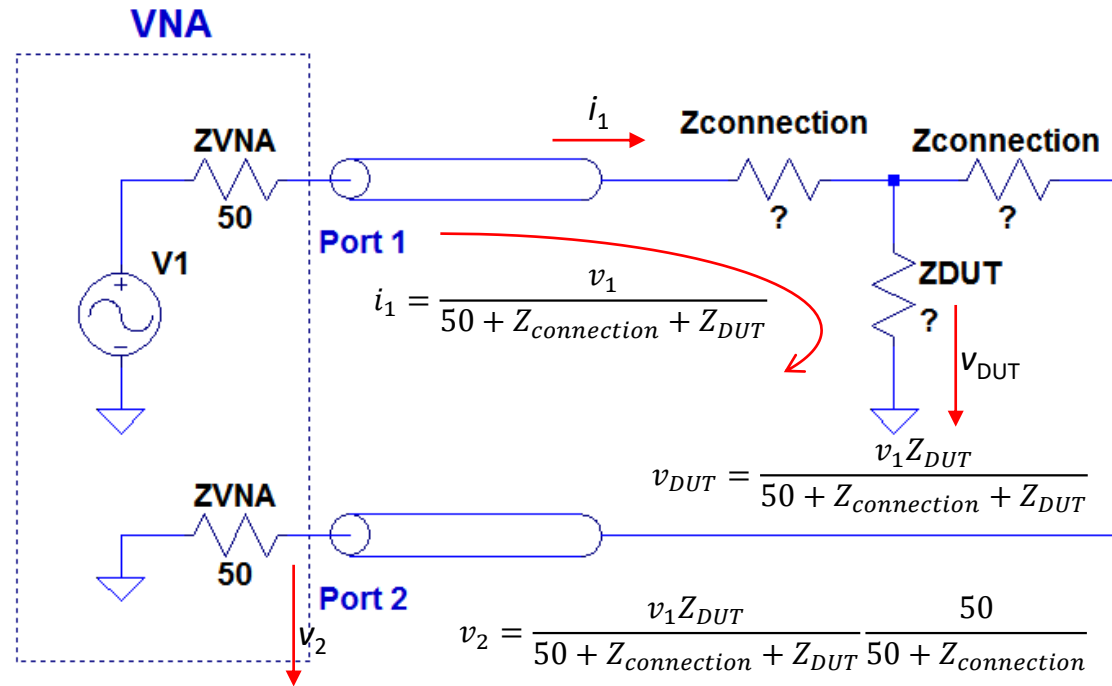
The Problem

$$\Gamma = \frac{Z_{DUT} - Z_{VNA}}{Z_{DUT} + Z_{VNA}}$$

$$Z_{DUT} = Z_{VNA} \frac{1 + \Gamma}{1 - \Gamma}$$



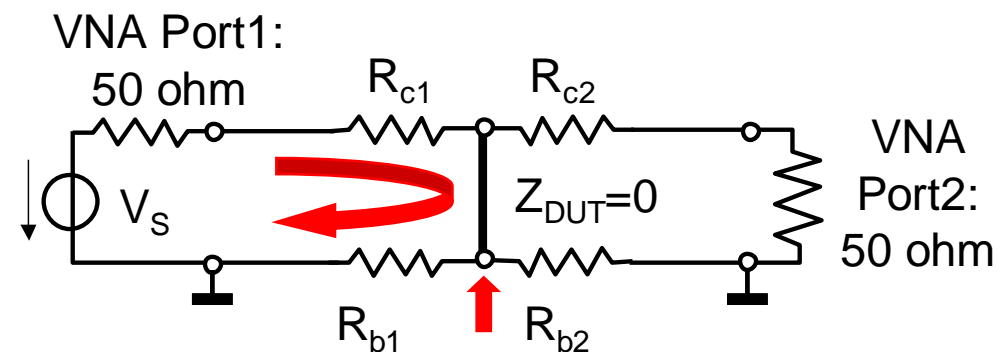
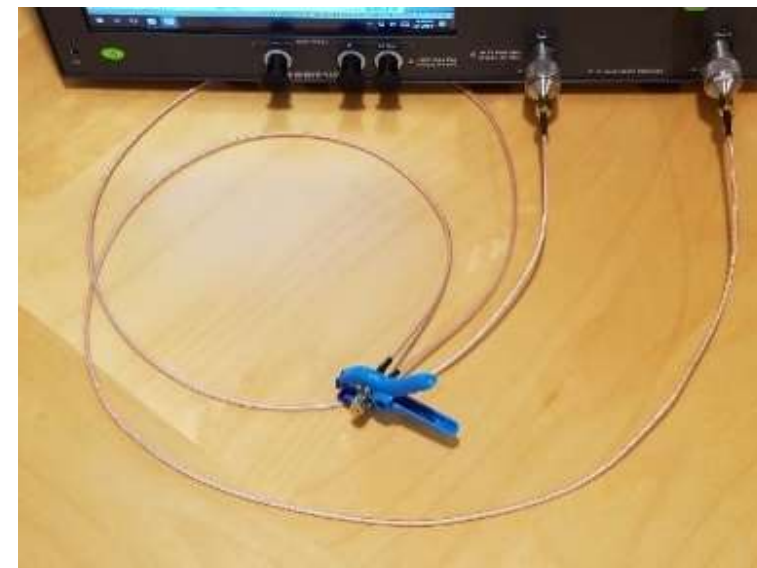
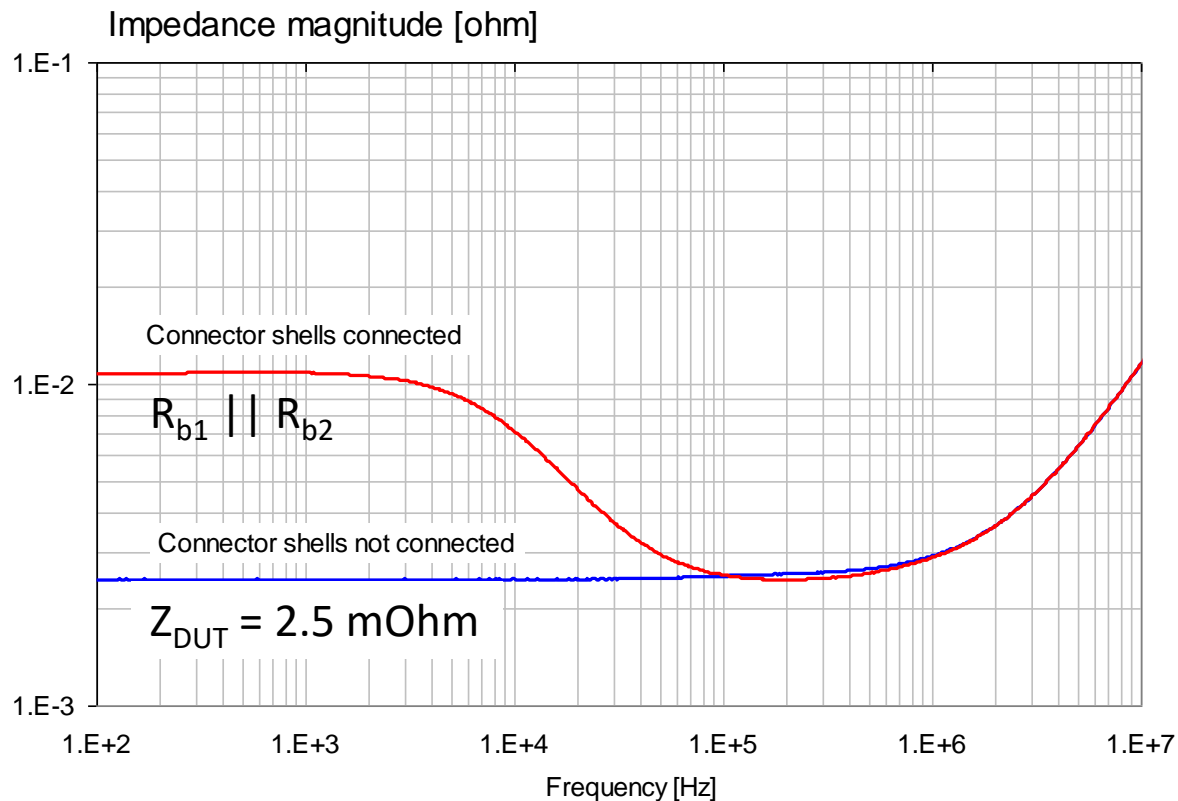
The Solution: Two-port Shunt-through Connection



$$Z_{DUT} = \frac{50}{2} \frac{S_{21}}{1 - S_{21}}$$

- VNA Two-port Shunt-Through connection (RF Kelvin)
- First connection injects test current
- Second connection picks up voltage across DUT

But There is a New Problem



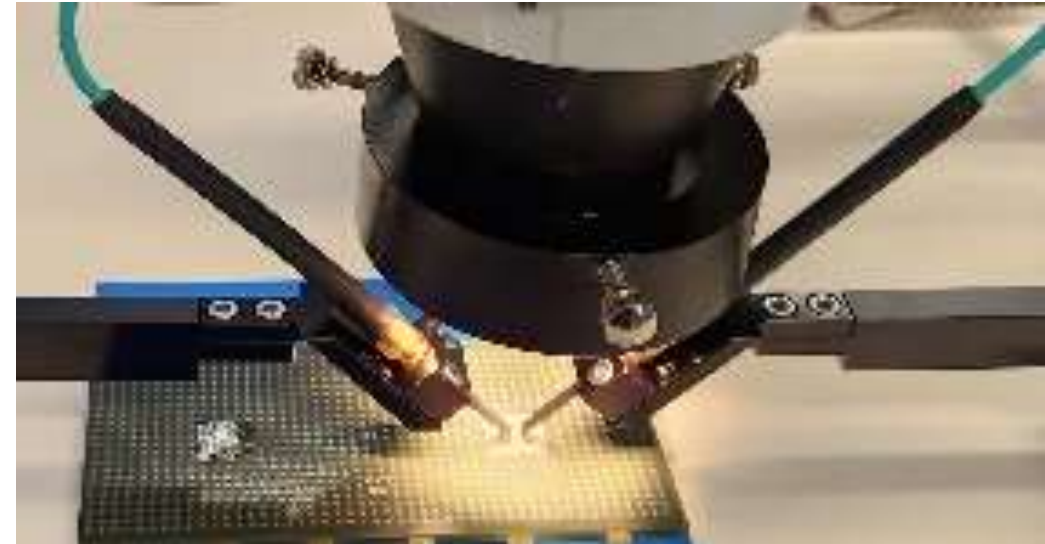
We measure the cable braid resistance instead of the DUT!

Can We Calibrate Out the Braid Error?

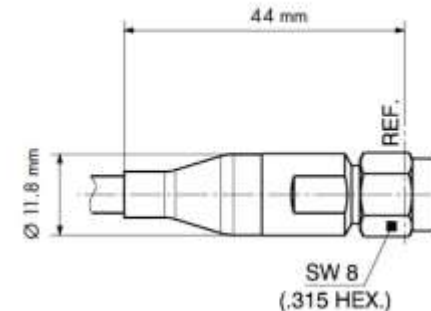


The short answer is **NO**

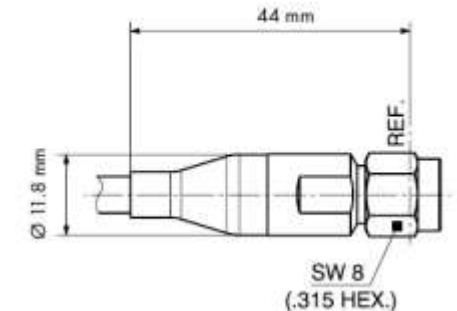
- No calibration method is available for it (though we could create it)
- The 'braid' error is not constant
 - It is the sum of resistances all along the return path, including the connectors and/or probes
 - The error will likely vary with cable/connector movement



SMA male (SF_11_SMA-501)

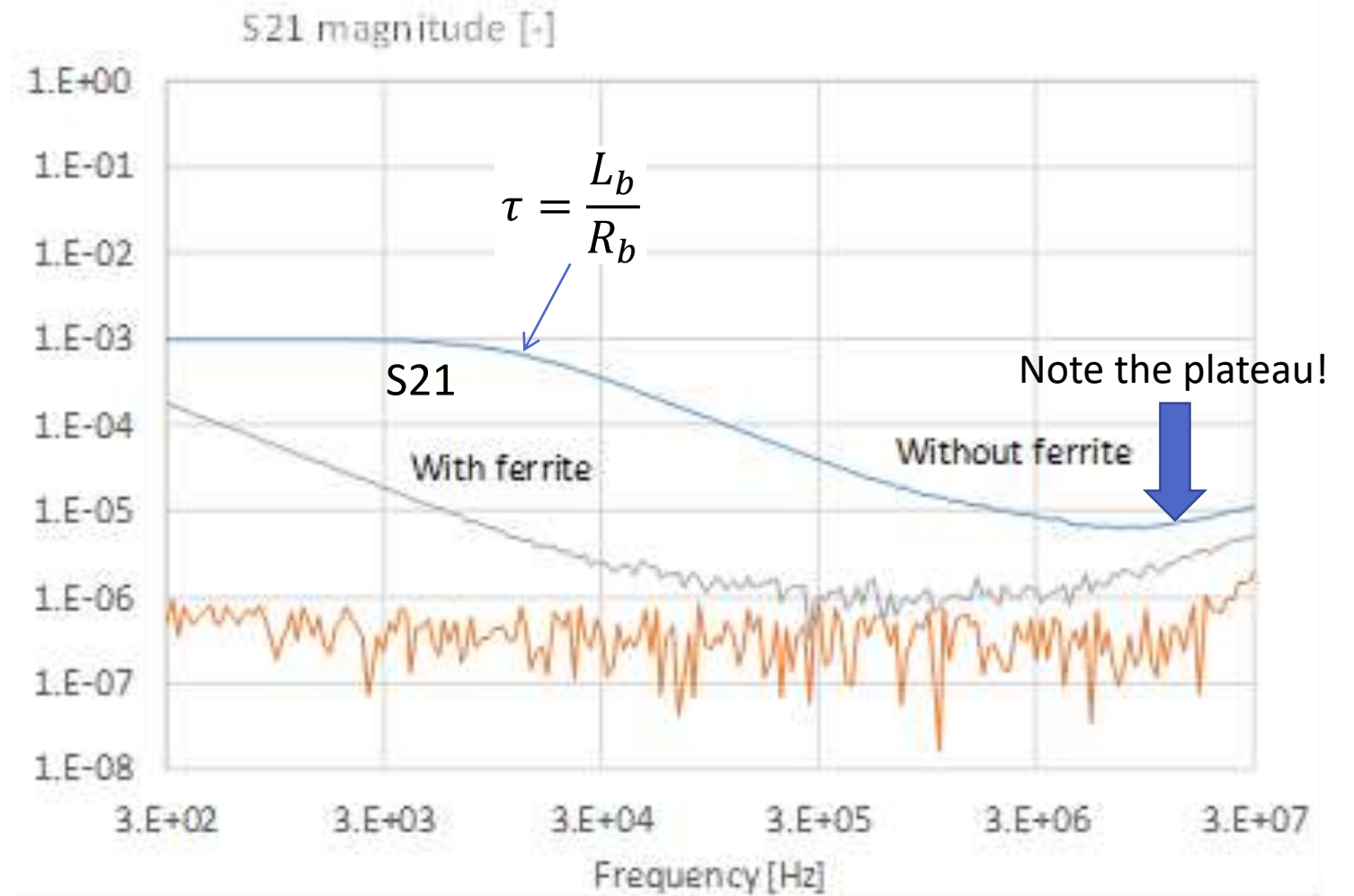


3.5 mm male (SF_11_PC35-501)



What Can We Do?

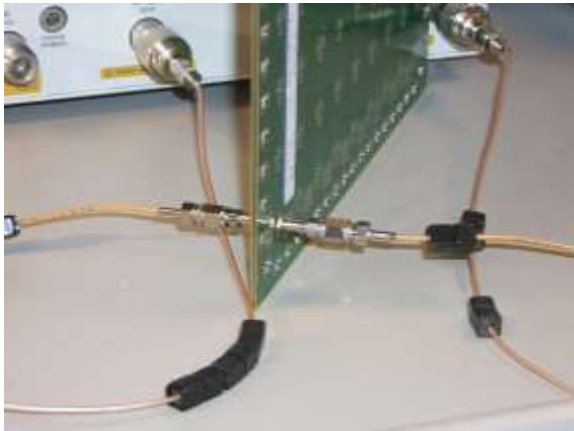
- We need to open up the cable-braid loop
- One option: use a common-mode choke to increase τ



Common-mode Choke Options



We need to open up the cable-braid loop
A popular option: make use of common-mode inductance



Measuring Milliohms and PicoHenrys
in Power Distribution Networks,
DesignCon 2000



Accuracy Improvements of PDN
Impedance Measurements in the Low
to Middle Frequency Range, DesignCon
2010



Overview of Frequency-Domain
Power-Distribution Measurements,
DesignCon East 2003



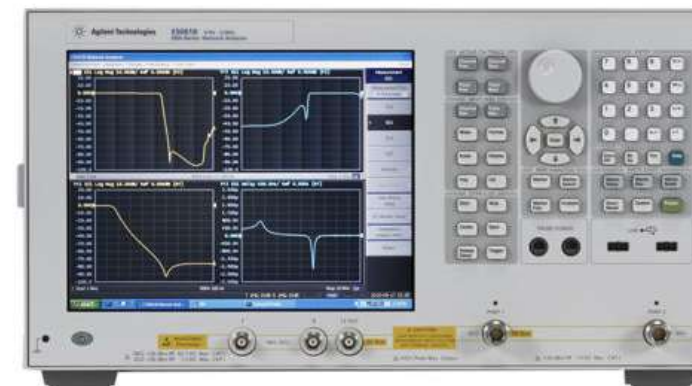
Picotest J2102B



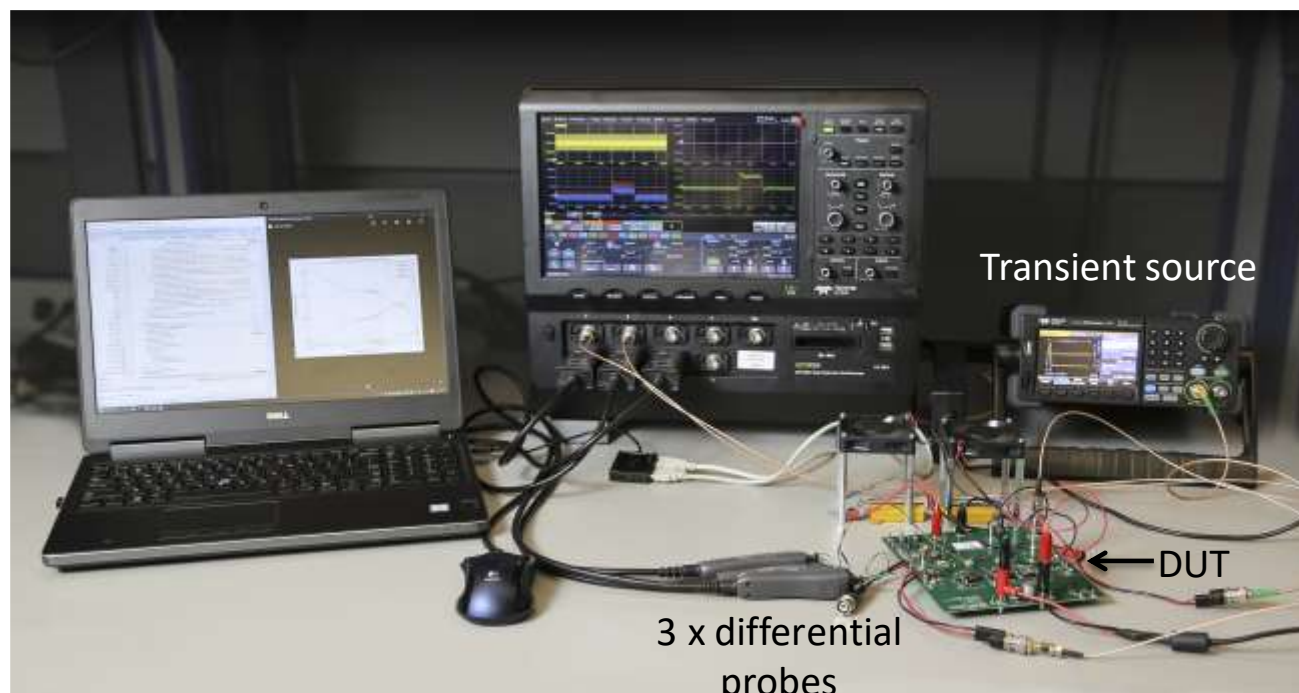
Home-made
common-mode
choke

Some Other Options

- Floating or semi-floating connections
- Differential amplifiers
- Current booster amplifiers



Keysight E5061B – 3LO



Transient source

DUT

3 x differential probes

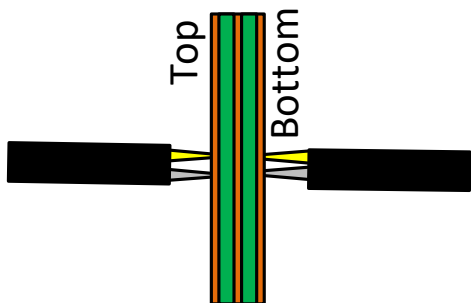
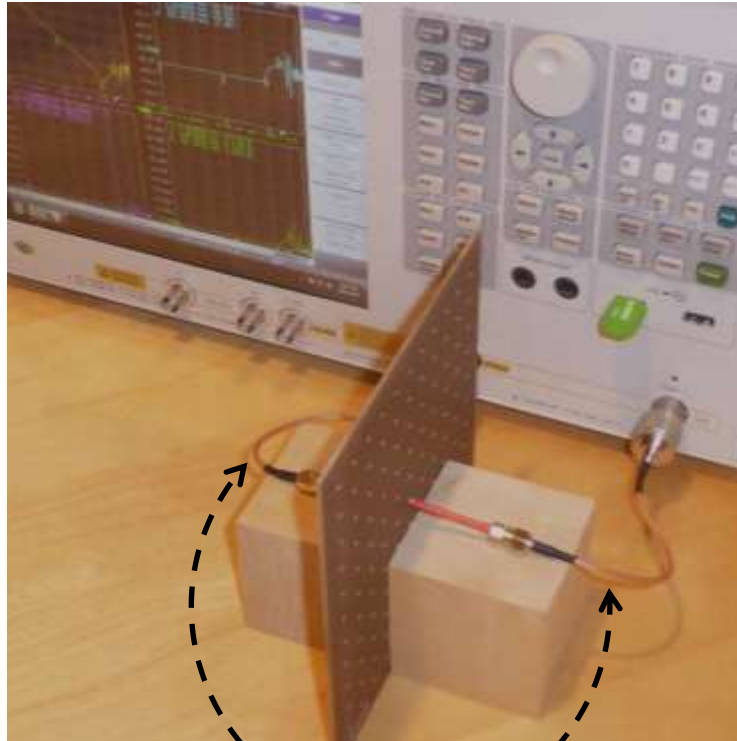


Picotest J2113A amplifier

“A Generic Test Tool for Power Distribution Networks,” Designcon 2017

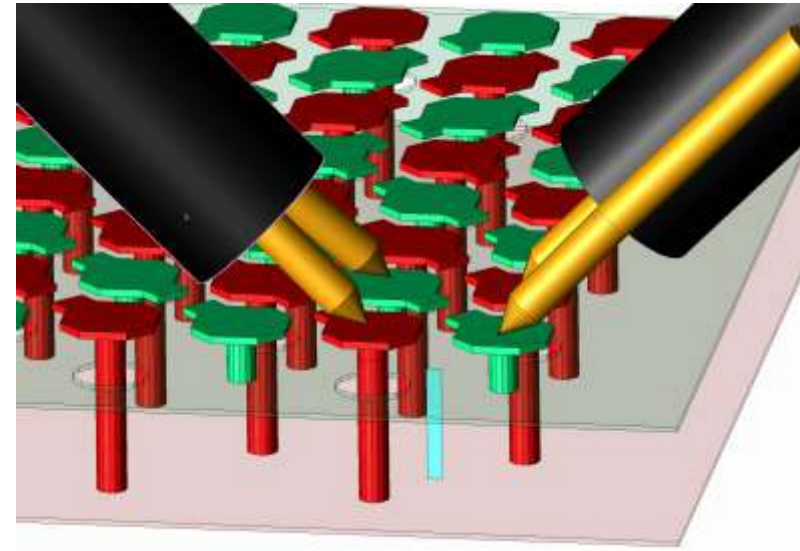
http://www.electrical-integrity.com/Quietpower_files/QuietPower-48.pdf

Two-sided vs. One-sided Connections



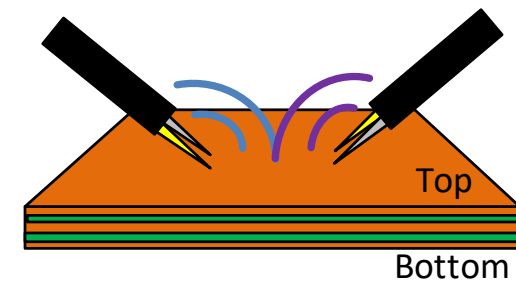
Coupling is minimized

- Cable-to-cable
- Probe-to-probe
- Via-to-via



If two-sided connection is not possible

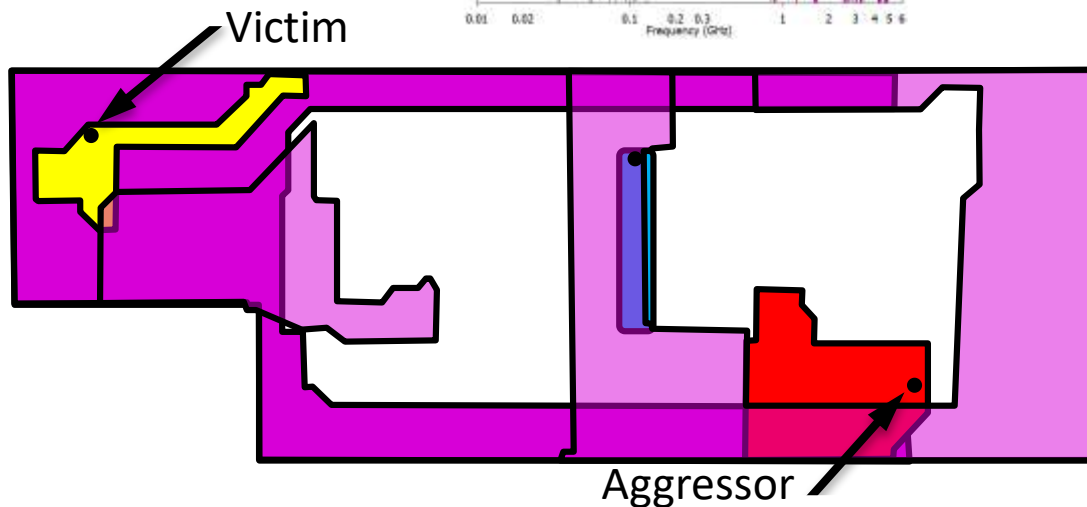
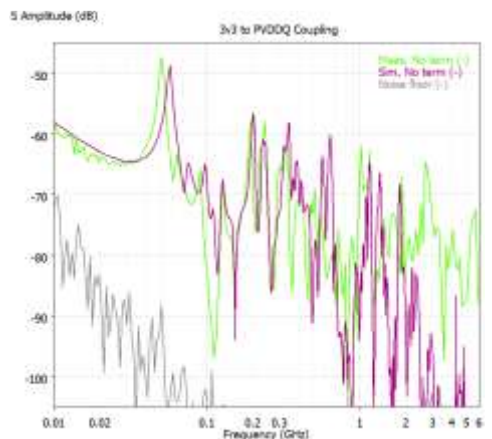
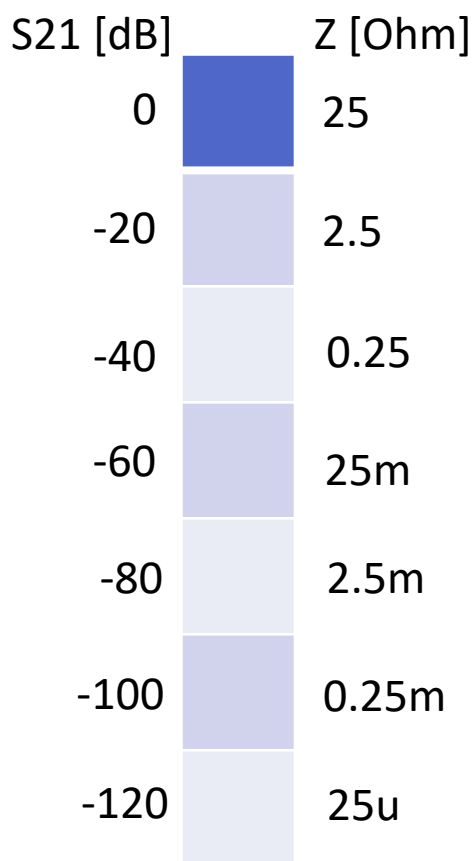
- Use nearby via pairs
- Coupling in probe loops and via loops is present



What Dynamic Range Do We Need?



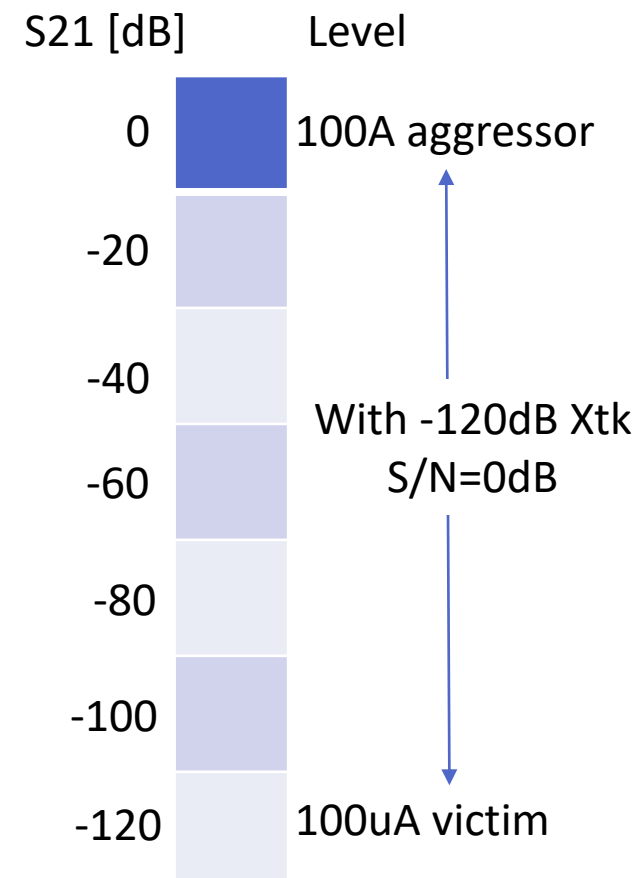
Self impedance



20" production board with multiple power rails

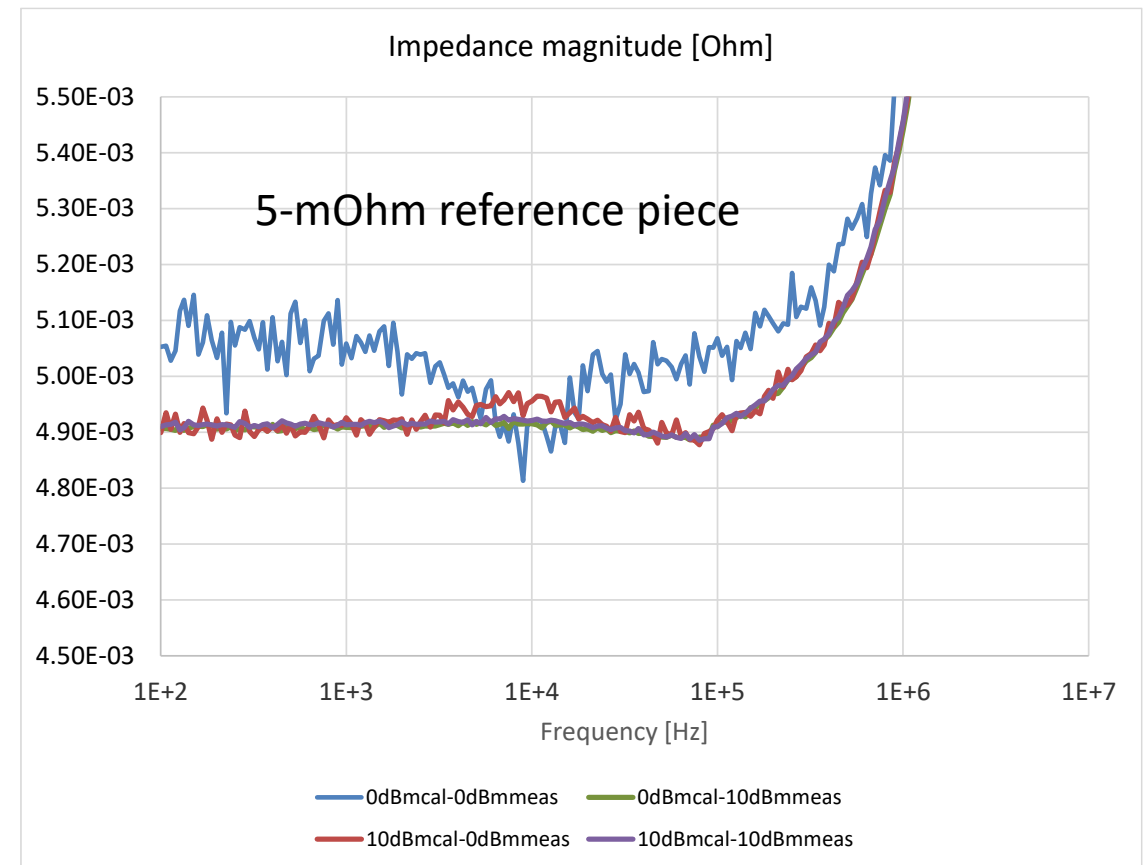
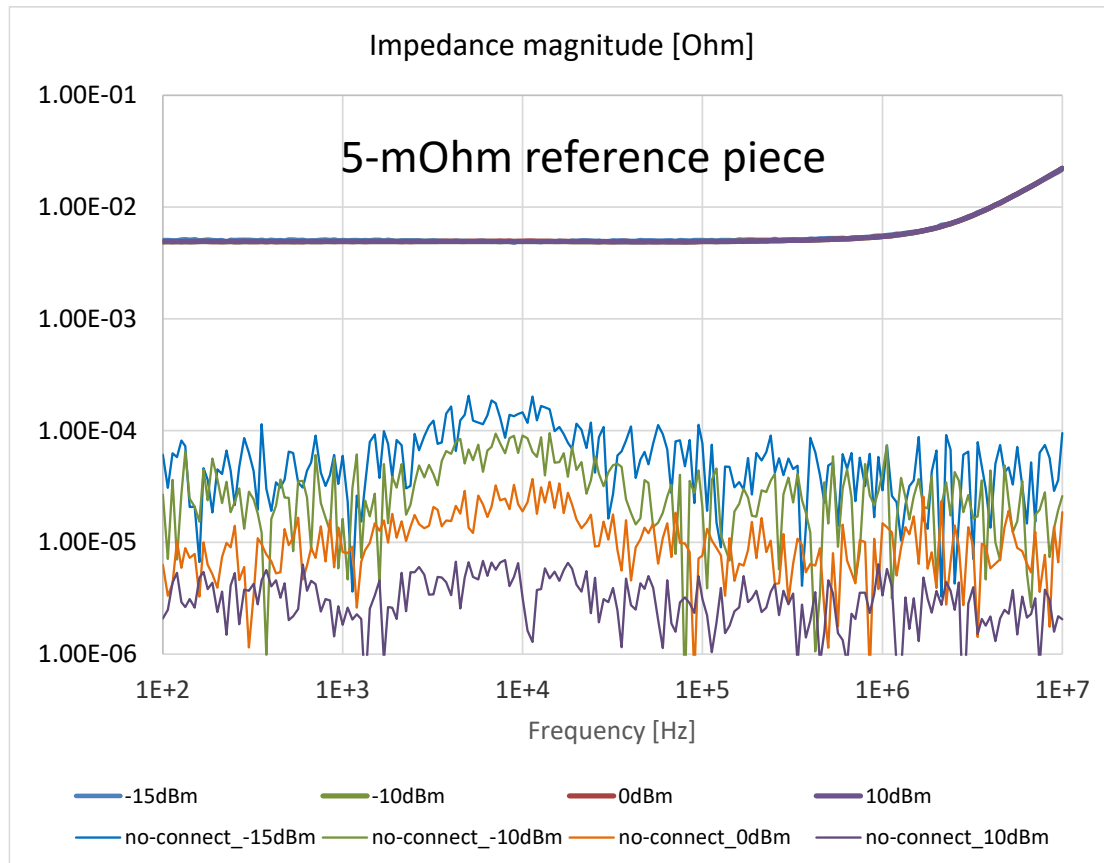
Long-Haul Inter-Domain Power Noise, DesignCon 2022

SI-PI transfer impedance



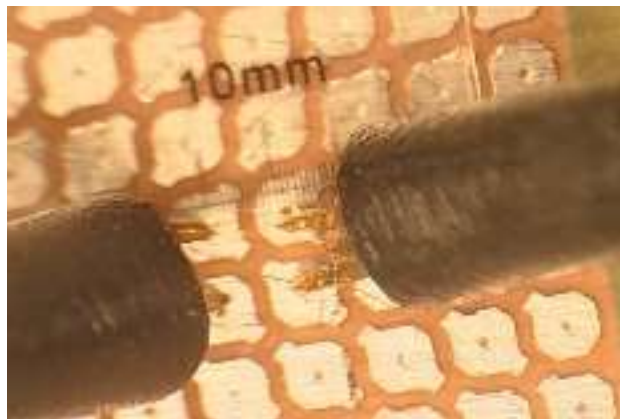
What Dynamic Range Can We Achieve?

- With VNA only: 120 ... 140dB
- With current booster: 140 ... 160 dB

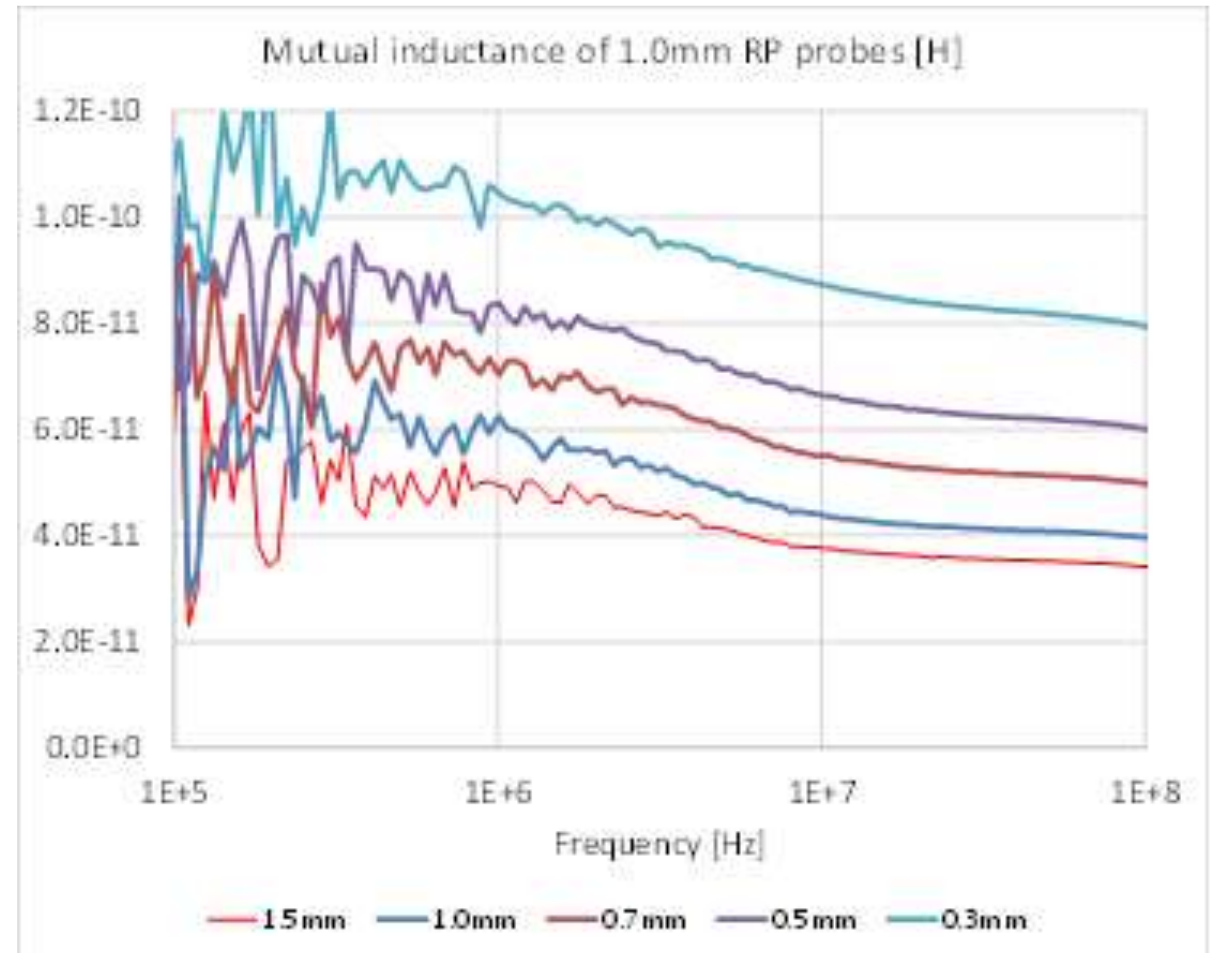


New Challenges

Wafer-probe (and via) crosstalk calibration/deembedding and coupling



3D Connection Artifacts in PDN Measurements, DesignCon 2023



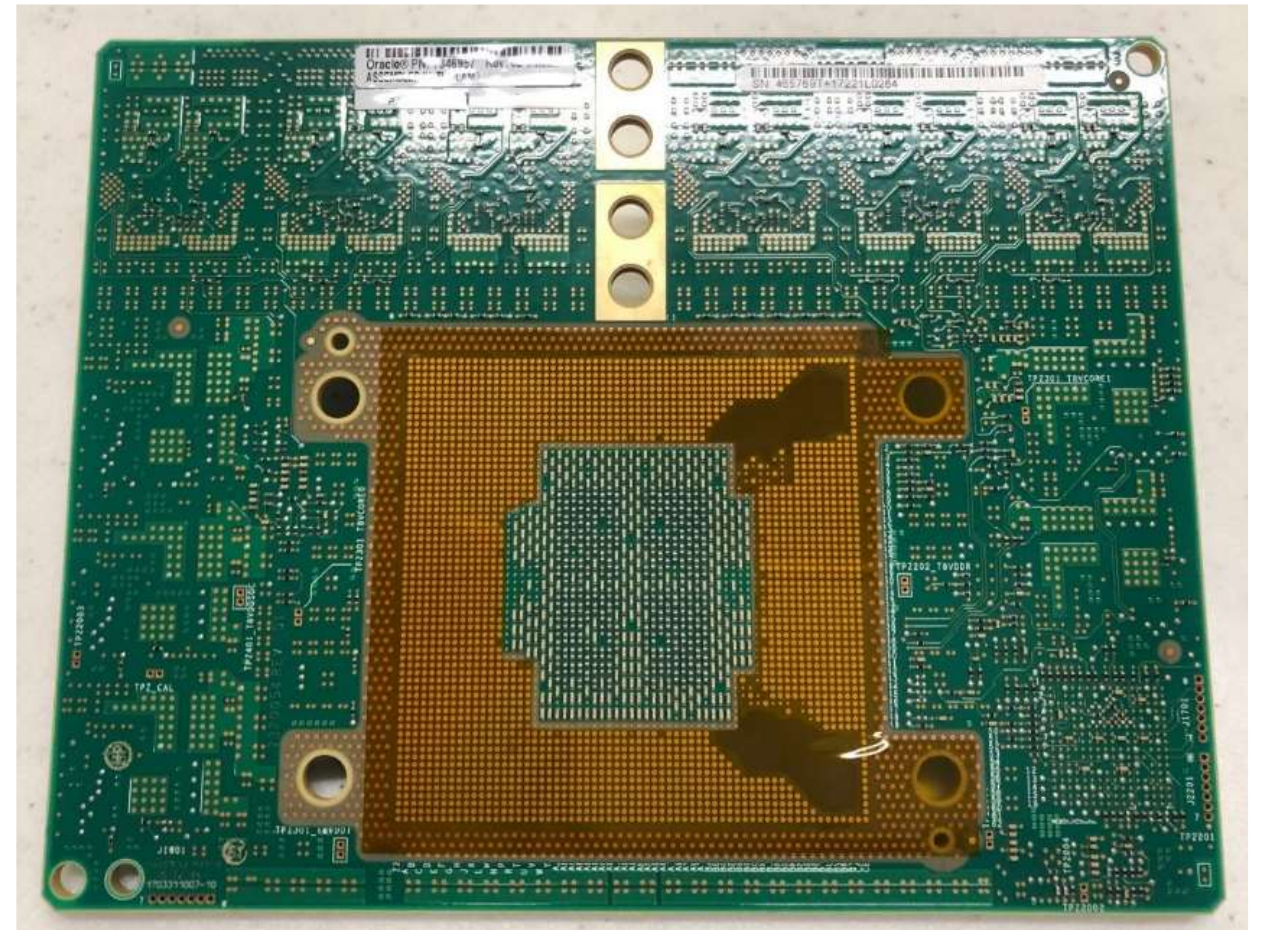
3D Connection Artifacts in PDN Measurements, DesignCon 2023

New Challenges



Large currents through large arrays

- Horizontal connections cant be ignored
- Packages are growing beyond 70x70mm
- One square of (unperforated) copper sheet has approximately 0.6 mOm sheet resistance
- With $< 1\text{mOhm}$ target impedance, the impedance is strongly location dependent
- Challenge for simulations
- Challenge for measurements



Is Power Integrity the New Black Magic?, Cadence E-Learning Forum, 2021

IEEE Pkg Benchmarks

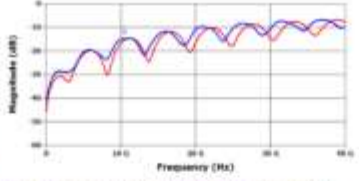



IEEE Electronics Packaging Society (EPS) Technical Committee on Electrical Design, Modeling and Simulation (TC-EDMS)

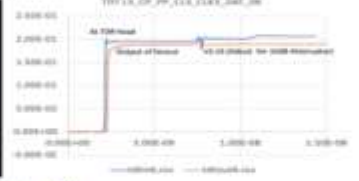

- Users and CAD companies need to work together to create correlation cases that are
 - Open source
 - Verified
- Good example: IEEE Packaging Benchmark project

<https://packaging-benchmarks.org/repository/>

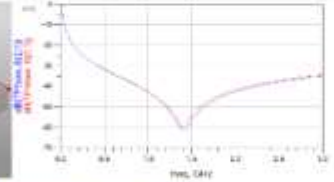
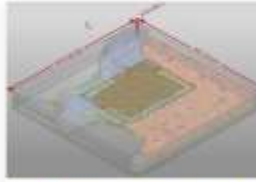
Packaging Benchmarks



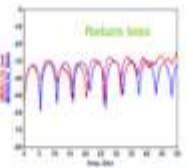
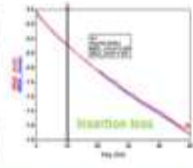

I. Single-ended Microstrip Transmission Line (version 1.0)
Single-ended Microstrip Transmission Line Benchmark Problem



II. Plasma Package (version 1.0)
Plasma Package Benchmark Problem



III. Power-Integrity Test Package (version 1.0)
Package Power Integrity Benchmarking Problem



IV. PCB Laminate Parameter Extraction for Simulation (version 1.0)
PCB Laminate Parameter Extraction for Simulation Benchmark Problem

Good Measurement Practices



- Select the instruments, cables, probes and calibration methods carefully
- Be aware of uncertainty factors and limitations
- Maximize source power, minimize IFBW and number of sweep points for very low impedances
- Connections matter at any frequencies
- Keep 'golden,' well-characterized reference pieces on hand
- Check the test setup periodically with the 'golden' pieces
- Be aware of probe and via coupling artifacts
- Correlate as much as possible

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