DesignCon 2023 Preview

Scott McMorrow, Steve Krooswyk, Rich Mellitz,
Istvan Novak & Robert Branson | Samtec, Inc.

Technical Sessions & Panels

- Panel – PCIe® 6.0: Challenges of achieving 64GT/s with PAM4 in lossy, HVM channels
- A novel approach to 224 Gb/s Reference Receiver design using Raised Cosine Response for noise mitigation
- Panel – What users need from Power Integrity Simulators
- 3D Connection Artifacts in PDN measurements
- Cascaded vs. End-to-End Multi-Pin Interconnect Simulation Models

PCIe® 6.0: Achieving Stable 64GT/s PAM4 Lossy Channel Links within HVM

Tuesday, January 31st, 4:45 pm

Track: 06. System Co-Design: Modeling, Simulation & Measurement Validation

Panel Discussion:

- PCIe 6.0 doubles throughput from 5.0 devices through PAM4 modulation
- New signaling modulation has led to reduced loss and noise budgets, ushering in a new set of system and IC challenges
- Our panel of domain experts enable us to cover the challenges and solutions from die-to-die, and from concept design to test and measurement

Panel Preview: PCIe 6.0: Achieving Stable 64GT/s PAM4 Lossy Channel Links within HVM (Tuesday 4:45 pm)

Panelists:

Pegah Alavi | Sr. Solutions Engineer, Keysight Technologies

Pegah is a Senior Applications Engineer at Keysight Technologies, where she focuses on Signal Integrity and High-Speed Digital Systems and Applications. Prior to joining Keysight Technologies, Pegah worked on system level modeling of analog and mixed signal circuits in order to best predict the overall systems performance and accurately represent each component.

Tim Wig | Signal Integrity Engineer, Intel Corporation

Tim Wig joined Intel in 2001, where he works as a signal integrity engineer in a pathfinding and spec development group whose charter includes PCIe and other interconnect standards. Tim coordinates the Card ElectroMechanical (CEM) Spec document for Gen 4.0 and 5.0, and has contributed many of the signal integrity enablers that allowed PCIe to reach 16 and 32 GT/s. His primary focus is passive component, PCB, and channel level modeling, measurement, and optimization for PCIe CEM, though he also supports the M.2, U.2, and OCuLink standards. He holds a PhD in Engineering Science from Washington State University; and and a MS and BS in Electrical Engineering and a BS in Engineering Physics from the University of North Dakota. He delivered a tutorial on PCIe Gen 4.0 to DevCon 2016.

Steve Krooswyk | Sr. Signal Integrity Engineer, Samtec

Steve is involved in new high-speed connector development and PCIe standards at Samtec. His 16 years of signal integrity experience has had a focus on the design, simulation, and correlation of PCIe interconnect and I/O. Previously, Steve was the PCIe tech lead for SI in Intel's data center division during Gen3 and Gen4 development. He is an author of the book High Speed Digital Design: Design of High-Speed Interconnects and Signaling and holds a MS degree from the University of South Carolina.

Panel Preview: PCIe 6.0: Achieving Stable 64GT/s PAM4 Lossy Channel Links within HVM (Tuesday 4:45 pm)

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Panelists:

Rick Eads | Principal PCIe Program Manager, Keysight

Rick Eads is a principal program manager at Keysight Technologies with expertise in technical/industrial marketing of test and measurement tools and electronic design automation software in the computer, semi-conductor, communications, and storage industries worldwide. Rick's specialty is precision product and solution definition. He provides technical leadership in driving standards within industry organizations for PCI Express, CCIX, GenZ, OCP, NVM Express, CEI 4.0, IEEE 802.3, Express Card, DDR, SATA, and InfiniBand. He markets test and measurement products covering oscilloscopes and associated compliance software tools, vector network analyzers, bit error ratio testers (BERTs) and EDA tools. Rick earned an MBA from the University of Colorado and holds a BSEE from Brigham Young University with an emphasis on digital design and computer architecture. Rick actively contributes to the development of the PCIe physical layer BASE, CEM, and Test specifications and has led electrical Gold Suite testing at PCI-SIG workshops worldwide since 2004.

David Bouse | PCIe Principal Technology Lead, Tektronix

David Bouse is the PCI Express Principal Technology Lead at Tektronix and has been heavily involved in PCIe Physical layer pathfinding and specification development within the PCI-SIG. His areas of focus include transmitter and receiver test methodology, test fixture design, and waveform post-processing algorithms for NRZ & PAM4. David is an active participant in the Electrical Work Group and Serial Enabling Group where he helps accelerate the pace of technology development and adoption across multiple market segments.

Madhumita Sanyal | Sr. Staff Technical Marketing Manger, Synopsys Inc.

Madhumita Sanyal is a Senior Staff Technical Marketing Manager for Synopsys' high-speed SerDes PHY IP portfolio. She has over 16 years of experience in design and application of ASIC WLAN products, logic libraries, embedded memories, and mixed-signal IP. Madhumita holds a Master of Science degree in Electrical Engineering from San Jose State University and LEAD from Stanford Graduate School of Business.

Panel Preview: PCIe 6.0: Achieving Stable 64GT/s PAM4 Lossy Channel Links within HVM (Tuesday 4:45 pm)

Expected Panel Focus:

- Equalization schemes
- Channel difference across data rate
- Channel simulation and correlation methodology
- I\O modeling with IBIS-AMI
- CEM form factor and critical layout updates
- New CEM power connector
- Requirements for TX compliance
- Rx jitter tolerance considerations
- New SNDR specifications
- Changes to cable and connector SI requirements
- Cable and connector fixture design & measurement

A Novel Approach to 224 Gb/s Reference Receiver Design Using Raised Cosine Response for Noise Mitigation

Richard Mellitz | Samtec, Inc.

A Novel Approach to 224 Gb/s Reference Receiver Design Using Raised Cosine Response for Noise Mitigation

Authors

Luis Boluna (Keysight), **John Calvin** (Keysight), **Francesco de Paulis** (University of L'Aquila), **Richard Mellitz** (Samtec), **Rick Rabinovich** (Keysight), **Mike Resso** (Keysight)

February 1, 2:00 PM – 2:45 PM Ballroom G, Track 7, 9

Speakers

Francesco de Paulis

Research Professor at
University of L'Aquila

Mike Resso

Signal Integrity Applications Scientist
at Keysight Technologies

Preview:

A Novel Approach to 224 Gb/s Reference Receiver Design Using Raised Cosine Response for Noise Mitigation

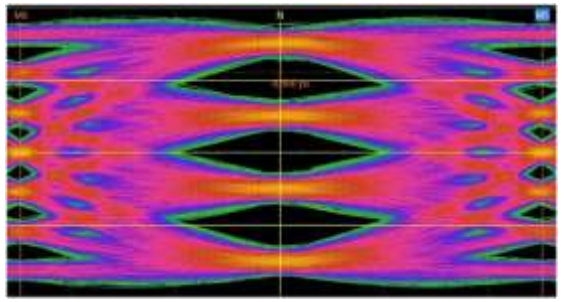
- The key term here is “Novel”
  - The intent is showing new ideas and stimulate questions for new research and development
- The Raise Cosine Filter is in essence an anti-aliasing filter
  - i.e., What to do about frequency content above the Nyquist rate
- Content include:
  - Non-symbol rate based Raised Cosine theory
  - Measurements performed
  - How COM computations were used with measurement instruments
  - Performance improvement of a very clean 224 Gb/s PAM4 channel
  - Extrapolate performance improvement for product with realistic noise and impairments

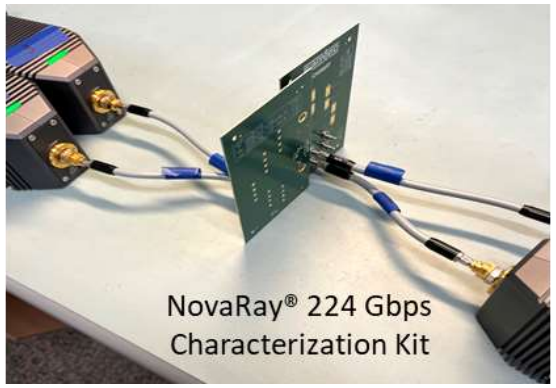
Common Questions:

- What are salient features of the non-symbol rate based Raised Cosine Filter?
- Can this be implemented in an actual receiver?
- Are their issues with too much bandwidth?

Content: Setting the Stage

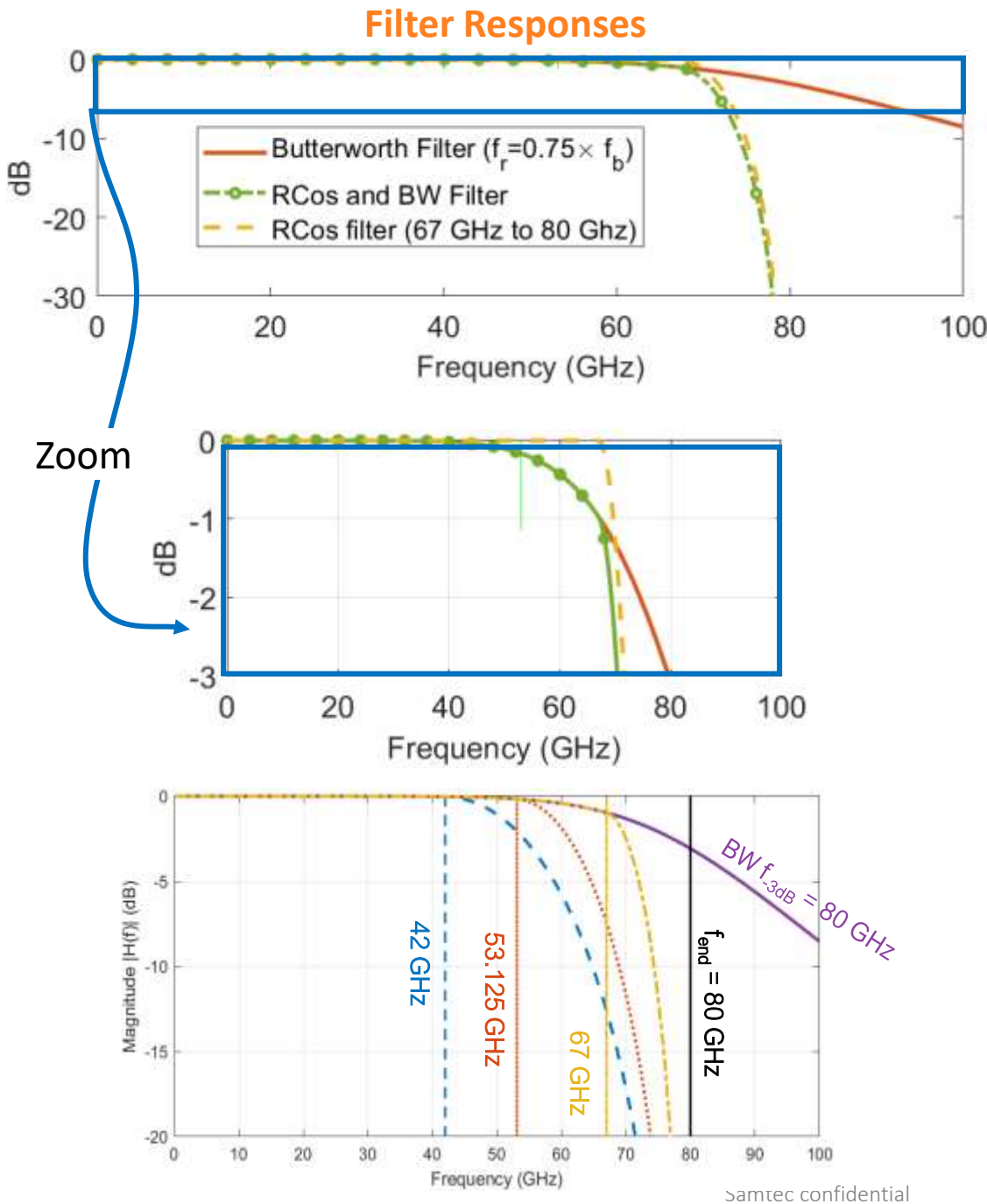
- COM computation, VEC, and EH review
- NovaRay® 224 Gbps Characterization Kit test setup
- Determine measurement Parameters which align COM and Keysight 120 GBd Bert and 100 G DCA
- Explain the process where COM is supplied with pulse response data from the DCA determines the variable filter setting
  - i.e., COM without supplying s-parameters





Non-Symbol Rate Based Raise Cosine (RCOS) Filter Experiment and Results

- The experiment is to look at Voltage Eye Closure (VEC) and Eye Height (EH) changes
- With and without the RCOS filter
- Sweeping start RCOS start frequency
- Addition on varying amounts of noise
- **Note: T**he DCA can implement the RCOS filter



What Users Need from Power Integrity Simulators

Panel Discussion

Wednesday, February 1st, 2023, 4:00 PM

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What Users Need from Power Integrity Simulators

Panel discussion, Wednesday, February 1st, 2023, 4pm

Power distribution keeps getting more and more demanding in a lot of electronic designs and the pre- and post-layout PI simulations are becoming an integral part of the design and validation processes. This panel brings together PI tool users from various OEMs with decades of design experience so that they can summarize and discuss the state of the PI simulation tools the way how they have experienced it and lay out the user needs for additional features and capabilities. A follow-up panel will be devoted to the emerging approaches and solutions offered by CAD companies.

Eric Bogatin | Professor, University of Colorado, Boulder | eric.bogatin@colorado.edu

Dr. Eric Bogatin is currently a Fellow with Teledyne LeCroy and a Professor at the University of Colorado, Boulder in the ECEE dept. He is also the Technical Editor of the Signal Integrity Journal. He received his BS degree in physics from MIT in 1976, and MS and PhD degrees in physics from the University of Arizona in Tucson in 1980. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansys, and Interconnect Devices. Eric has written 17 books on technical topics such as signal integrity and interconnect design and electronics for makers and over 600 papers and columns. Additional information can be found on his faculty web site: https://www.colorado.edu/faculty/bogatin/

Ethan Koether | Sr. Signal Integrity and Power Integrity Engineer, Amazon Project Kuiper | koether@amazon.com

Ethan Koether earned his master's degree in Electrical Engineering and Computer Science in 2014 from the Massachusetts Institute of Technology and has spent the last seven years as a hardware engineer at Oracle. He recently began his new role as a Power Integrity Engineer with Amazon's Project Kuiper. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

What Users Need from Power Integrity Simulators

Istvan Novak | **Principal Signal and Power Integrity Engineer, Samtec** | **istvan.novak@samtec.com**

Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25 µm power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-nine patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website. Istvan was named Engineer of the Year at DesignCon 2020.

Pete J. Pupalaikis | **Founding Member and Director of Signal Integrity, Nubis Communications**
pete.pupalaikis@nubis-communications.com

Peter J. Pupalaikis is a founding member of Nubis Communications, an optical communications startup, and is Director of Signal Integrity. Prior to Nubis, he worked for 25 years at Teledyne LeCroy where he was Vice President,Technology Development. He served in the United States Army before obtaining a BSEE from Rutgers University in 1988. Mr. Pupalaikis holds fifty-three patents in the area of measurement instrument design and is author of the textbook, "S-Parameters for Signal Integrity" published by Cambridge University Press in 2020. In 2013 he was elevated to IEEE fellow for contributions to high-speed waveform digitizing instruments.

Steve M. Sandler | **Founder, PICOTEST** | **steve@picotest.com**

Steve Sandler has been involved with power system engineering for more than 40 years. Steve is the founder of PICOTEST.com, a company specializing in power integrity solutions including measurement products, services and training. He frequently lectures and leads workshops internationally on the topics of power, PDN and distributed systems and is a Keysight certified expert for EDA software. Steve frequently writes articles and books related to power supply and PDN performance and his latest book, Power Integrity Using ADS was published by Faraday Press in 2019. Steve founded AEi Systems, a well-established leader in worst case circuit analysis and troubleshooting of high reliability systems.

3D Connection Artifacts in PDN Measurements

Istvan Novak | Samtec, Inc.

3D Connection Artifacts in PDN Measurements

- Technical Paper, Thursday, February 2nd, 2023, 9AM
- Ethan Koether, Amazon Project Kuiper
- Kristoffer Skytte (Cadence), John Phillips (Cadence),
- Shirin Farrahi (Cadence), Abe Hartman (Oracle),
- Sammy Hindi (Ampere Computing), Mario Rotigni (STMicroelectronics)
- Gustavo Blando (Samtec), Istvan Novak (Samtec)

Connecting to a DUT with two probes best can be done at test-via pairs connecting from opposite sides of the DUT. Some DUTs do not have through-holes. Measuring impedance in large pin fields, where one or both sides of the supply rail uses only blind vias, have this limitation and requires same-side probing. When the two ports are in close proximity, the coupling between the probe tip loops can be deembedded or calibrated out based on its equivalent circuit. Calibrating to the tips of probes may remove the probe-tip coupling error but leaves the effect of coupling between the DUT via-trace structures. It must also be noted that deembedding requires full two-port S parameters, which means we use inaccurate, measured S11/S22.

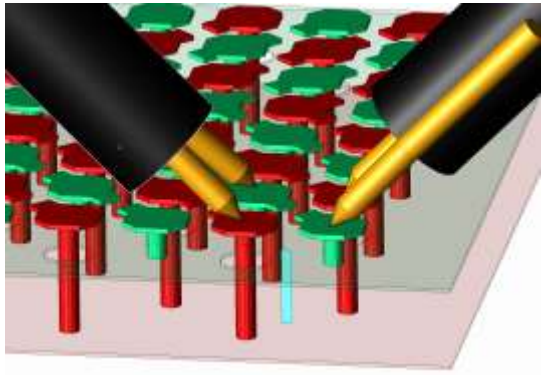
In this paper we will analyze via and trace coupling effects using hybrid and full-wave solvers by deembedding/calibration utilizing multiple test-boards. More sophisticated DUT boards will also be used to look at the parasitic probe-via coupling in two-port shunt-through self and transfer impedance PDN measurements.

3D Connection Artifacts in PDN Measurements

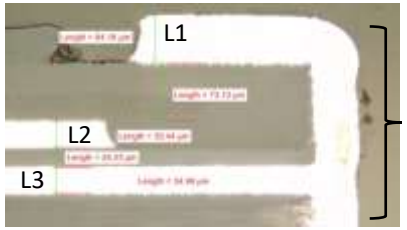
- Test board having 20 layers, 5 PWR-GND cavities
- Blind via arrays cut away from rest of board
- Via array has alternating checkered board PWR-GND pattern
- Entire area of array shorted for corresponding measurements

Test Board top-side view.

Blind via array under test.



Port landing configuration on via array with port location to which we de-embed DUT denoted in blue.



Test board stack up cross section.

Cascaded vs. End-to-End Multi-Pin Interconnect Simulation Models

Wednesday, February 2, 11:15 AM

Robert Branson | Samtec, Inc.

Cascaded vs. End-to-End Multi-Pin Interconnect Simulation Models

February 2, 2023 11:15 AM – 12:00 PM, Track 13

Authors

Robert Branson (Samtec), **Steve Krooswyk** (Samtec),
Scott McMorrow (Samtec), **Gustavo Blando** (Samtec)

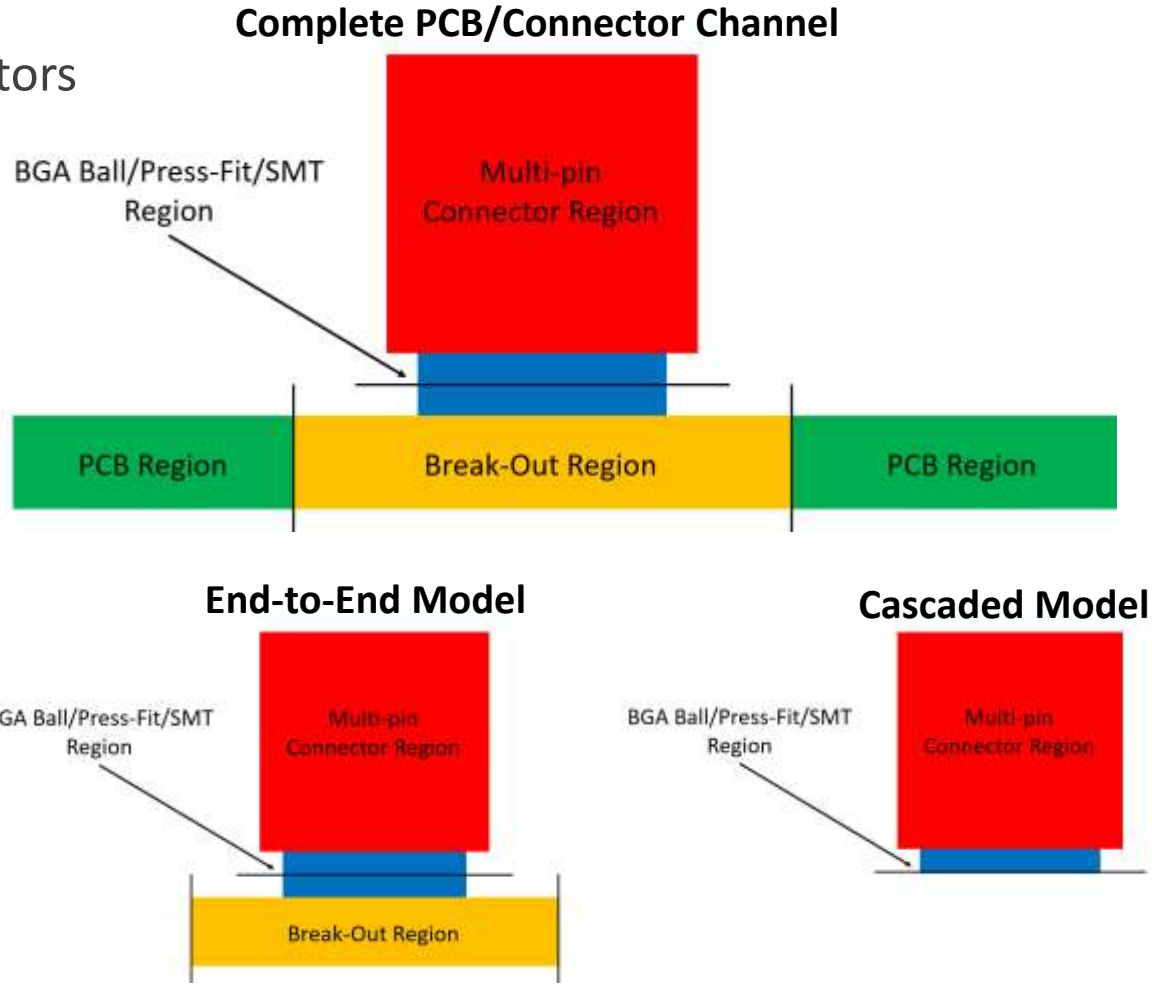
Speaker

Robert Branson
Signal Integrity Engineer (Samtec)

Preview:

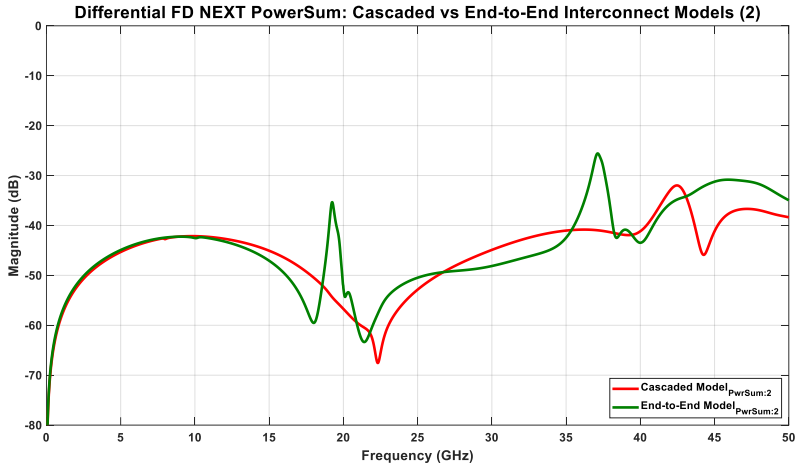
Cascaded vs. End-to-End Multi-Pin Interconnect Simulation Models

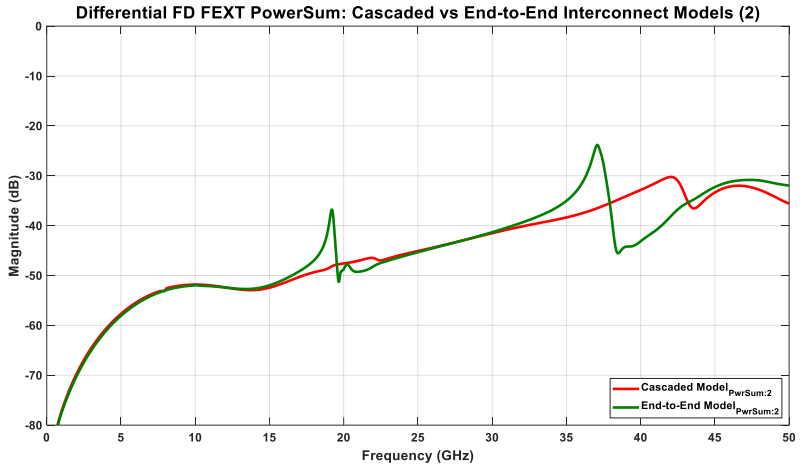
- How much to model must be considered when simulating connectors
- Cascaded Model:
  - Separately simulated PCB BOR and connector
- End-to-End Model:
  - One complete continuous simulation model
- Considerations for the decision:
  - Speed
  - Accuracy

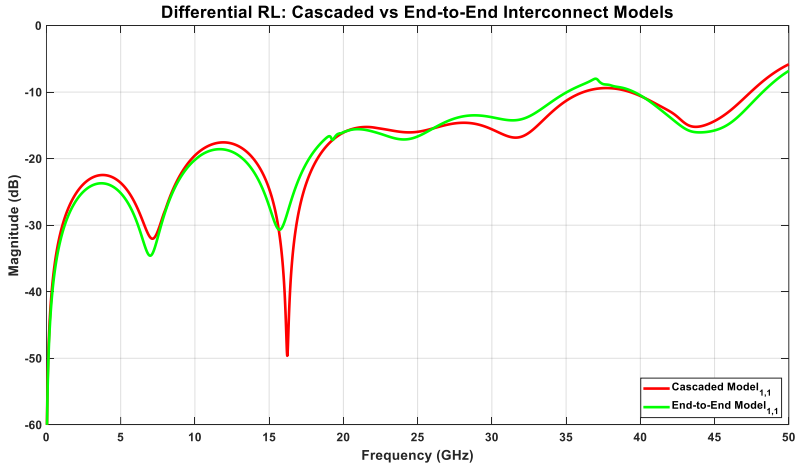


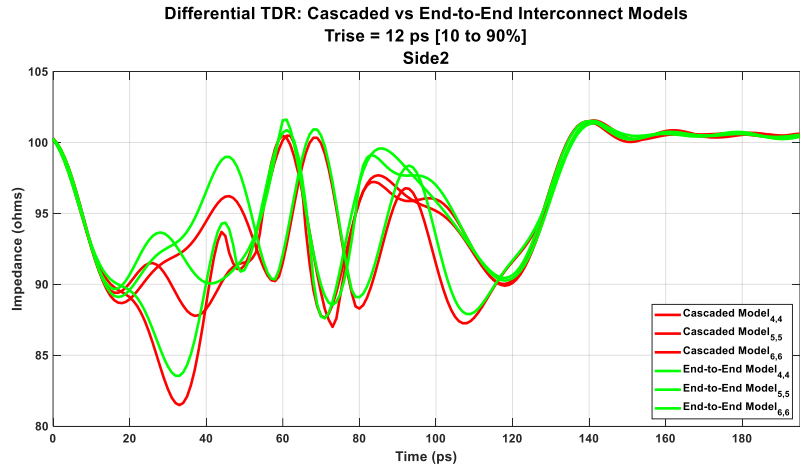
Content: Simulation Differences

- There are performance differences between simulation options
- These differences come about because the TEM assumptions are broken









Content: Exploration of Error and Alternatives

- The presentation will focus on exploring the causes of the differences between simulation options, as well as alternatives to the two main options
- Exploration of Cause:
  - Done using a generic and simplified connector model
  - Determine where the resonance occurs
  - Look at field plots to understand impact
- Alternatives
  - Multi-mode cascaded models
  - Intermittent solving

Common Questions:

- Is the behavior observed here consistent among different Resonance Sources?
- How much of a simulation time difference does Cascaded vs. End-to-End models make?

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BOOTH 939

Welcome Reception | Author Meet & Greet | Product Showcase

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