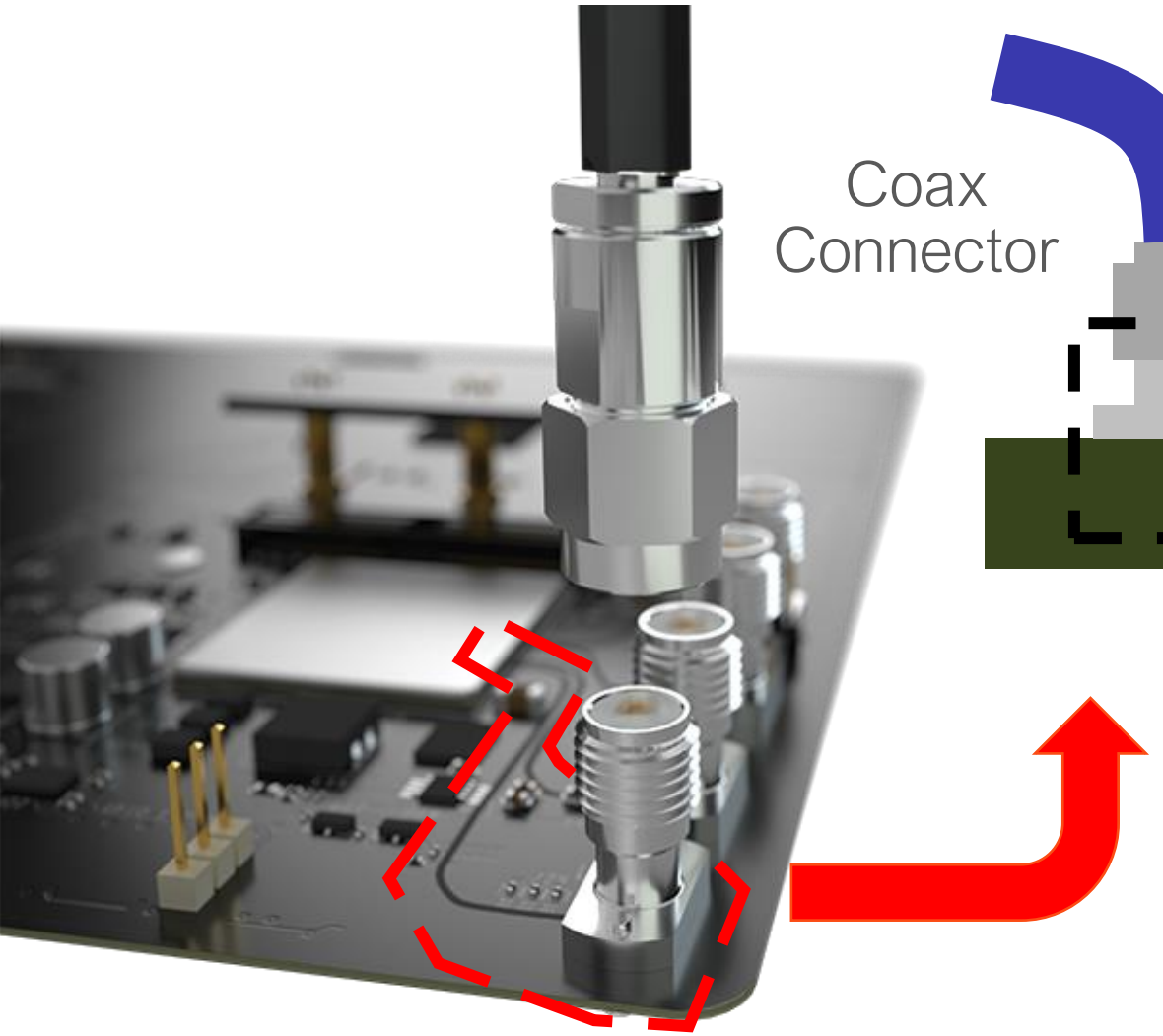
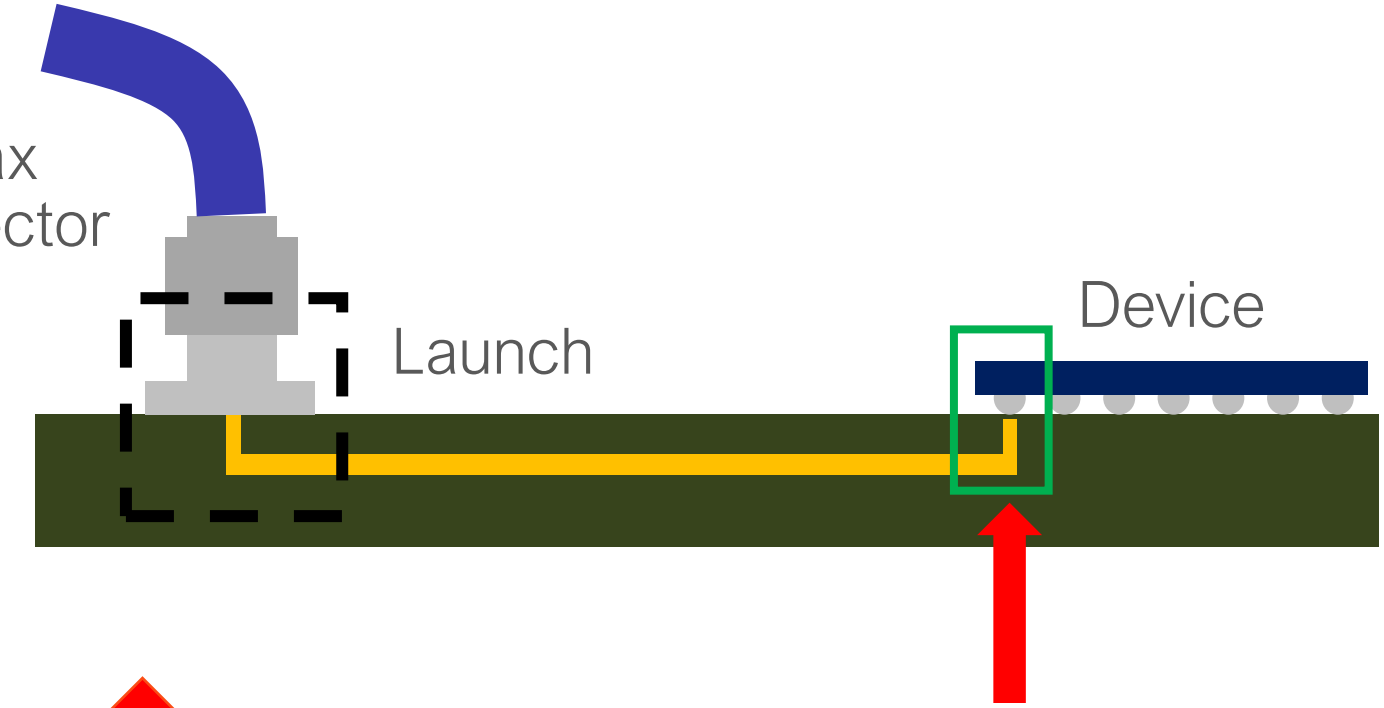
gEEk® spEEk

Precision RF Connector PCB Launches for 224 Gbps Devices

Sandeep Sankararaman

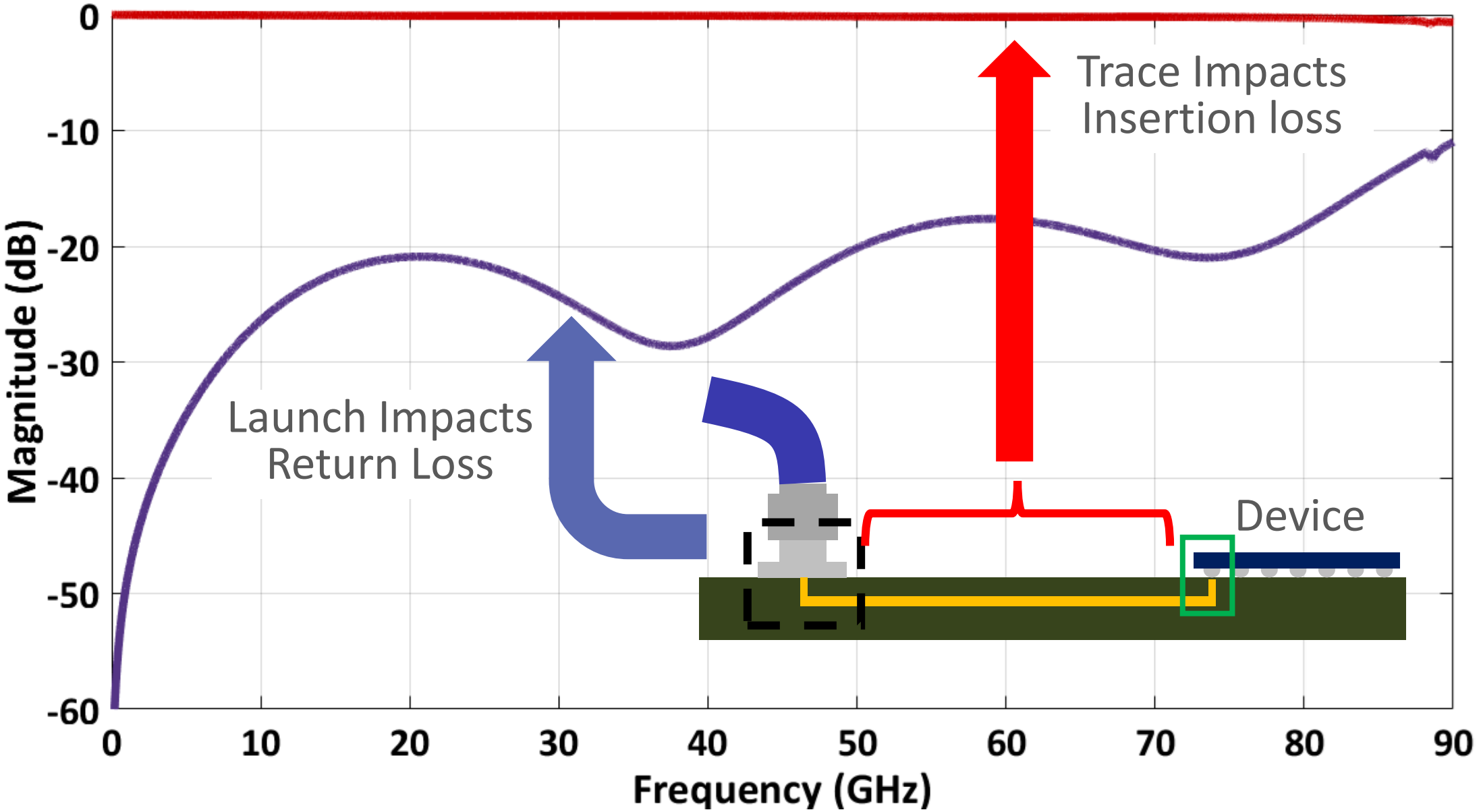
Why Launch Design Matters - Measuring a Device



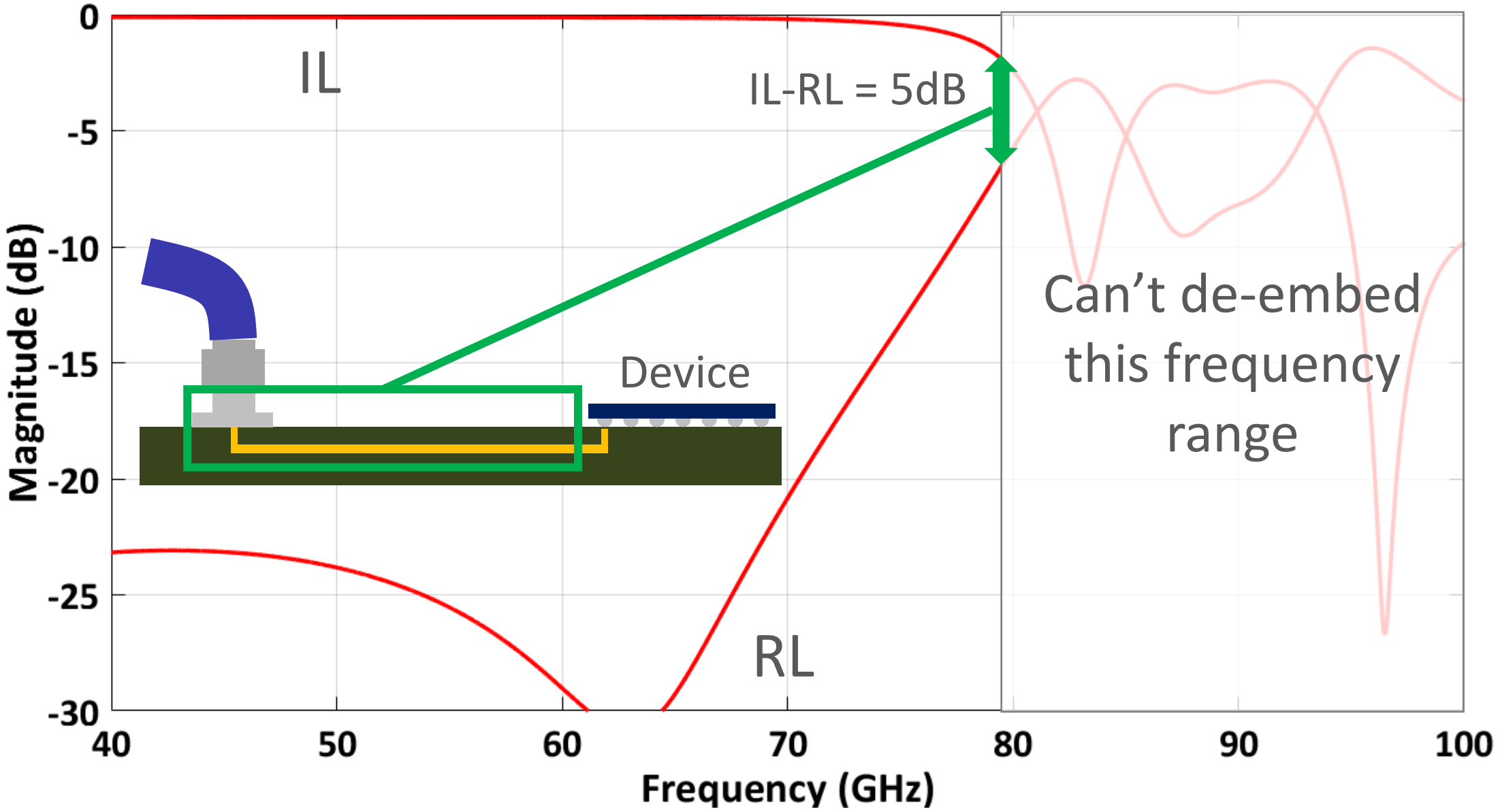


How do you isolate the performance of the device?

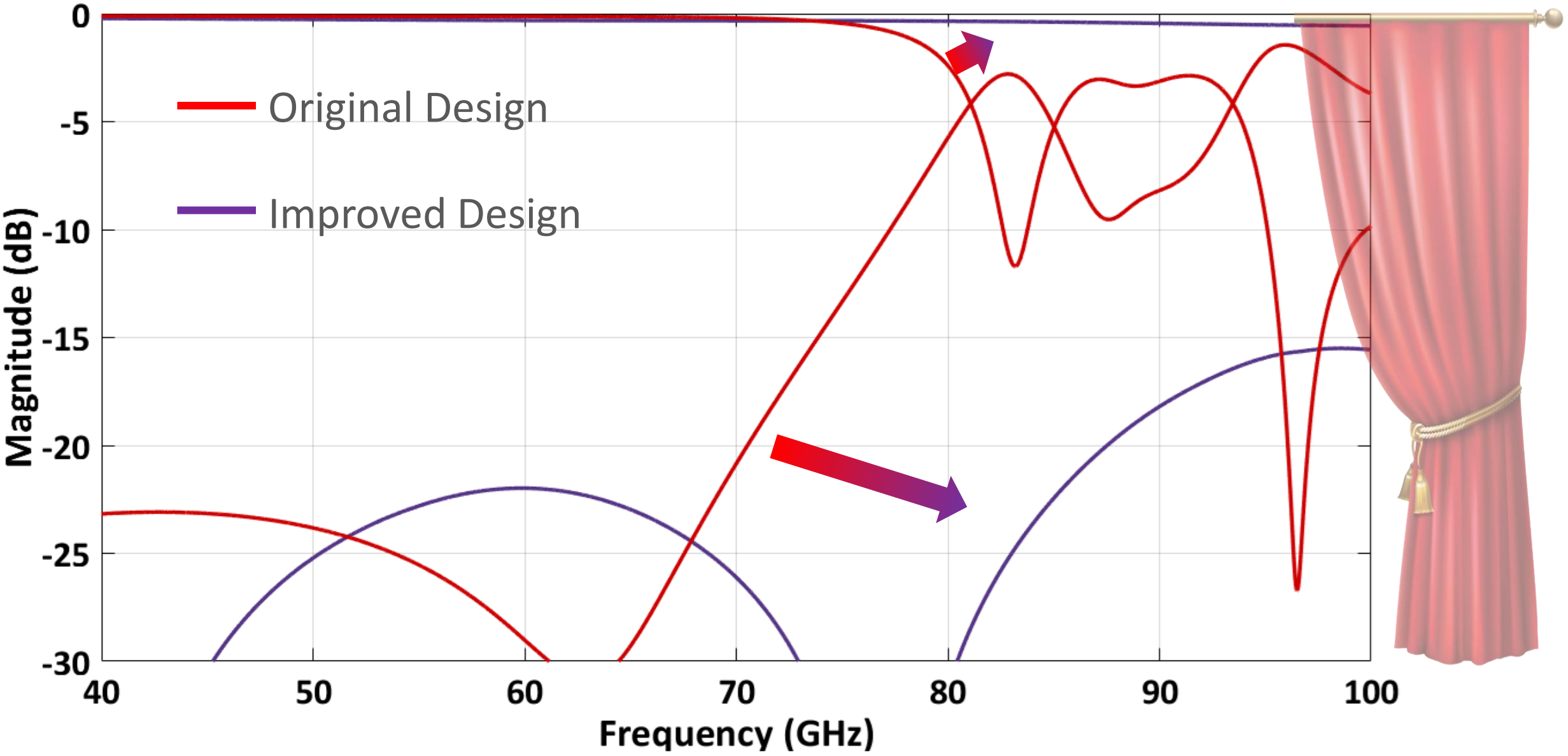
S-parameters vs. Frequency



Measuring a Device Accurately

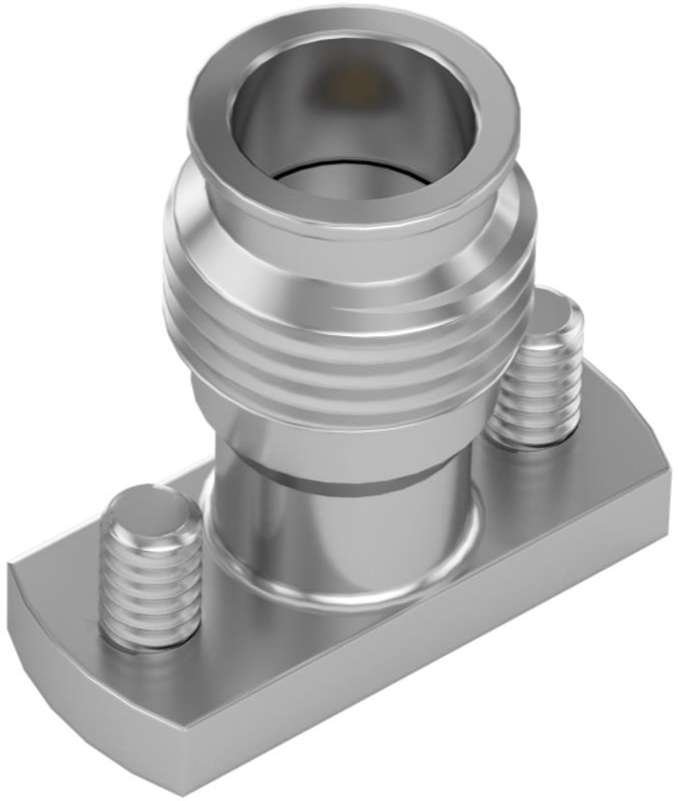


Benefit of Good RF Launch

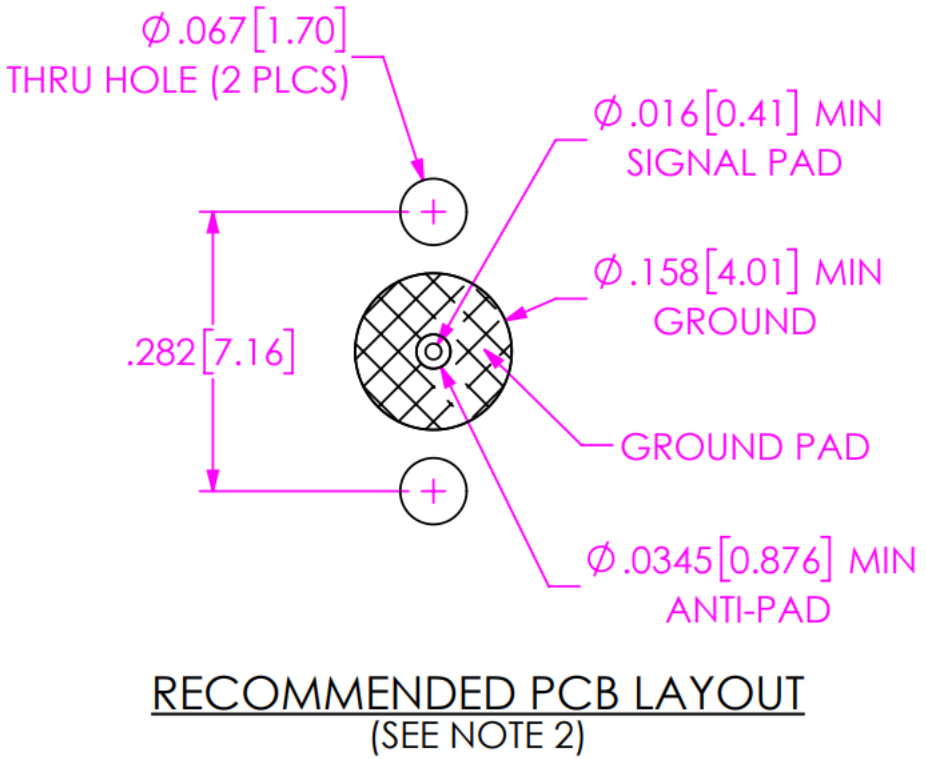


Sub-components of a Very Wide Bandwidth RF Launch

PCB Connector Footprint

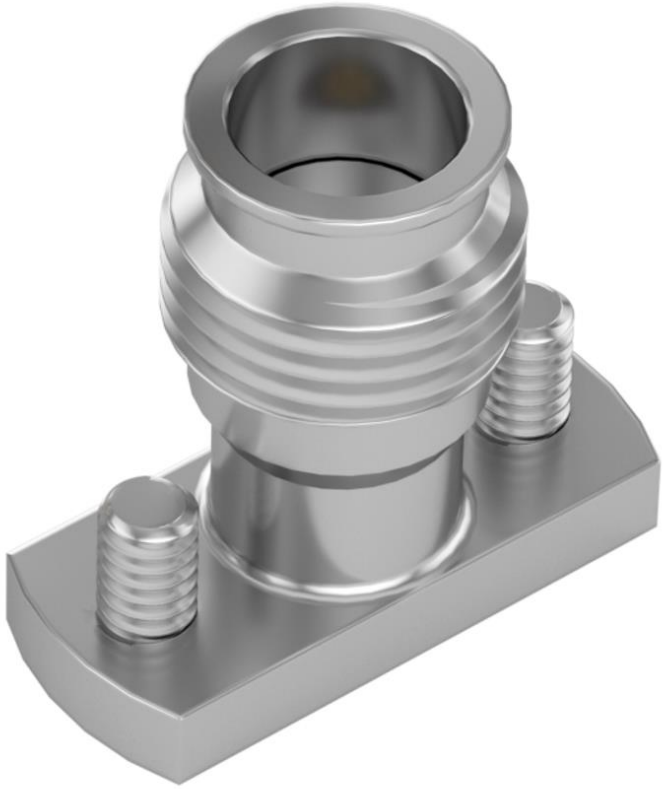


Samtec's 1.35mm compression mount PCB connector

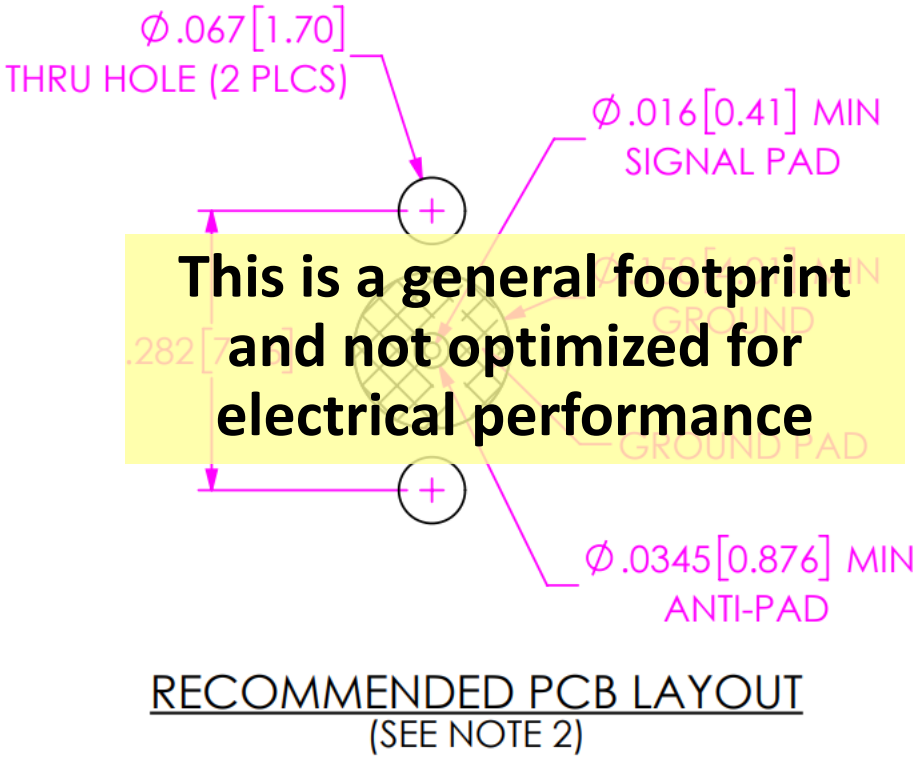


PCB footprint from datasheet

PCB Connector Footprint



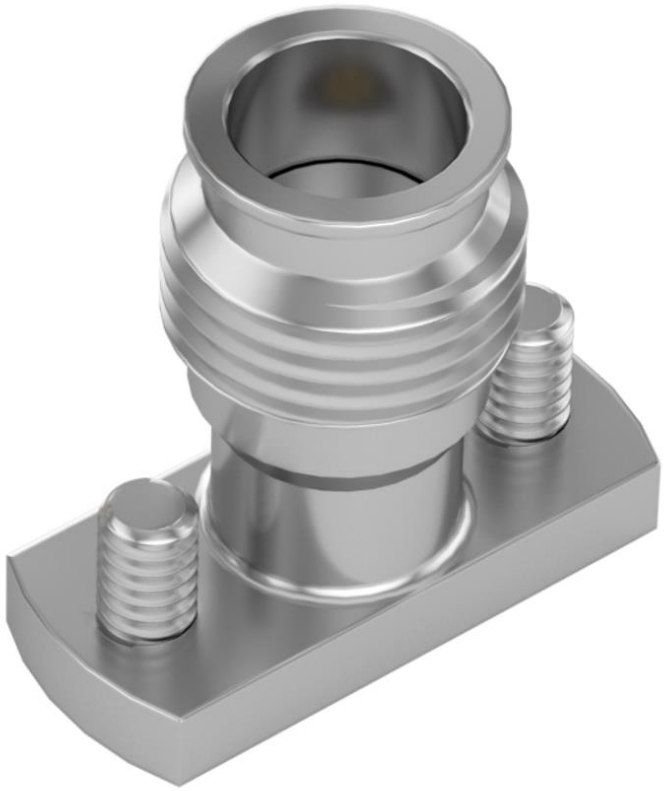
Samtec's 1.35mm compression mount PCB connector



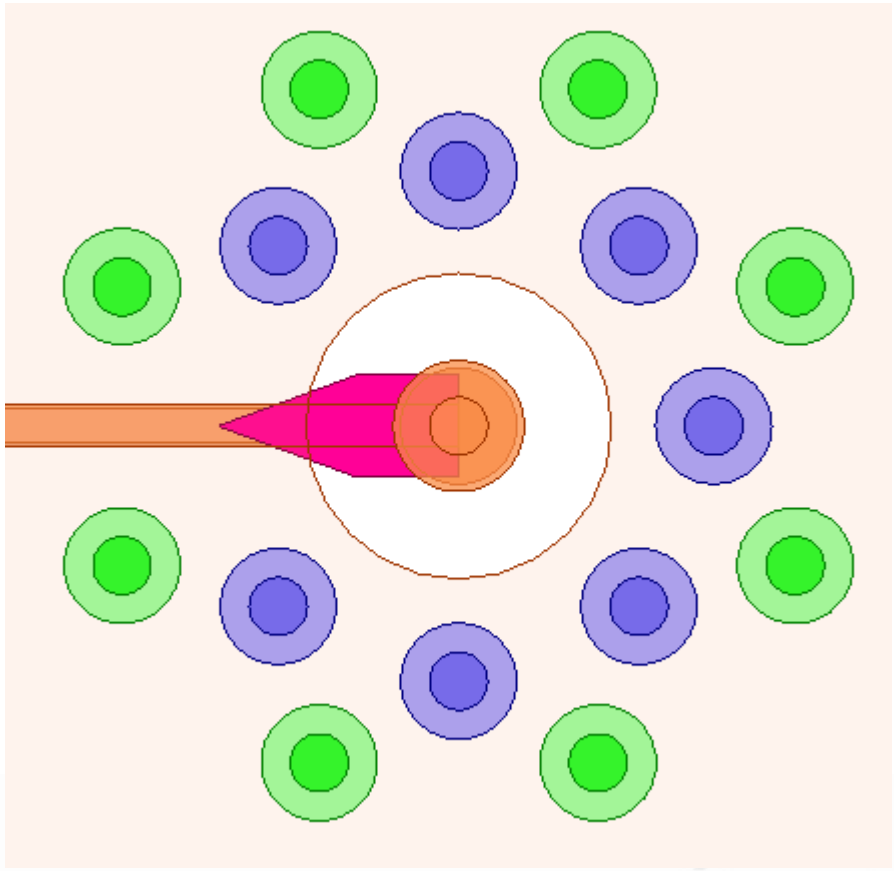
This is a general footprint and not optimized for electrical performance

PCB footprint from datasheet

PCB Connector Optimized Launch



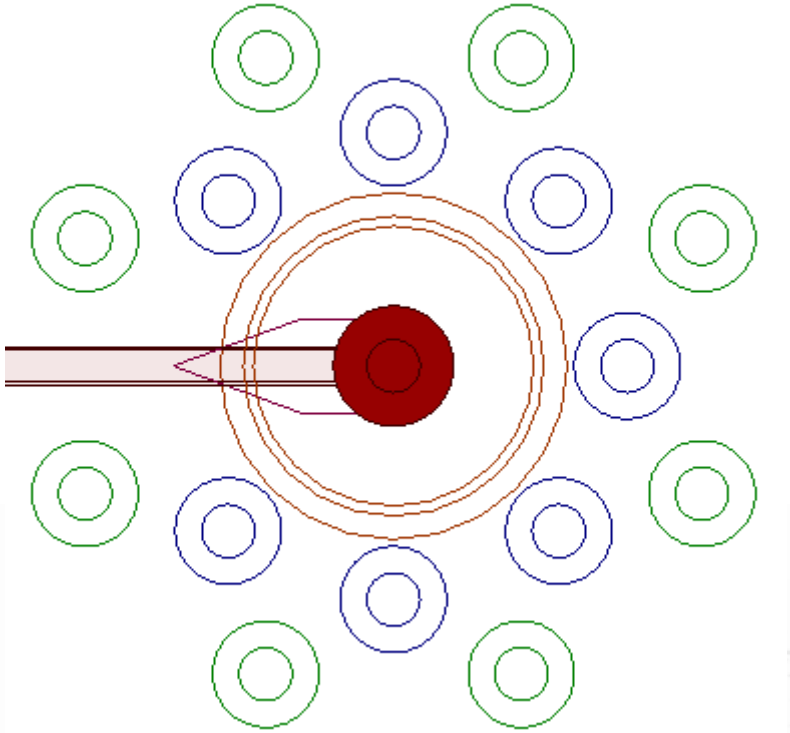
Samtec's 1.35mm compression mount PCB connector



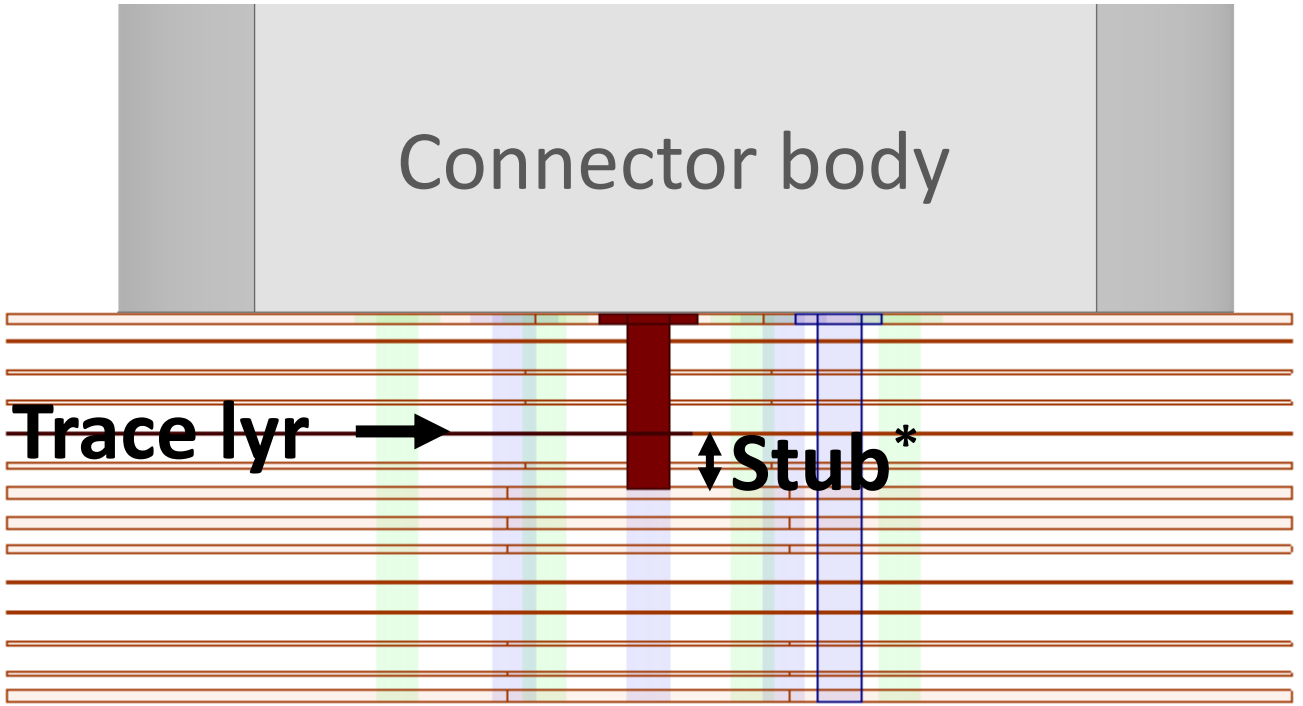
Top view of electrically tuned launch

Parts of a Connector Launch - Landing Pad + Signal Via

Top View



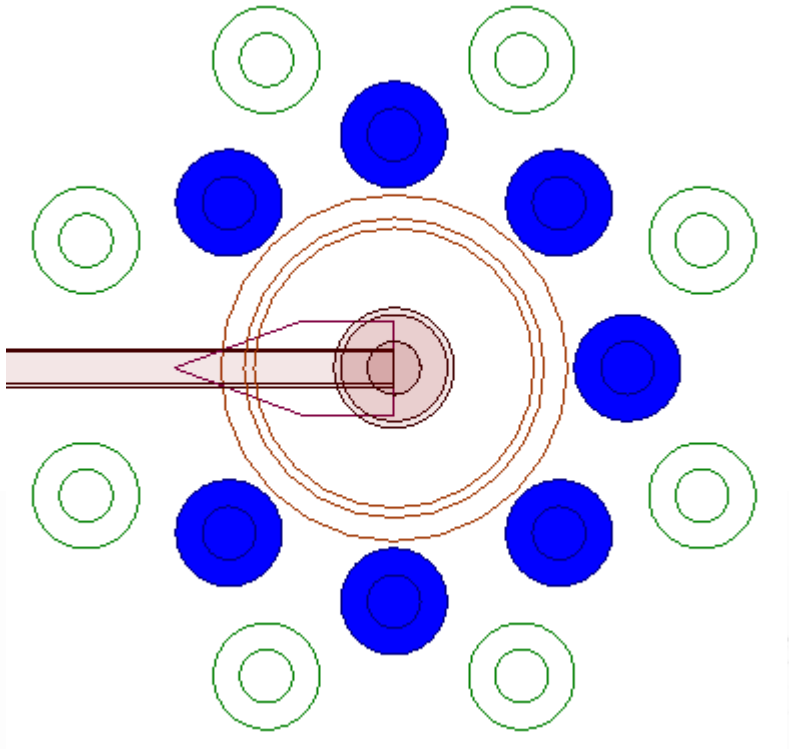
Side View



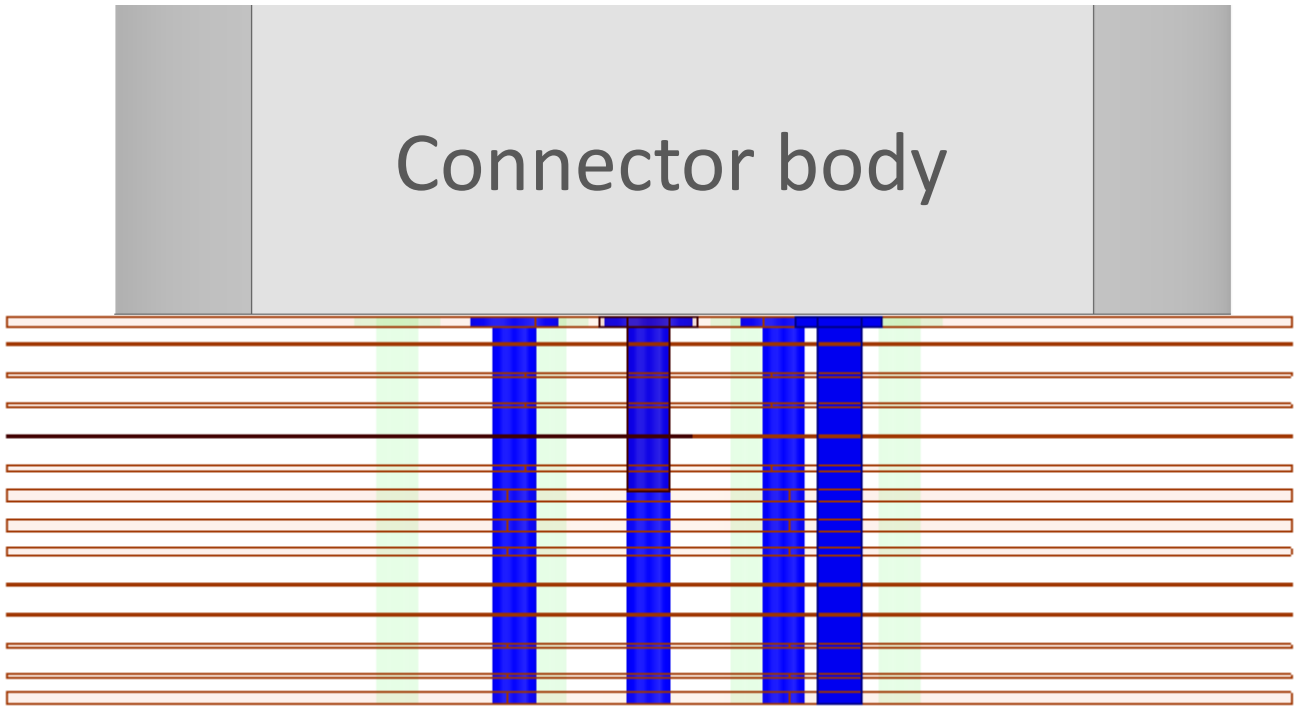
** Deep dive on pages 15-23*

Parts of a Connector Launch - Inner GND

Top View



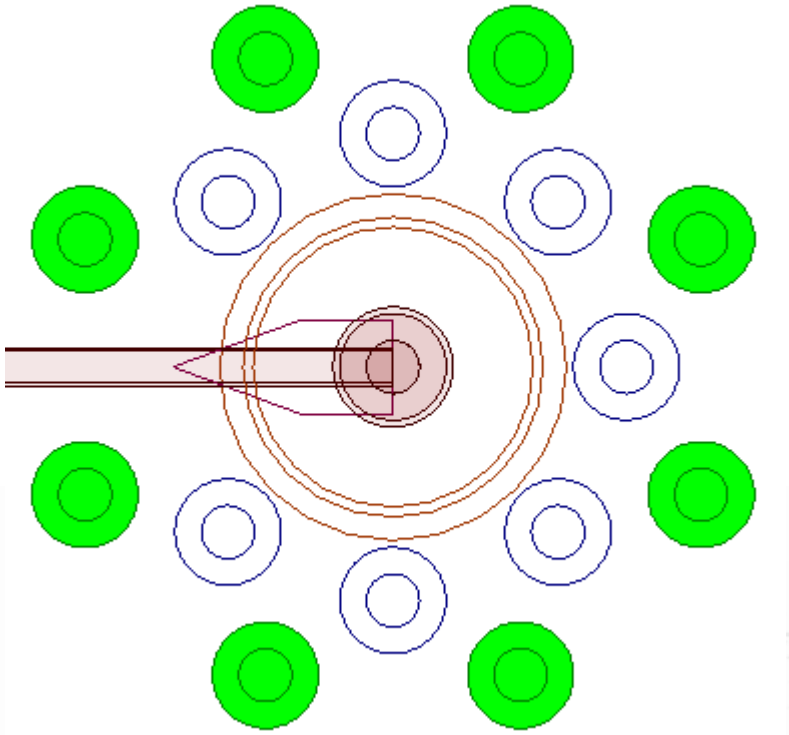
Side View



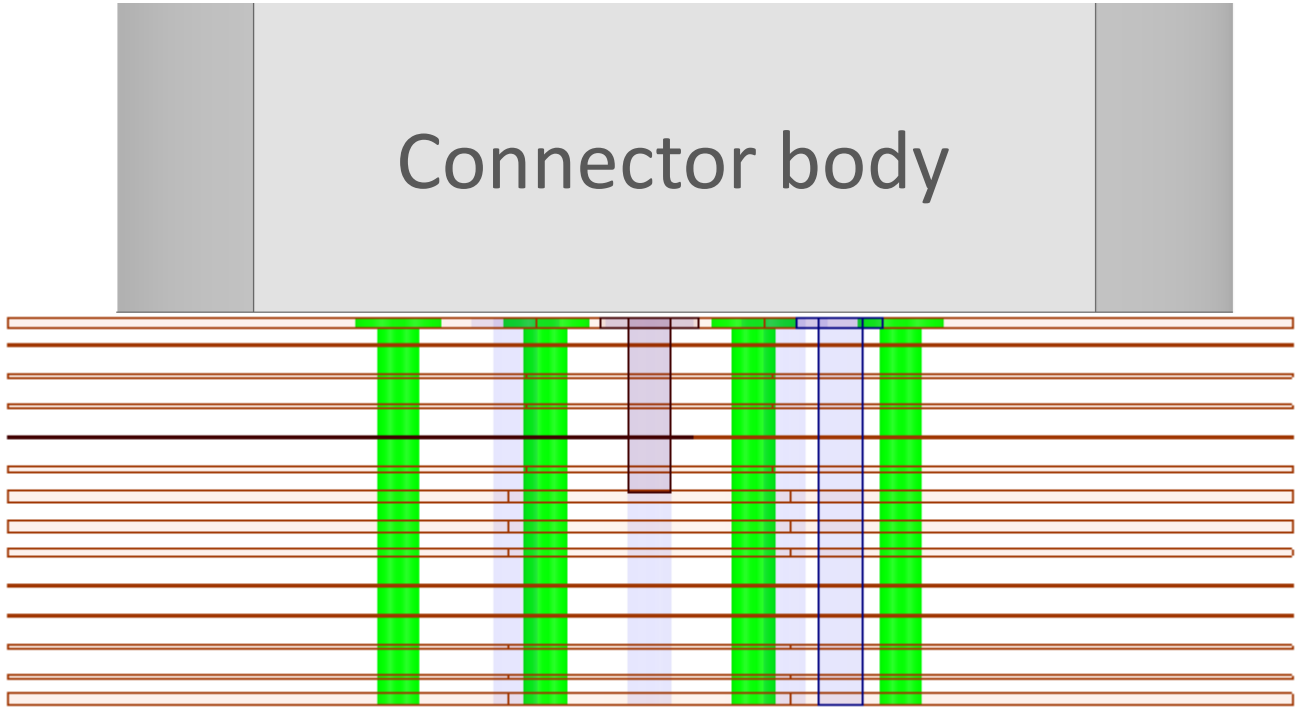
* Deep dive on pages 24-34

Parts of a Connector Launch - Outer GND ring

Top View

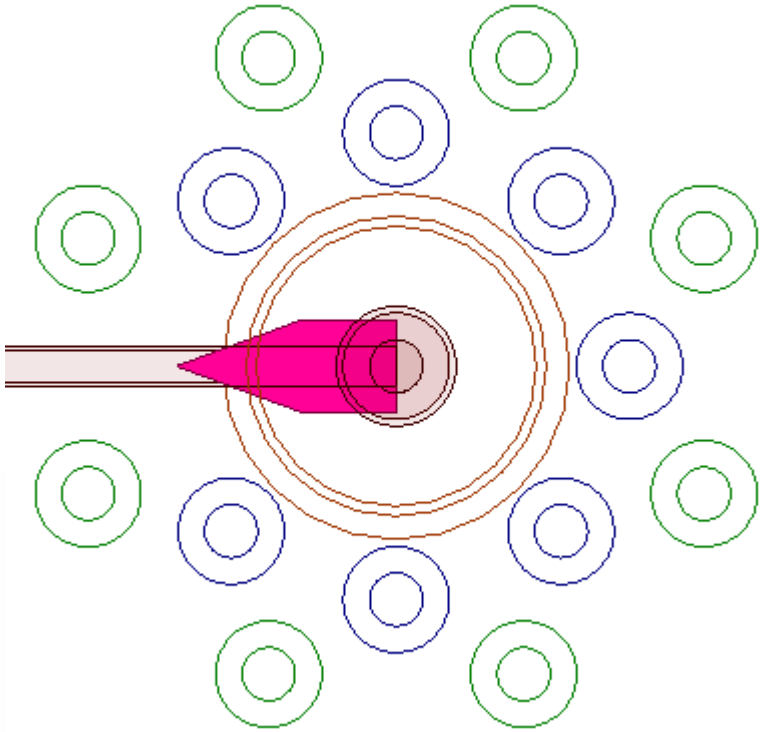


Side View

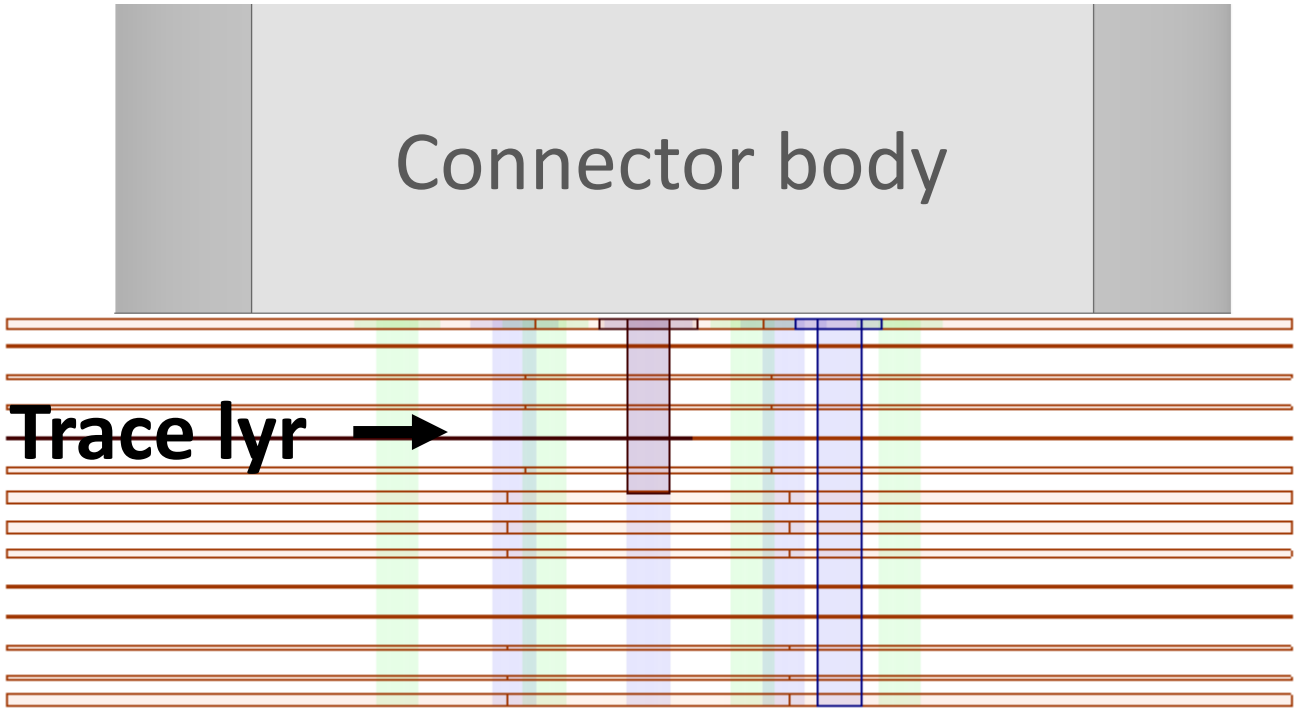


Parts of a Connector Launch - Tuning Feature

Top View



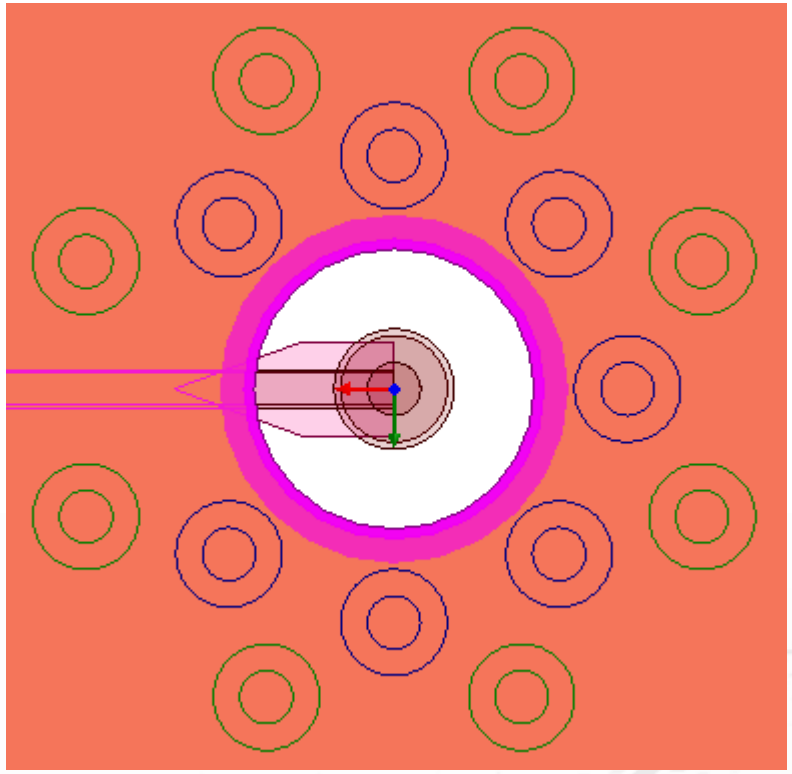
Side View



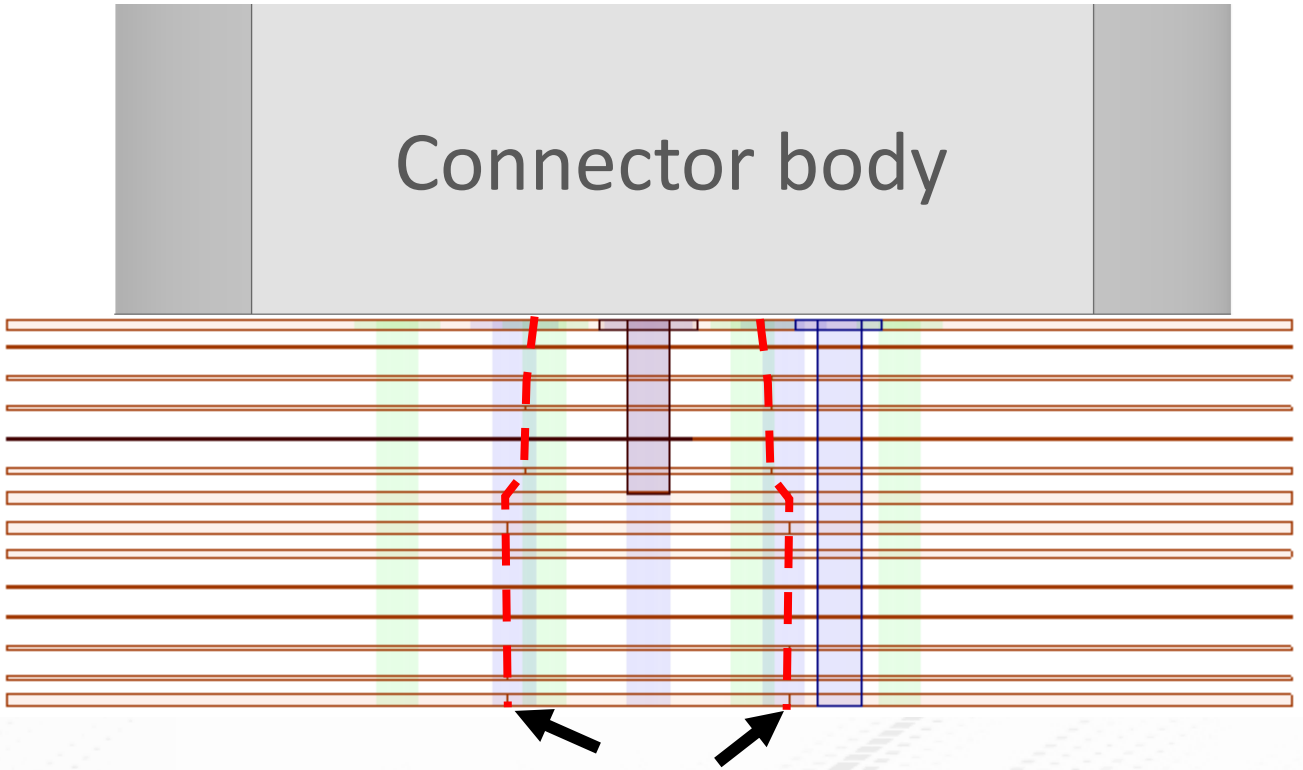
* *Deep dive on pages 35-40*

Parts of a Connector Launch - Plane Voids

Top View



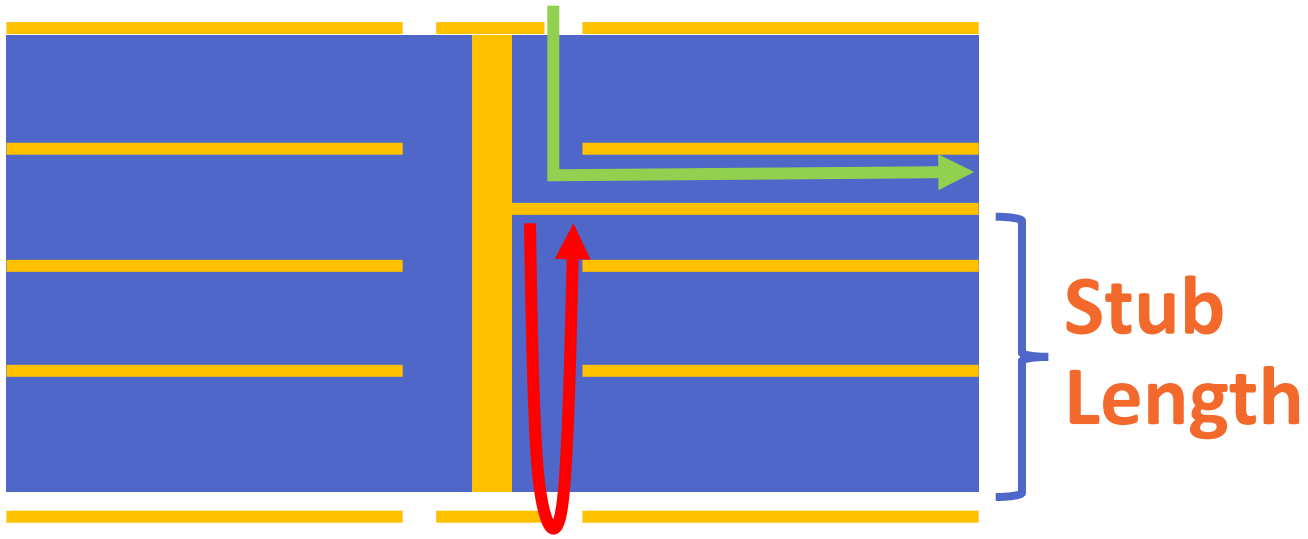
Side View



Key Focus Areas for an RF Launch

- **Stub impact**
- Correct GND ring sizing
- Misregistration compensation
- Improving assembly processes

Impact of Via Stubs - Suck Out Frequency



Desired Signal Path

Unwanted Signal Path

$$f_0 \approx \frac{c}{4\,(Stub\ length)\sqrt{\varepsilon_R}}$$

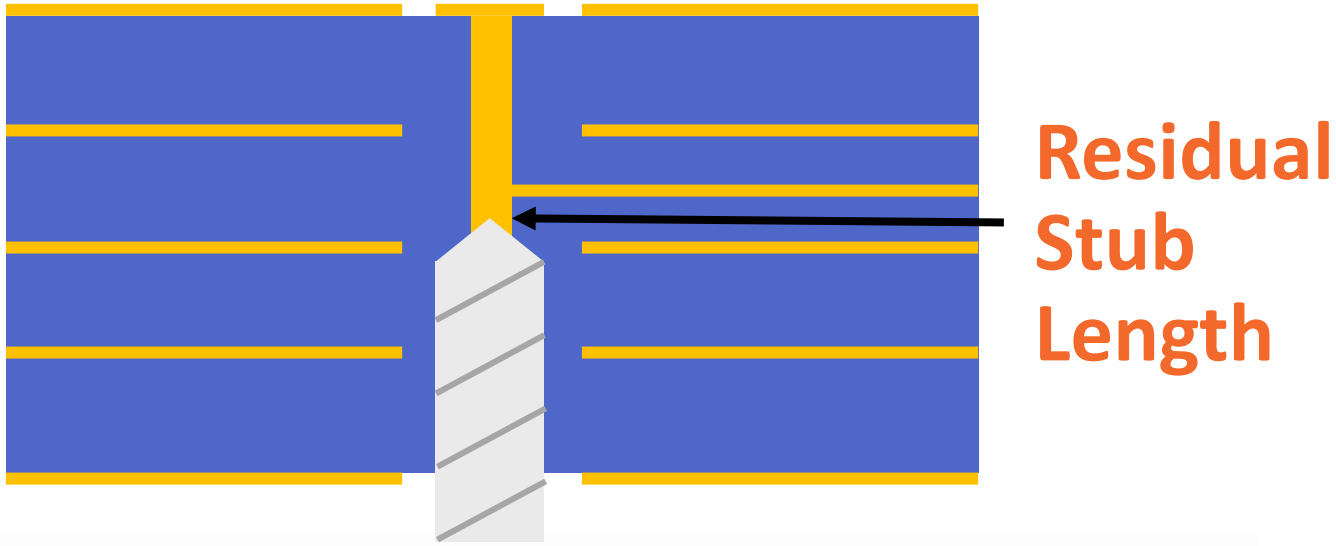
f_0 in Hz

c = Speed of light in vacuum [in/s]

Stub length in inches

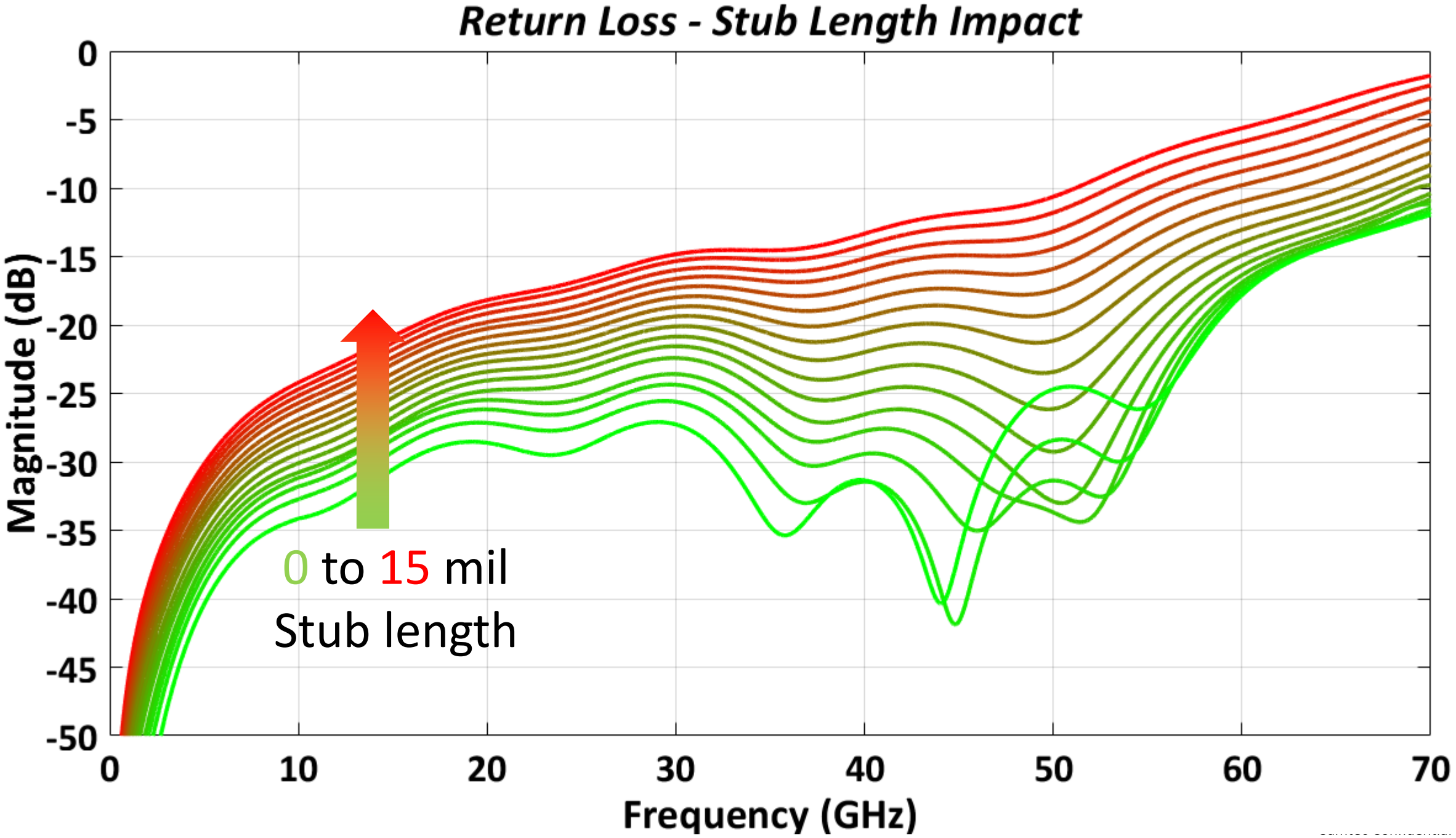
ε_R = Relative dielectric constant **<u>seen by the via</u>**

Reduce Impact of Via Stubs - Back Drilling

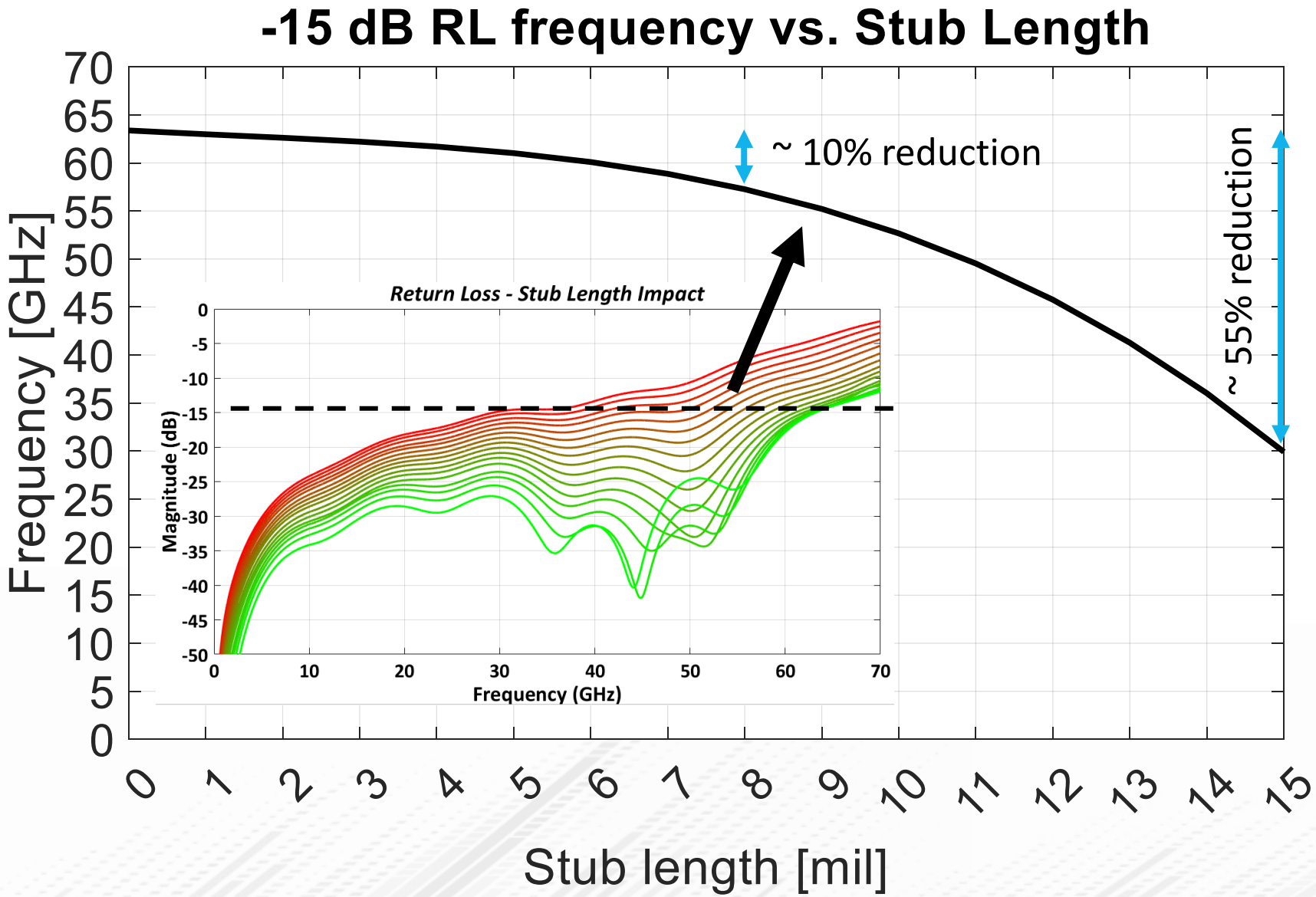


- Back drilling is a process where **most** of the via stub is removed
- Residual stub remains
- Residual stub has a nominal length and tolerance

  E.g: 8mil ± 4mil

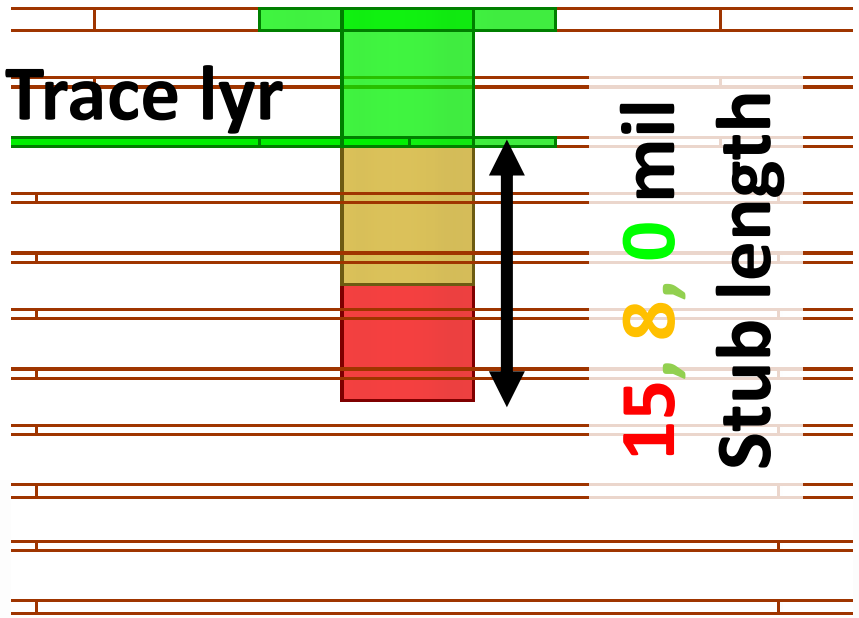

Return Loss - Stub Length Impact
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
Magnitude (dB)
0
10
20
30
40
50
60
70
Frequency (GHz)
0 to 15 mil
Stub length

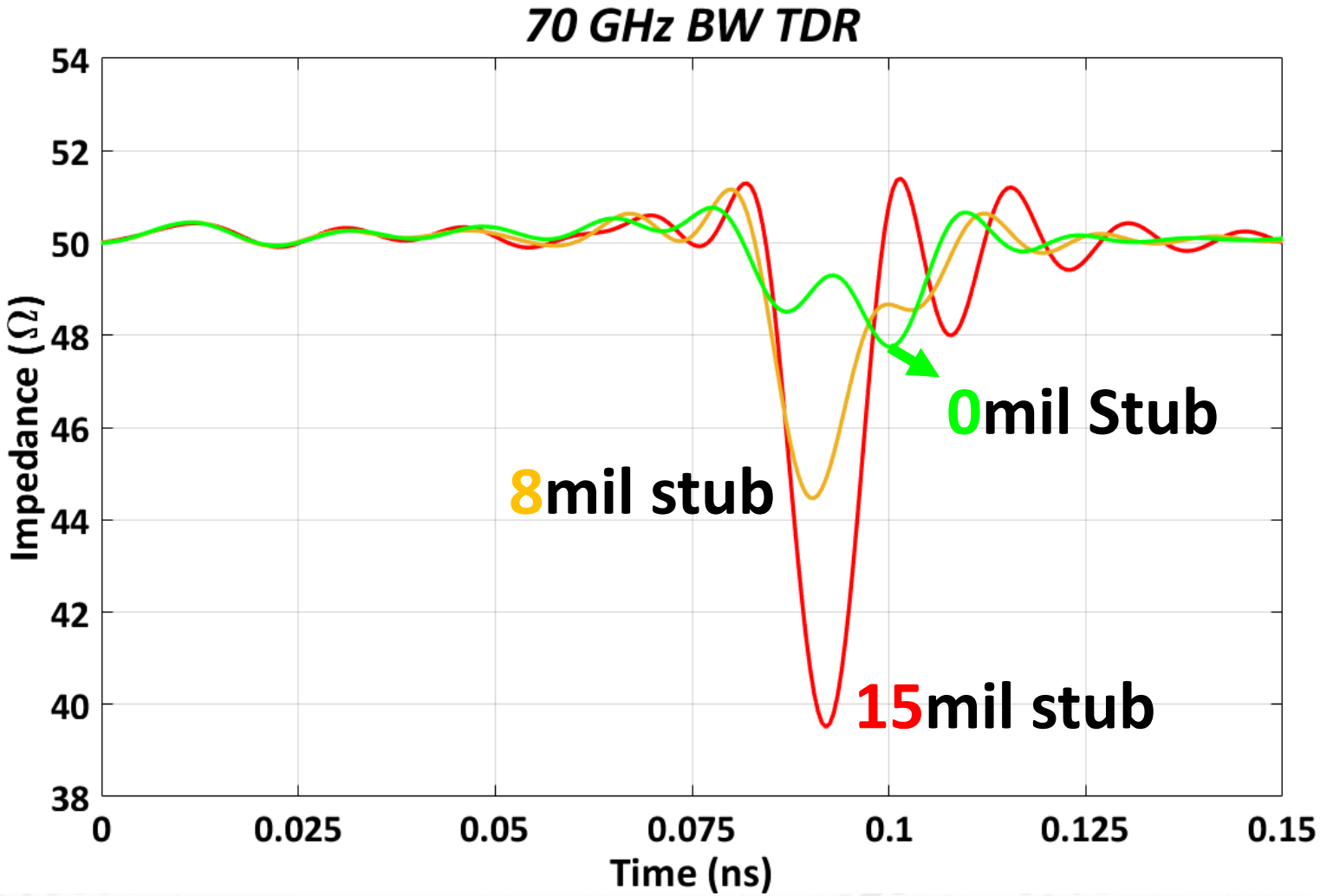
Impact of Via Stubs on Return Loss

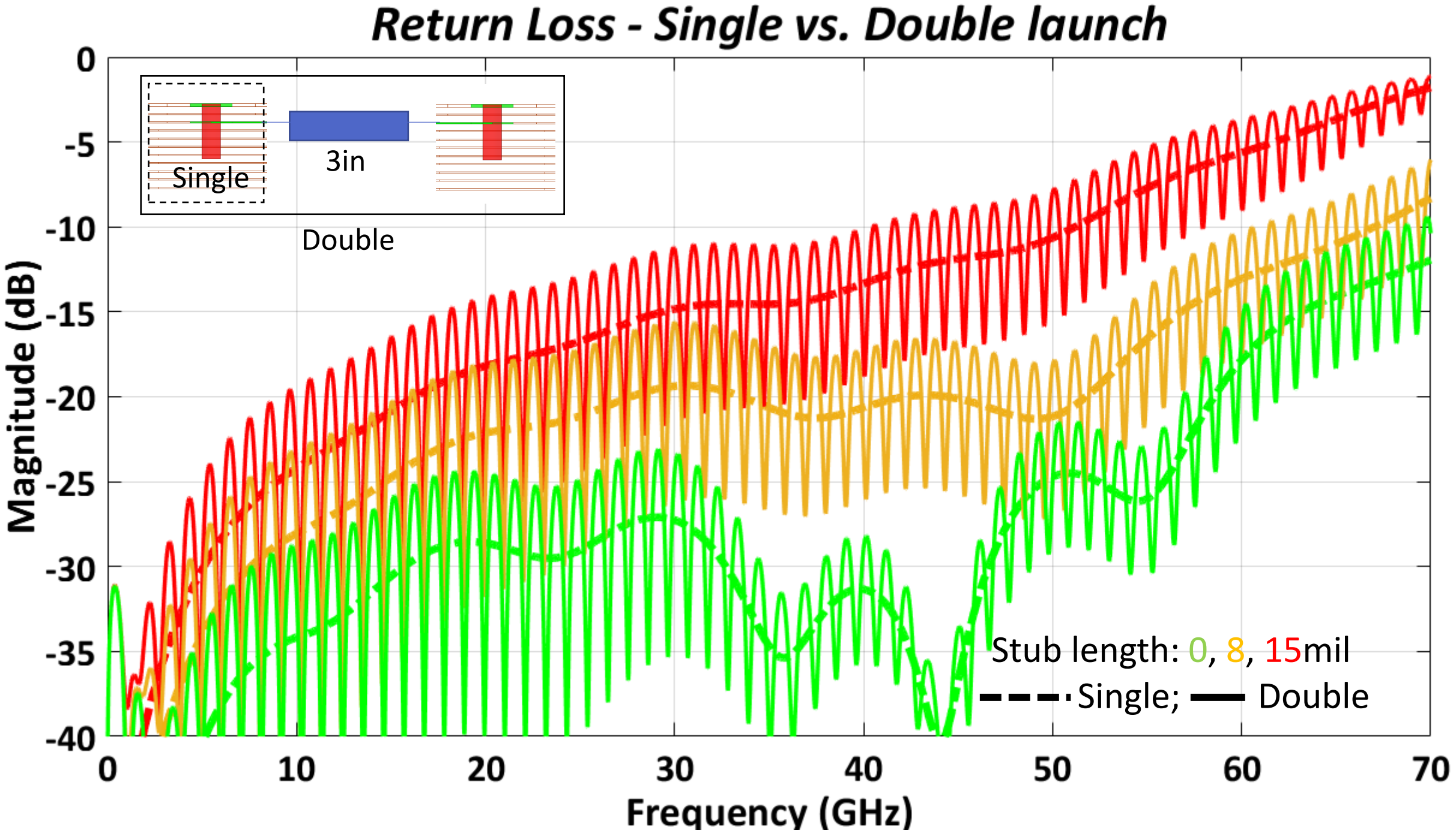


- Impact of <5mil stubs minimal
- Impact worsens non-linearly for longer stubs

Single Launch Z Profile - Stub Impact



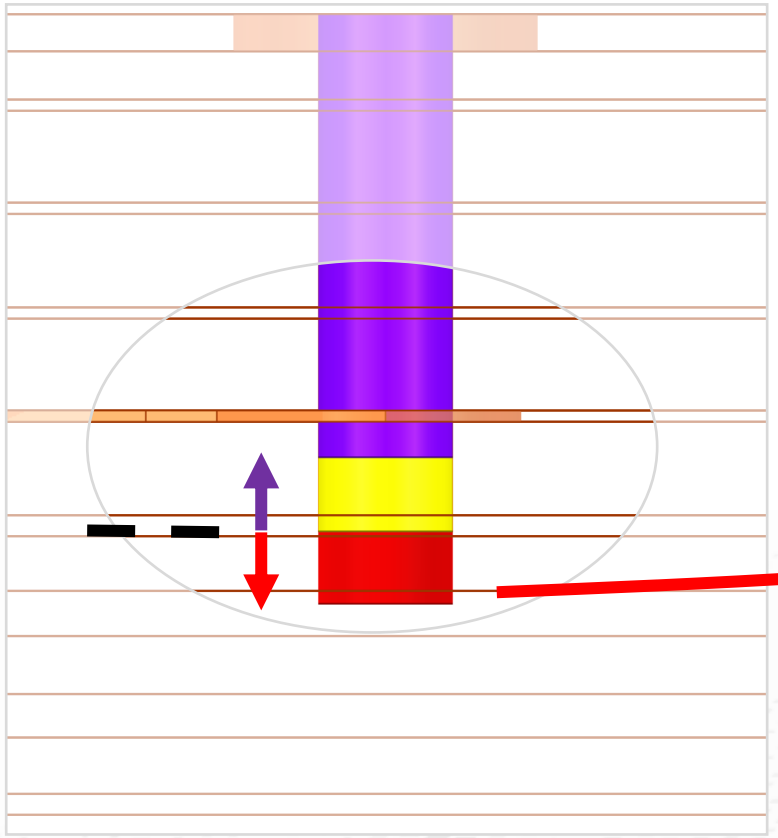


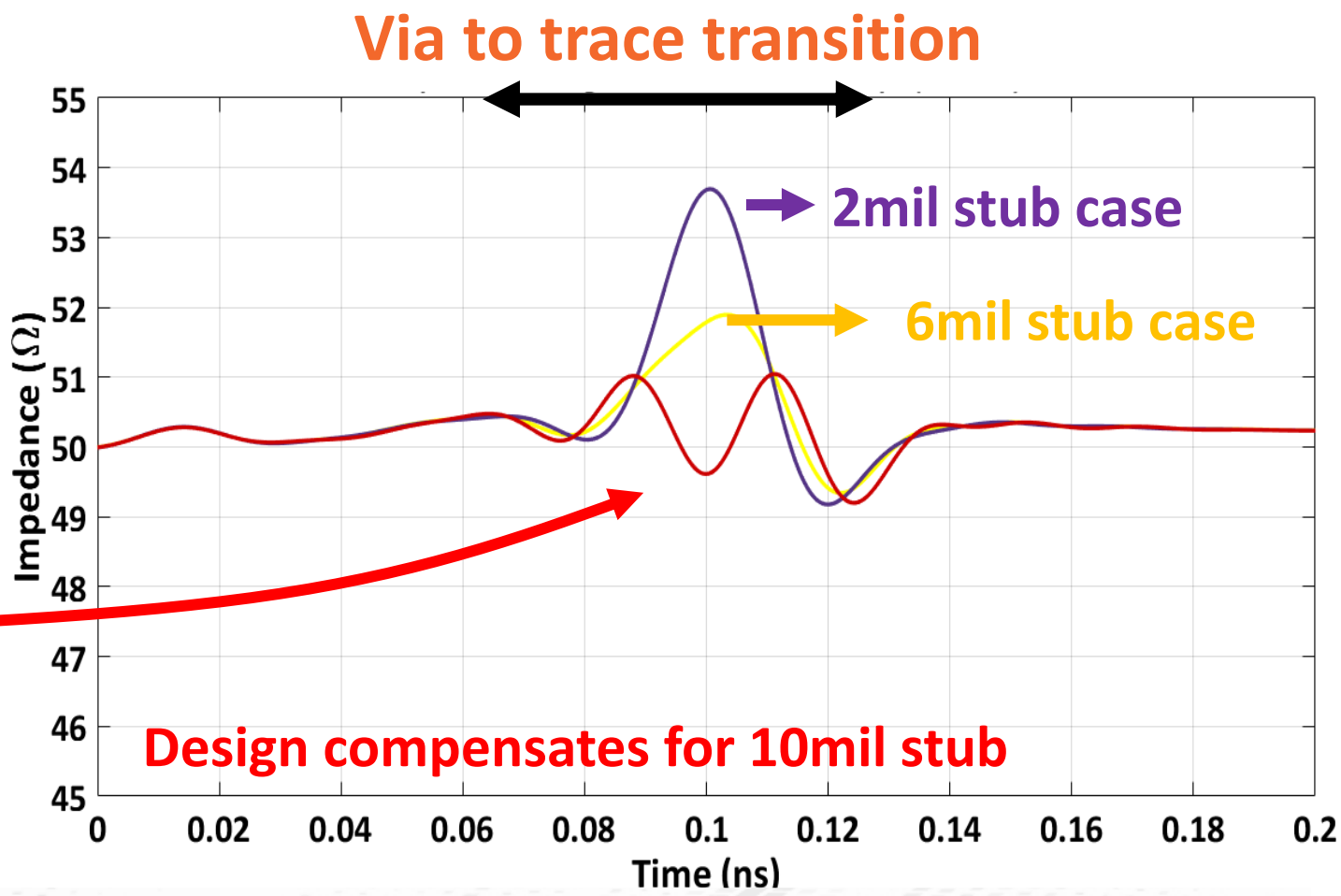

Return Loss - Single vs. Double launch
Single
3in
Double
Magnitude (dB)
0
-5
-10
-15
-20
-25
-30
-35
-40
0
10
20
30
40
50
60
70
Frequency (GHz)
Stub length: 0, 8, 15mil
Single; Double

Properly Accounting for Stub Tolerance

- With large stub tolerance, compensation based on longest stub is **not** good design.

Stub:
6mil ± 4mil





Section Takeaways

>8 mil via stub will hinder getting > ~ 60 GHz launch bandwidth

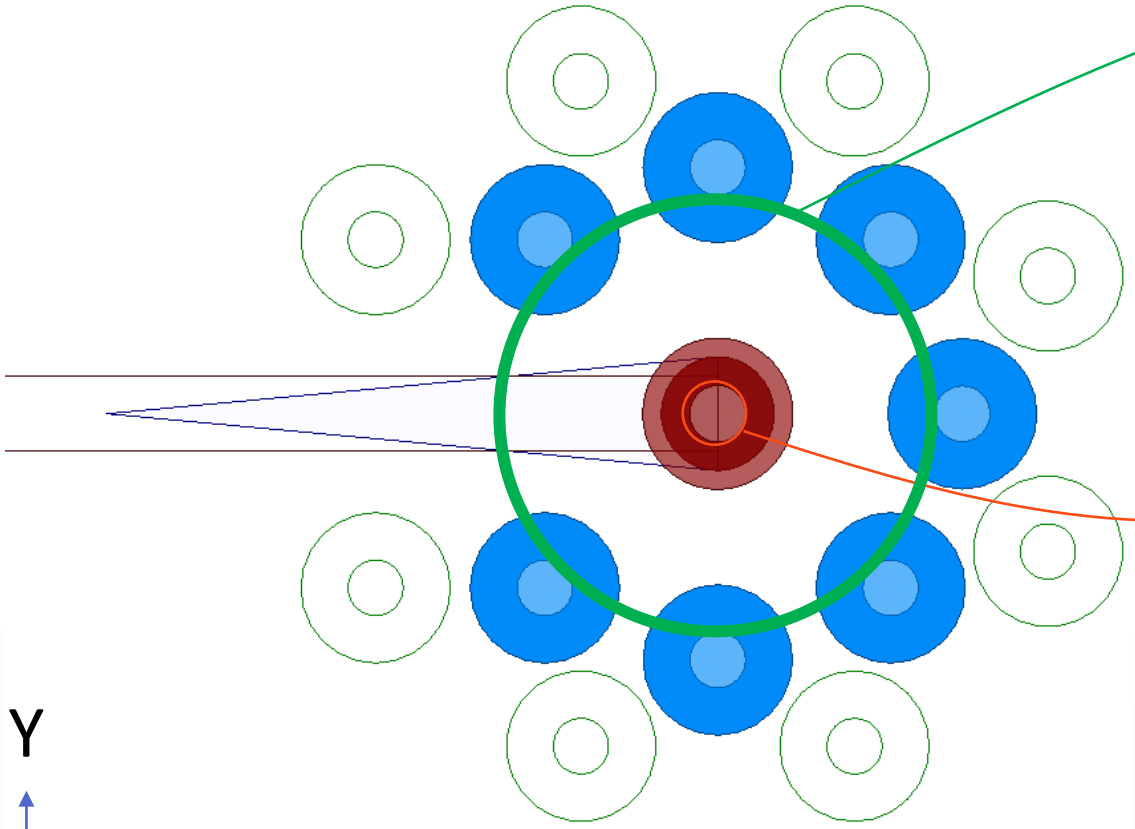
Fab limits on stub length **AND** length tolerance will determine launch limits

Designing in compensation for longest stub will make things bad for shortest stub length. Tight tolerance is key for wide bandwidth!

Key Focus Areas for an RF Launch

- Stub impact
- **Correct GND ring sizing**
- Misregistration compensation
- Improving assembly processes

Inner GND Ring Sizing - Impedance perspective



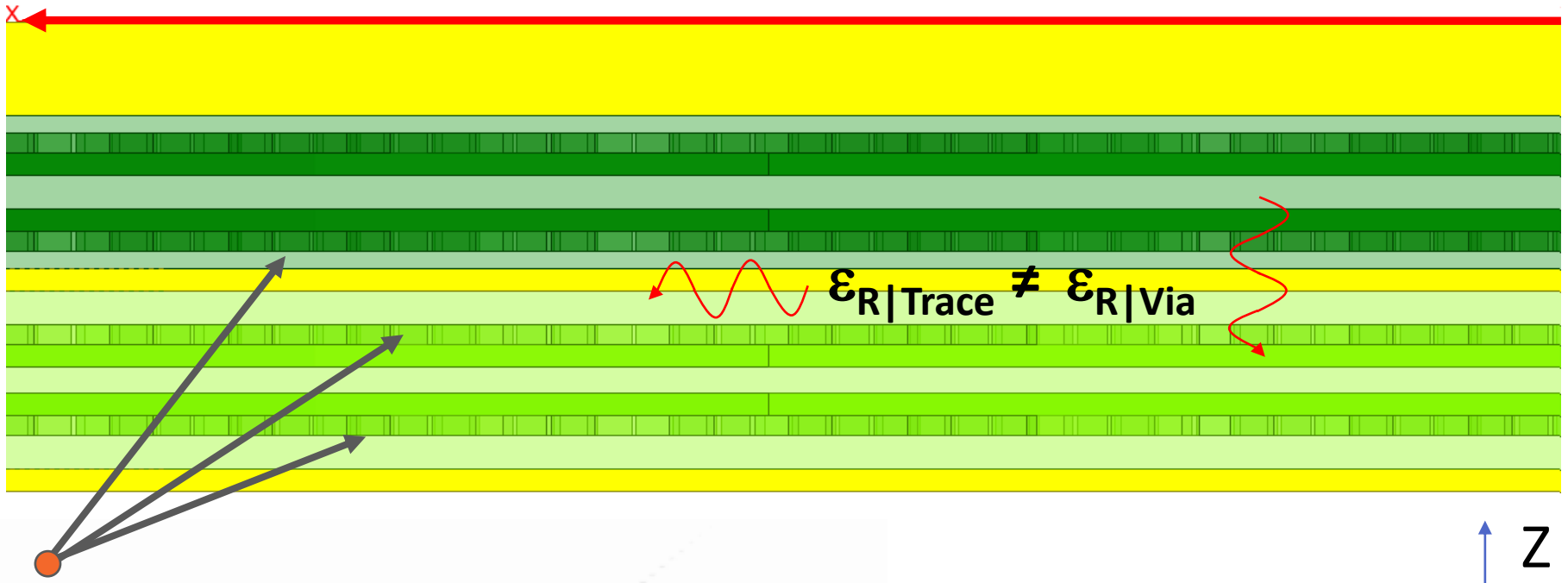
$$Z_0 = 138 \frac{\log_{10}\left(\frac{D_{GND}}{D_V}\right)}{\sqrt{\varepsilon_R}}$$

Z_0 in Ohms

D_V, D_{GND} in inches

ε_R = Relative dielectric constant **seen by the via**

ε_R Seen by the Via?



Glass Cloth

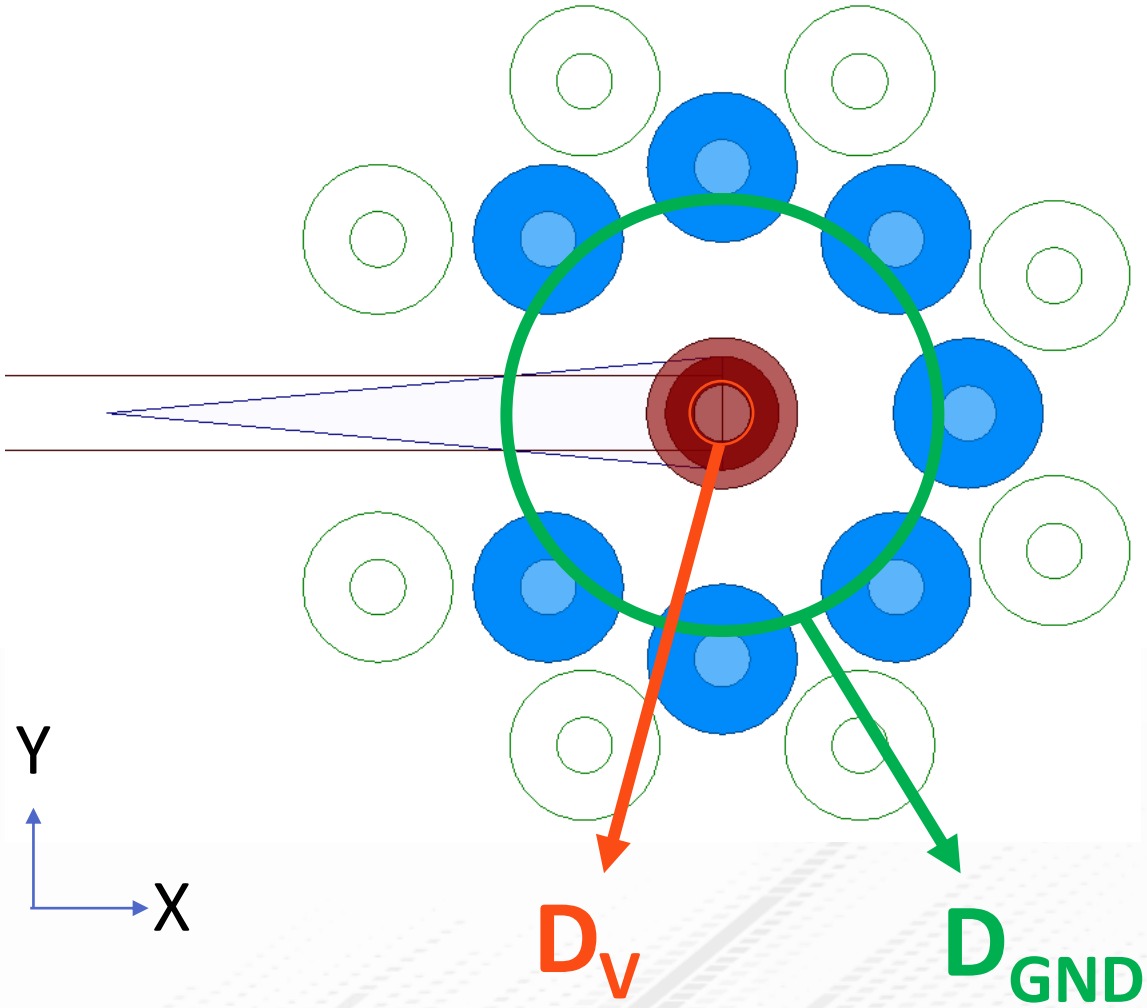
Optimal case:

a. ε_R Glass ≈ ε_R Resin

b. ε_R as low as possible

More info: "A MATERIAL WORLD Modeling dielectrics and conductors for interconnects operating at 10-50 Gbps", Y. Shlepnev., et. al: A Material World, DesignCon 2016

Inner GND Ring Sizing - Higher Modes perspective



$$f_{cutoff} = \frac{11.8}{\sqrt{\varepsilon_R}\,\pi\left(\frac{D_V + D_{GND}}{2}\right)}$$

f_{cutoff} in GHz

D_V, D_{GND} in inches

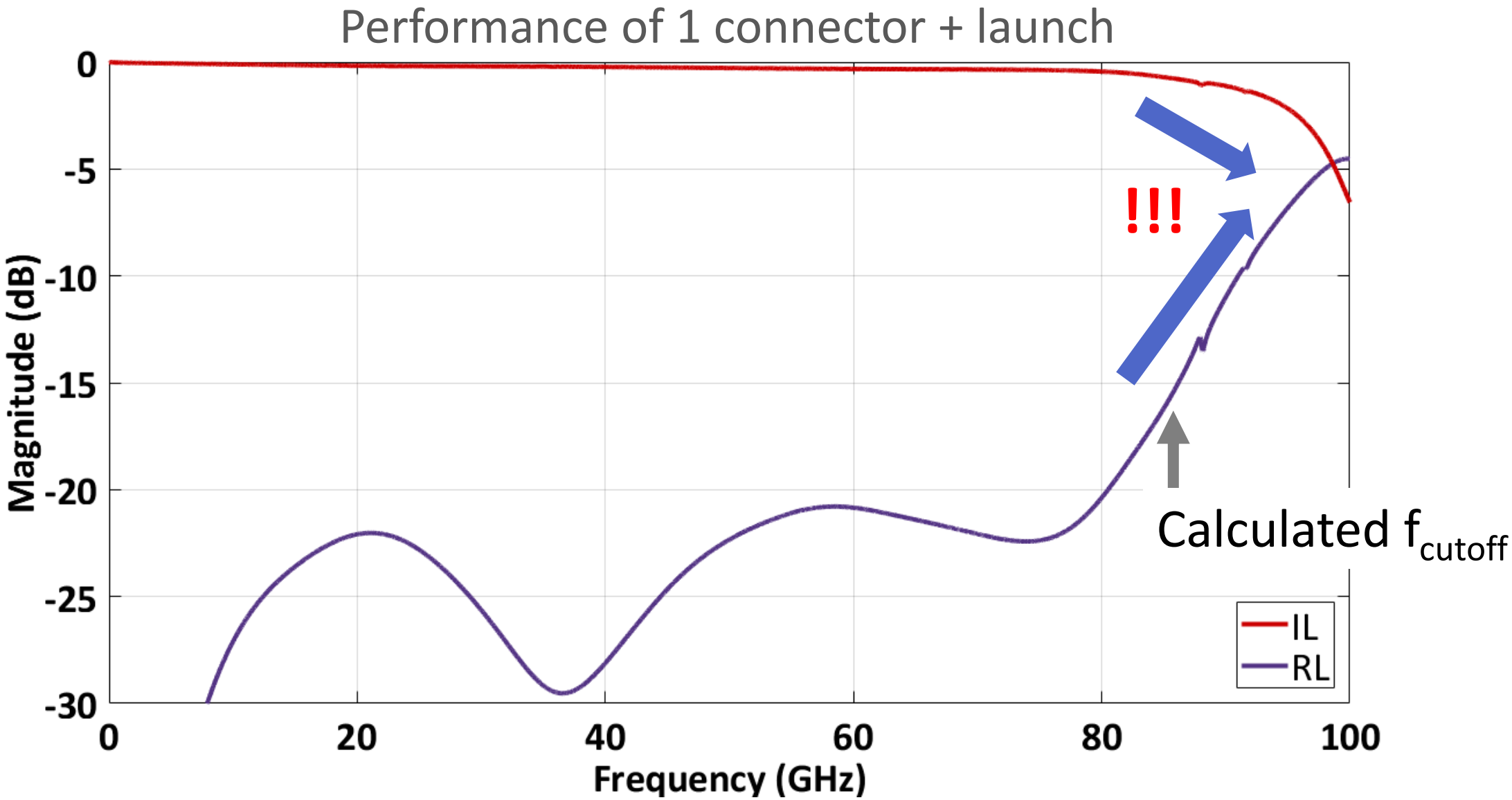
ε_R = Relative dielectric constant **seen by the via**

Inner GND Ring Sizing - What's the Sweet Spot spot?

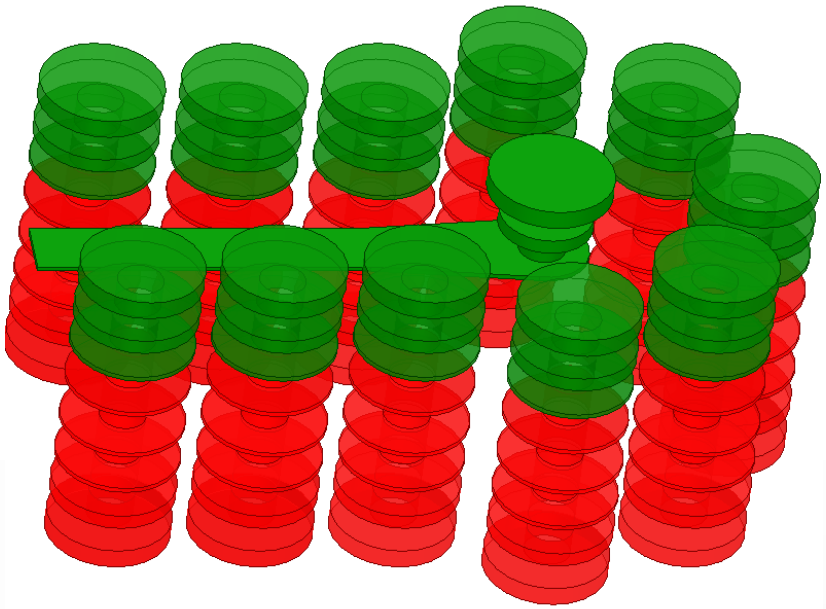
Drill diameter [mil]	Er						
	2.50	2.75	3.00	3.25	3.50	3.75	4.00
3	201	176	156	138	124	111	100
4	151	132	117	104	93	83	75
5	120	106	93	83	74	67	60
6	100	88	78	69	62	56	50
7	86	76	67	59	53	48	43
8	75	66	58	52	46	42	38

f_{cutoff} in GHz

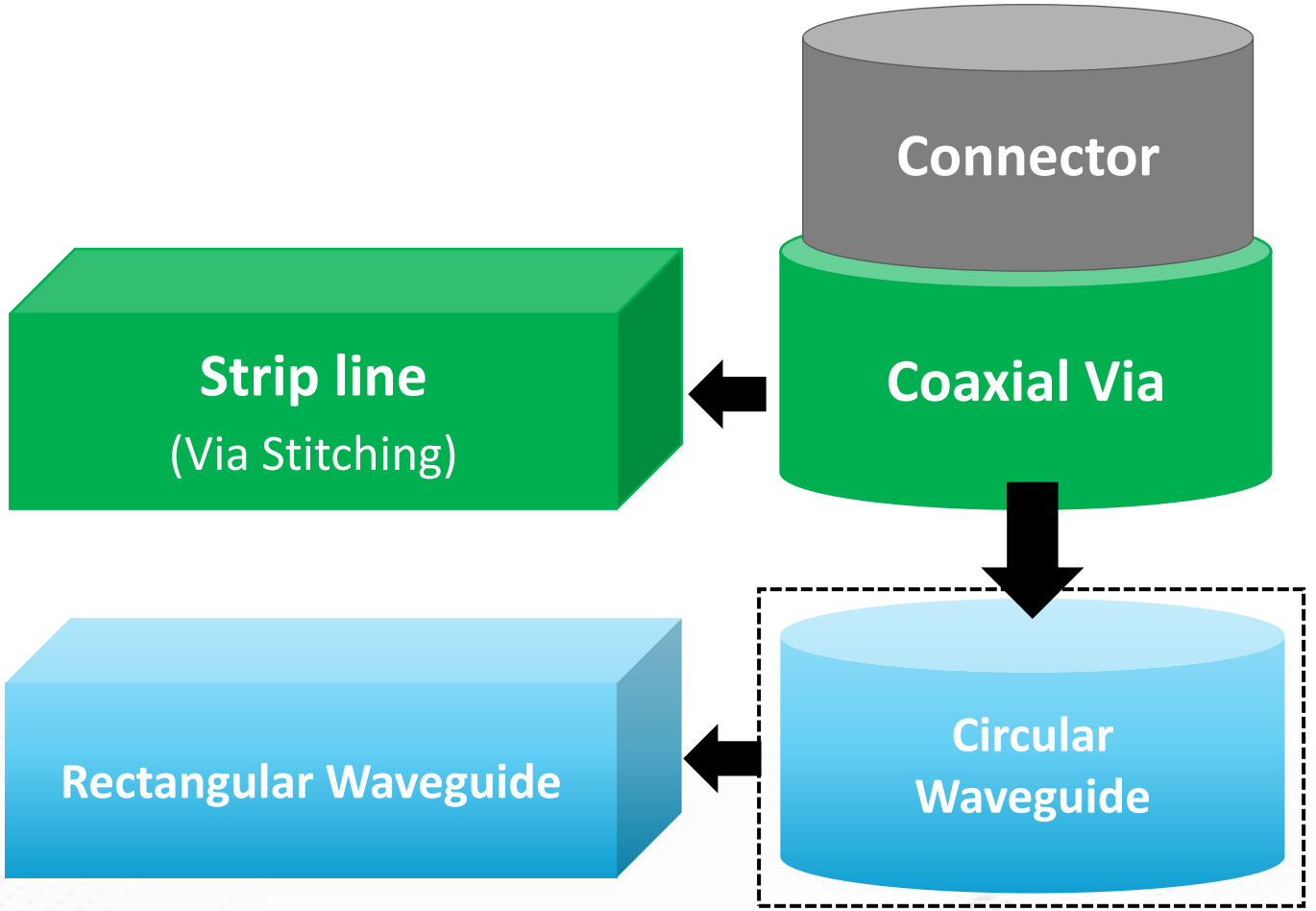
Launch Behavior Change Near f_{cutoff}



Launch Behavior Near f_{cutoff} Visualized

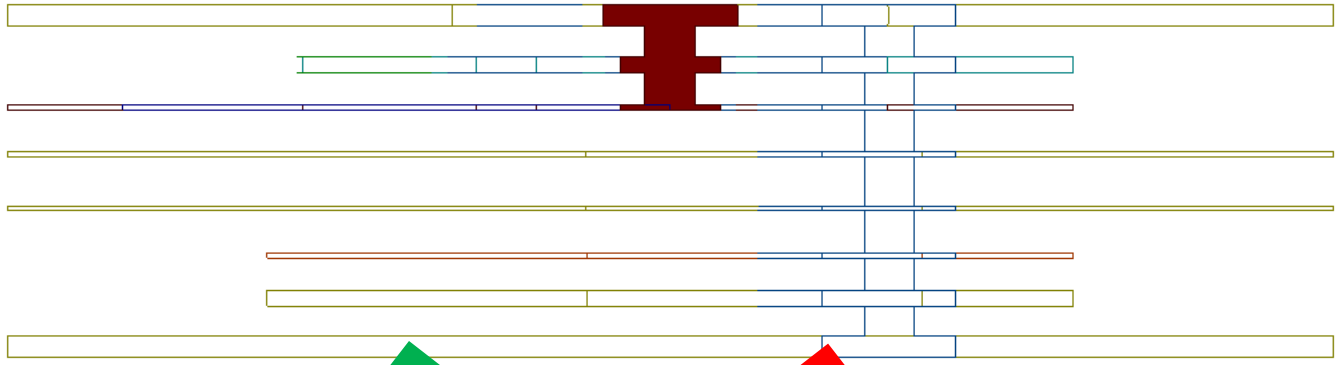


Shared Thru Vias



Launch Behavior Near f_{cutoff} Visualized

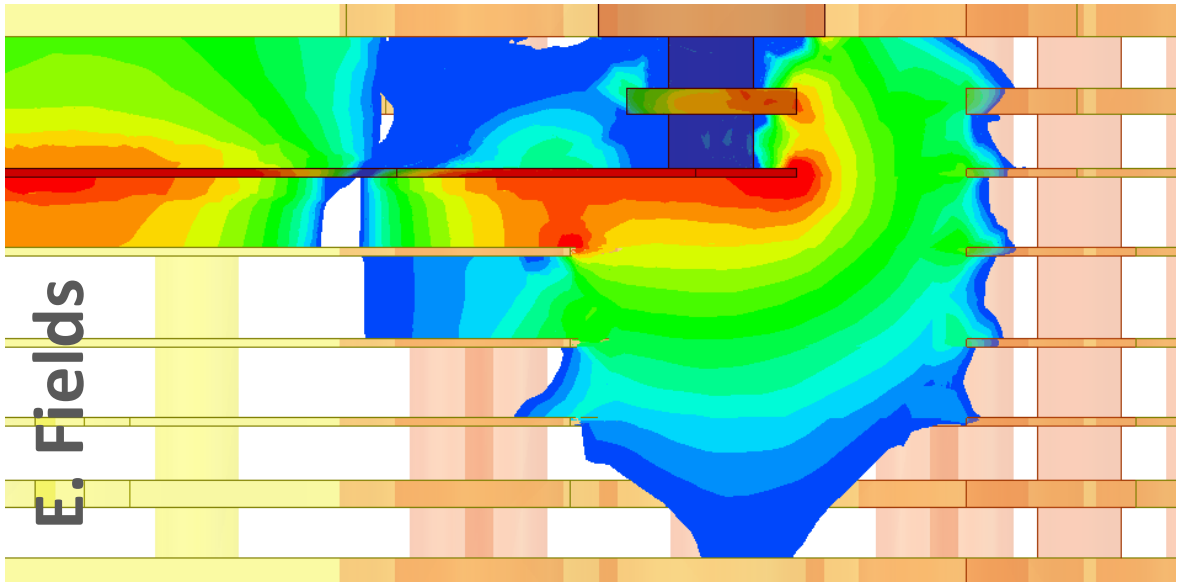
Structure

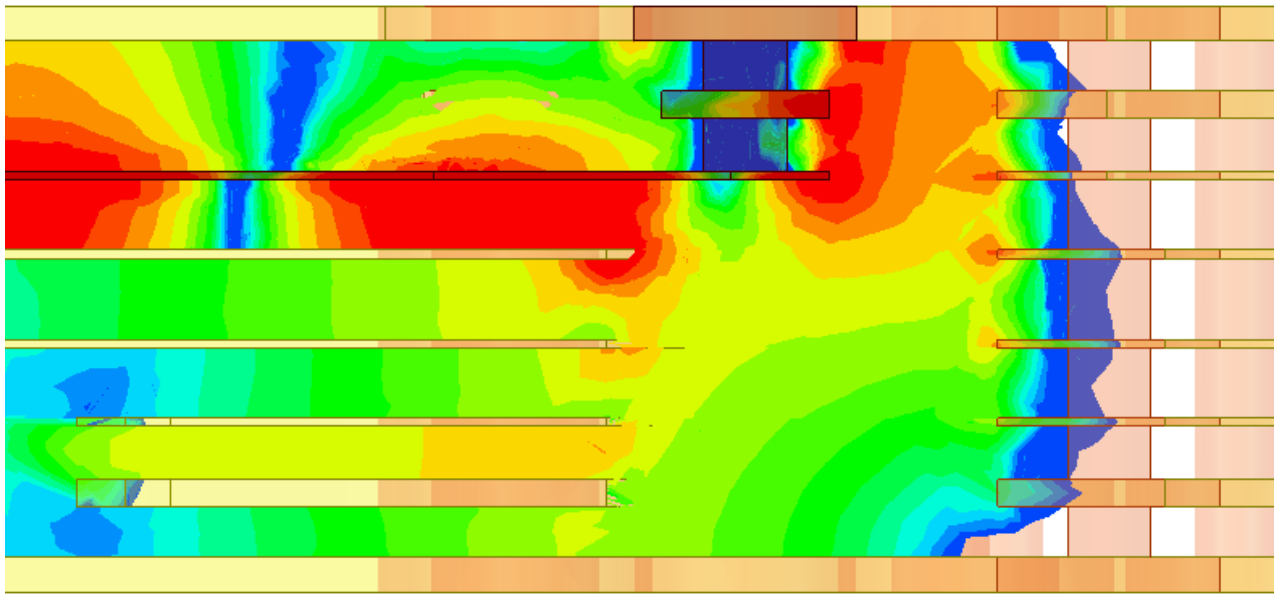


Below f_{cutoff}

Above f_{cutoff}

E. Fields





Field animations: samtec.com/wideband-RF-launches

Telling if f_{cutoff} is Too Low

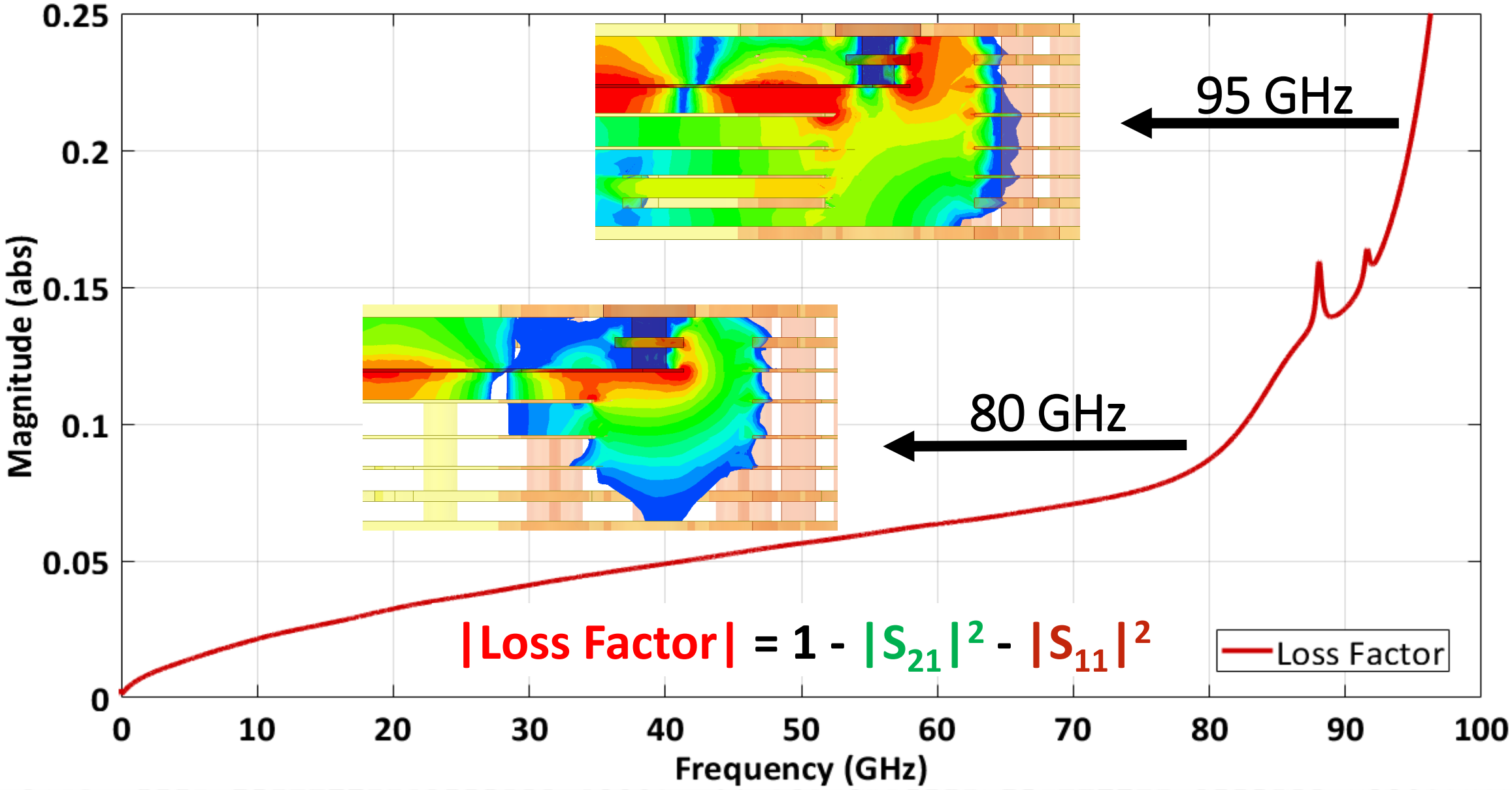
FOR 2 PORTS

$$|\text{Loss Factor}| = 1 - |S_{21}|^2 - |S_{11}|^2$$

Power that flows along unwanted paths

Transmitted power

Reflected Power


0.25
0.2
0.15
0.1
0.05
0
Magnitude (abs)
0
10
20
30
40
50
60
70
80
90
100
Frequency (GHz)
95 GHz
80 GHz
|Loss Factor| = 1 - |S21|2 - |S11|2
Loss Factor

Section Takeaways

RF launches with BW>70 GHz need $\varepsilon_R \leq 3$ and drill diameter $\leq$ 5mil

Plotting loss factor allows seeing when launch breaks down

More details: “PCB Stack up & Launch Optimization in High-speed PCB Designs“, S. Tucker, et. al, DesignCon 2022

Key Focus Areas for an RF Launch

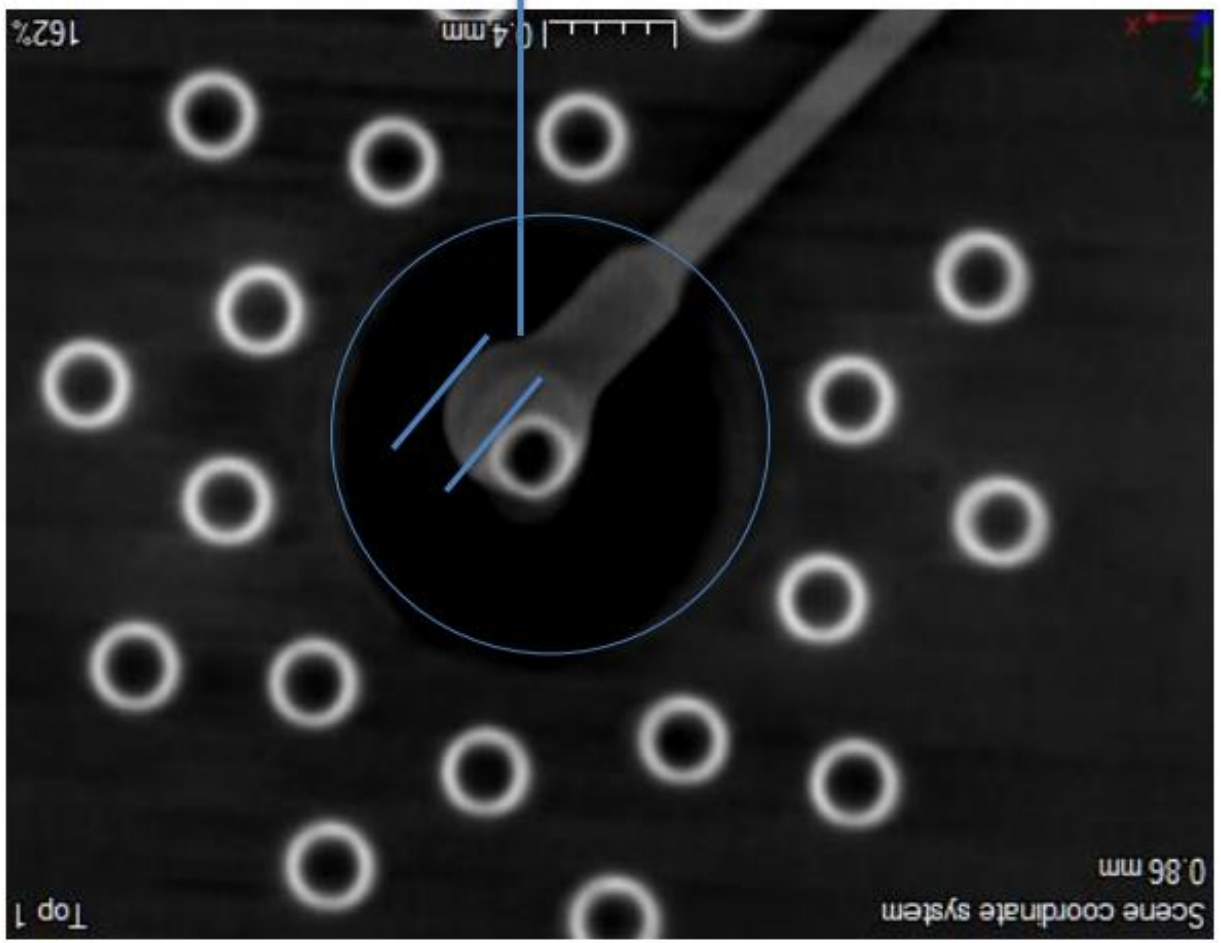
- Stub impact
- Correct GND ring sizing
- **Misregistration compensation**
- Improving assembly processes

Xray Image of PCB with Misregistration

Layer Registration

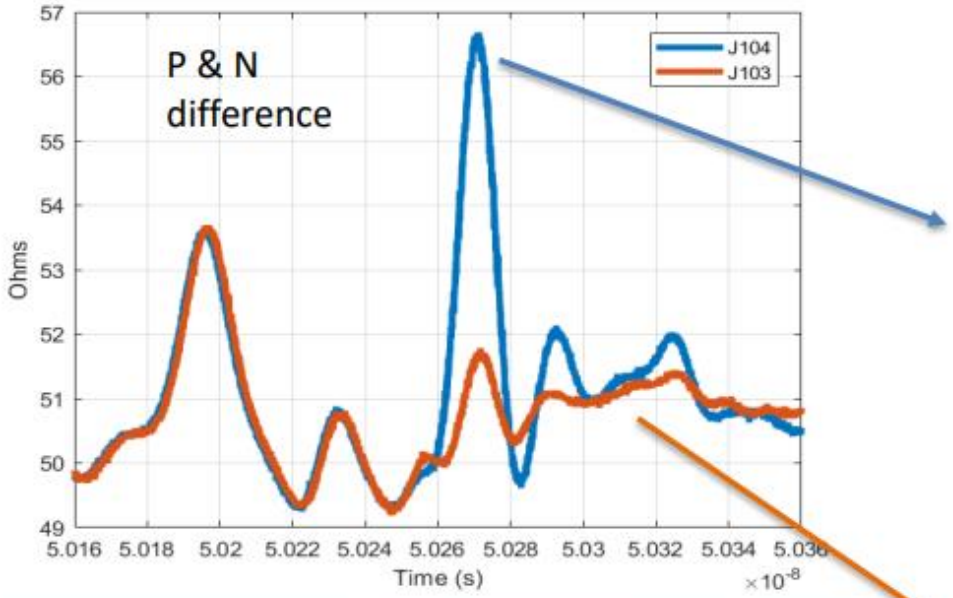
- 3.5mils (more than expected)

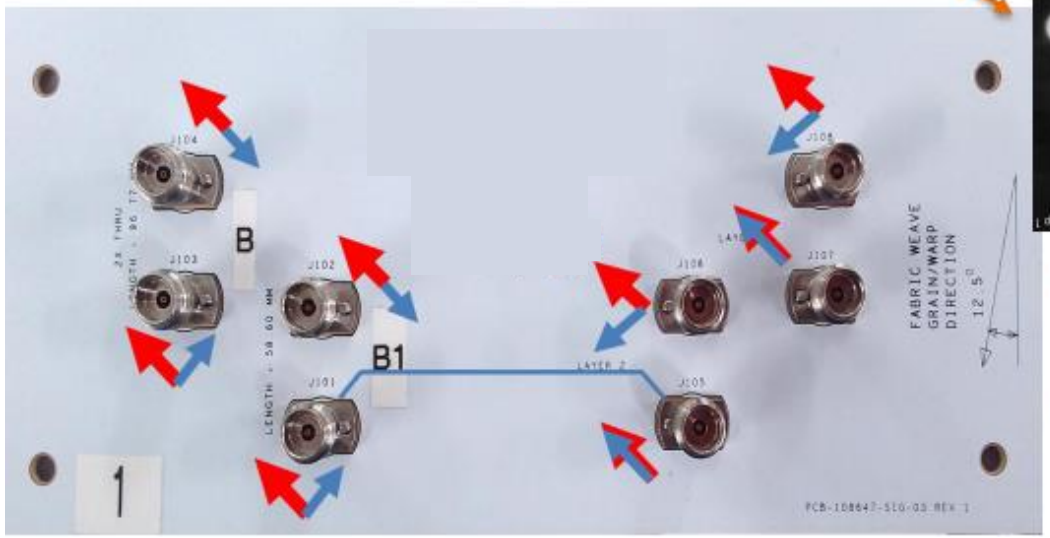
CT Scan of boards show quite a bit of TOP to SIG2 registration



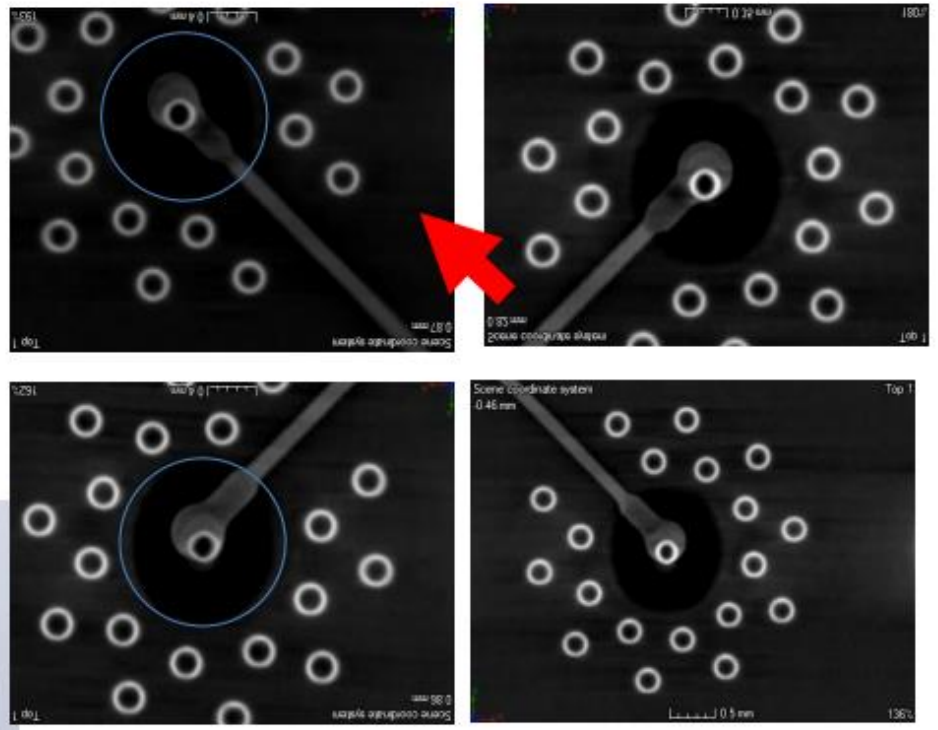
Registration direction

Misregistration: Directional Impact





Layer Registration

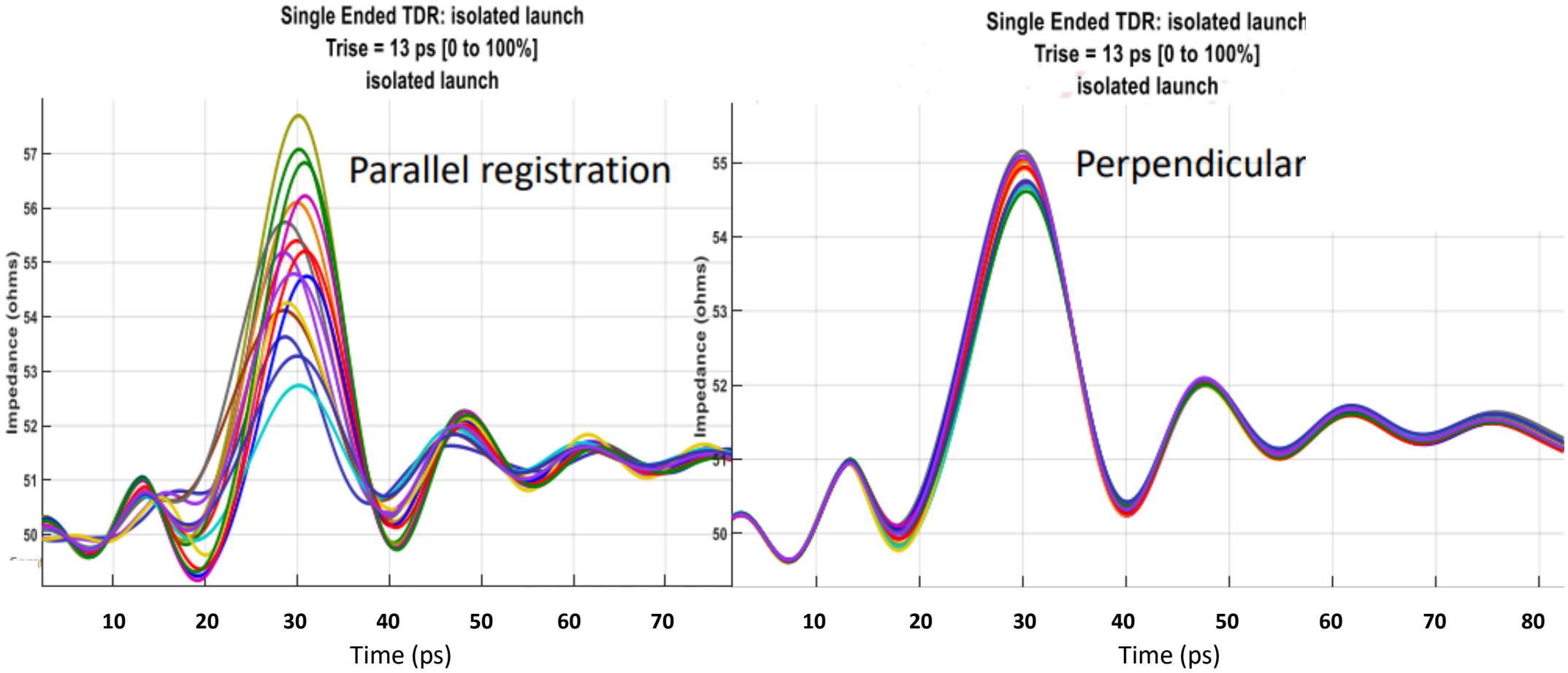


- In cases of misregistration perpendicular to the exit trace, we would expect relatively small impedance effects
- The main impact is from miss registration <u>along the axis</u> of the launch trace exit

Misregistration: Quantifying Impact

TDR VARIATIONS

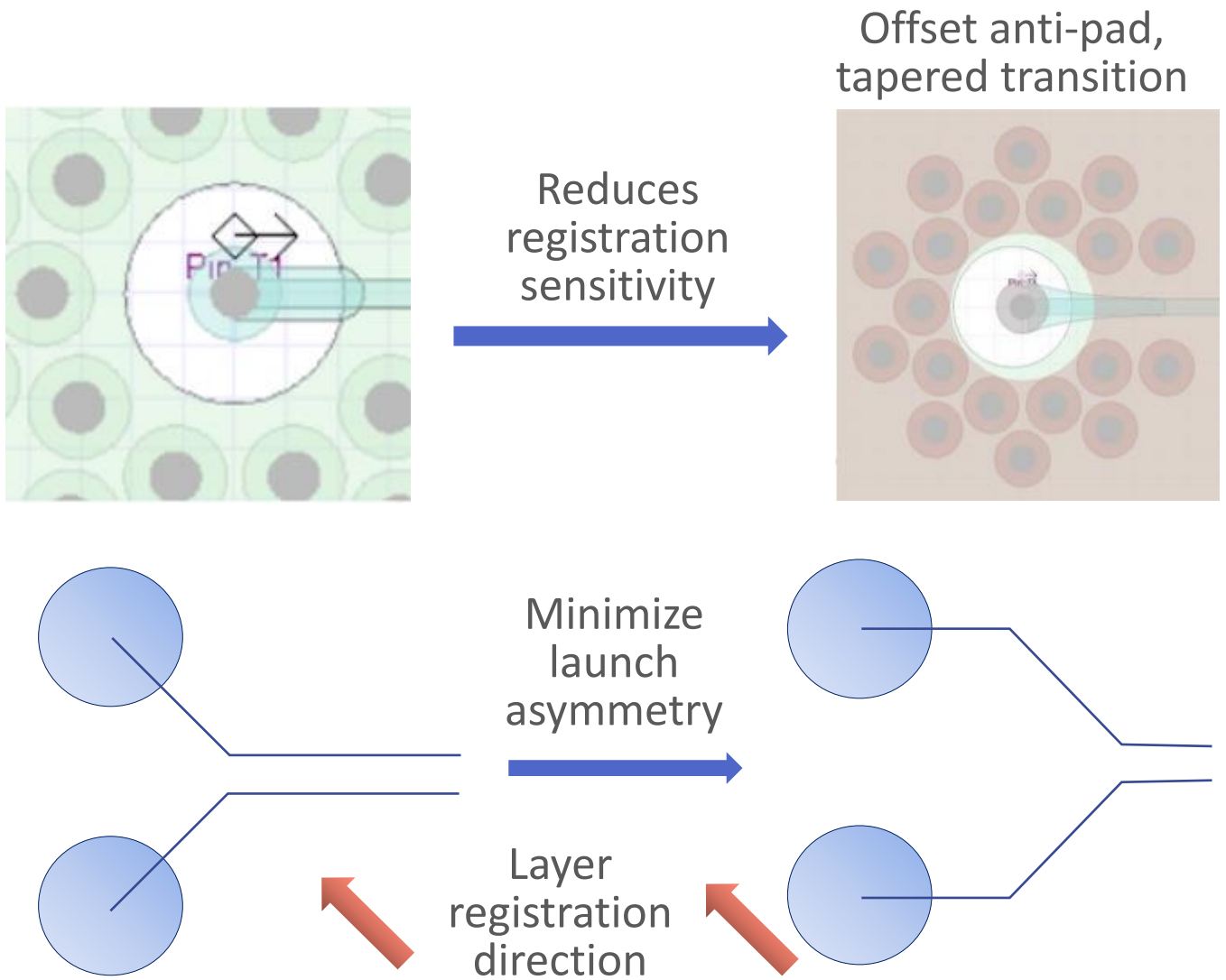
TDR impacts broken out between the P and N launch orientations



Misregistration: PCB Design Improvements

PCB Launch Design Improvements:

- Couple of ideas to improve registration sensitivities and asymmetries
- There are other parameters that can be tweaked to improve on the sensitivity



Section Takeaways

A tapered transformation from via to trace lowers impact of via to etch Misregistration

Minimize launch asymmetry between channels to minimize differences in performance

More details: “Increasing Broadband Interconnect Characterization“, G. Blando, et. al, EDICON 2018

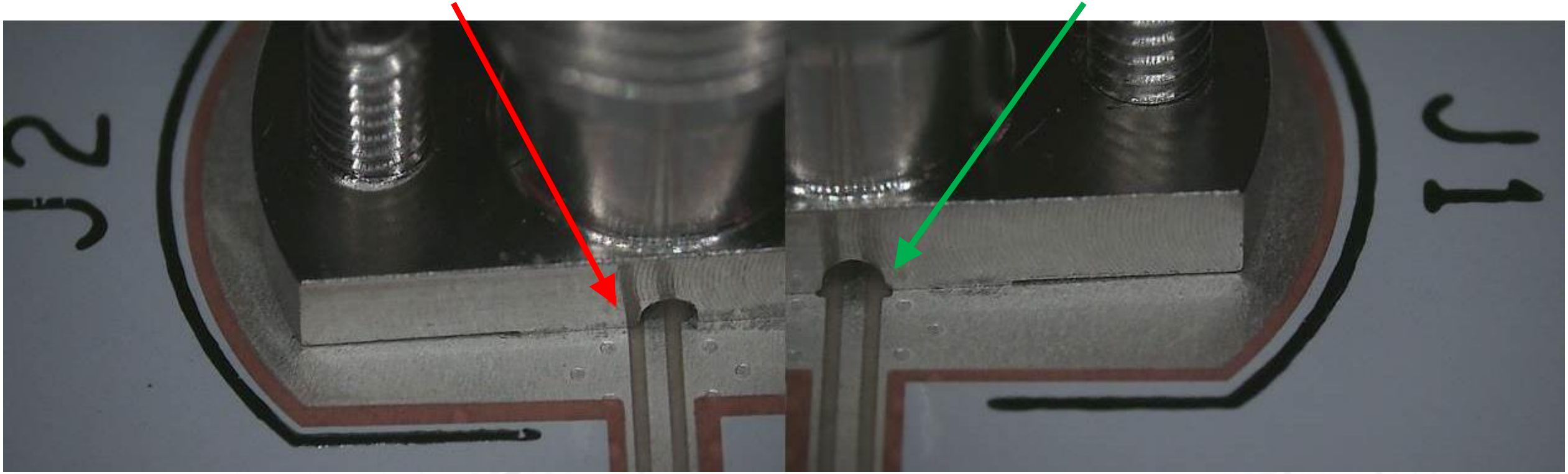
Key Focus Areas for an RF Launch

- Stub impact
- Correct GND ring sizing
- Misregistration compensation
- **Improving assembly processes**

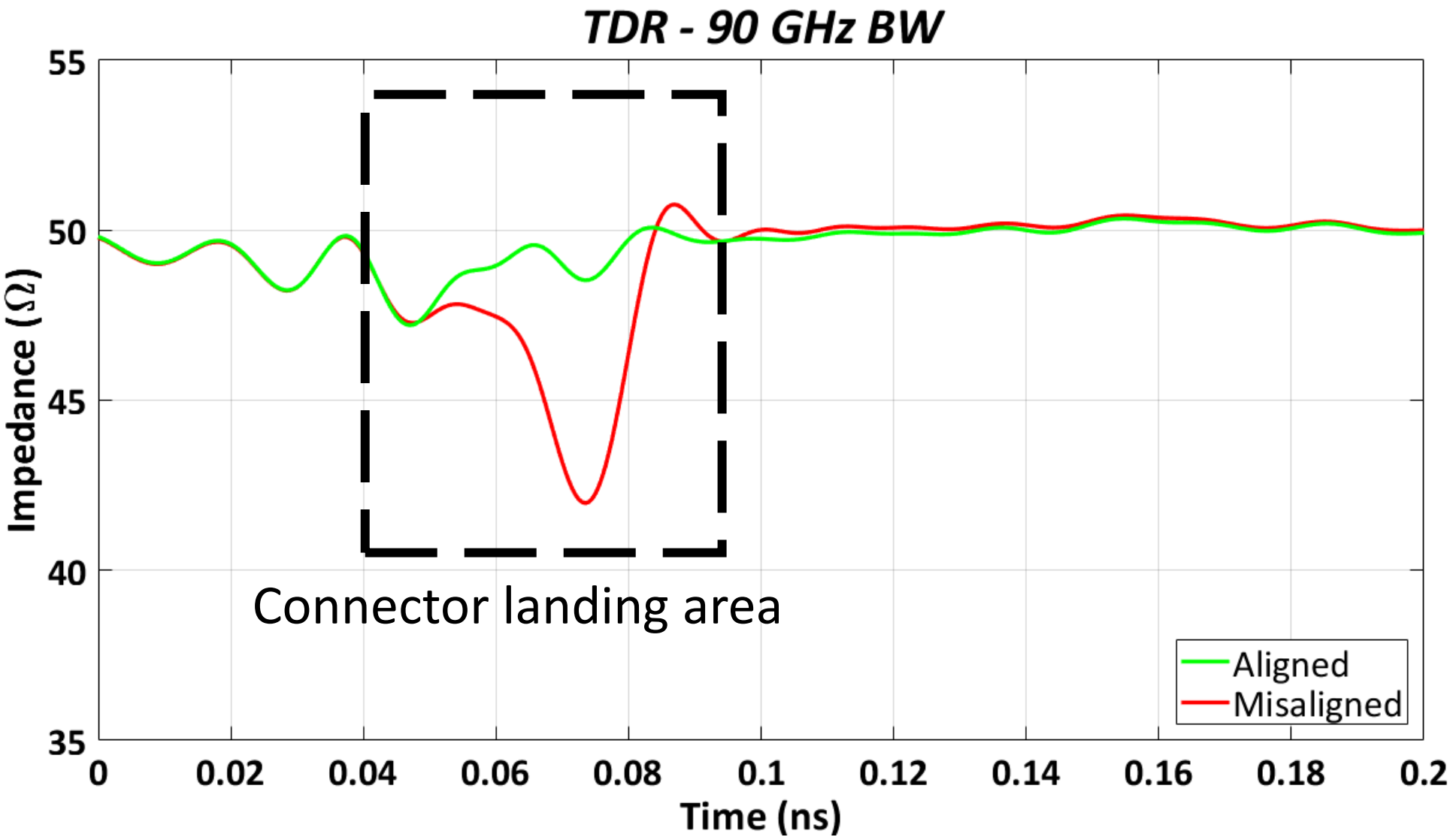
Compression Mount Connector Assembly Issues

Rotational misalignment during assembly

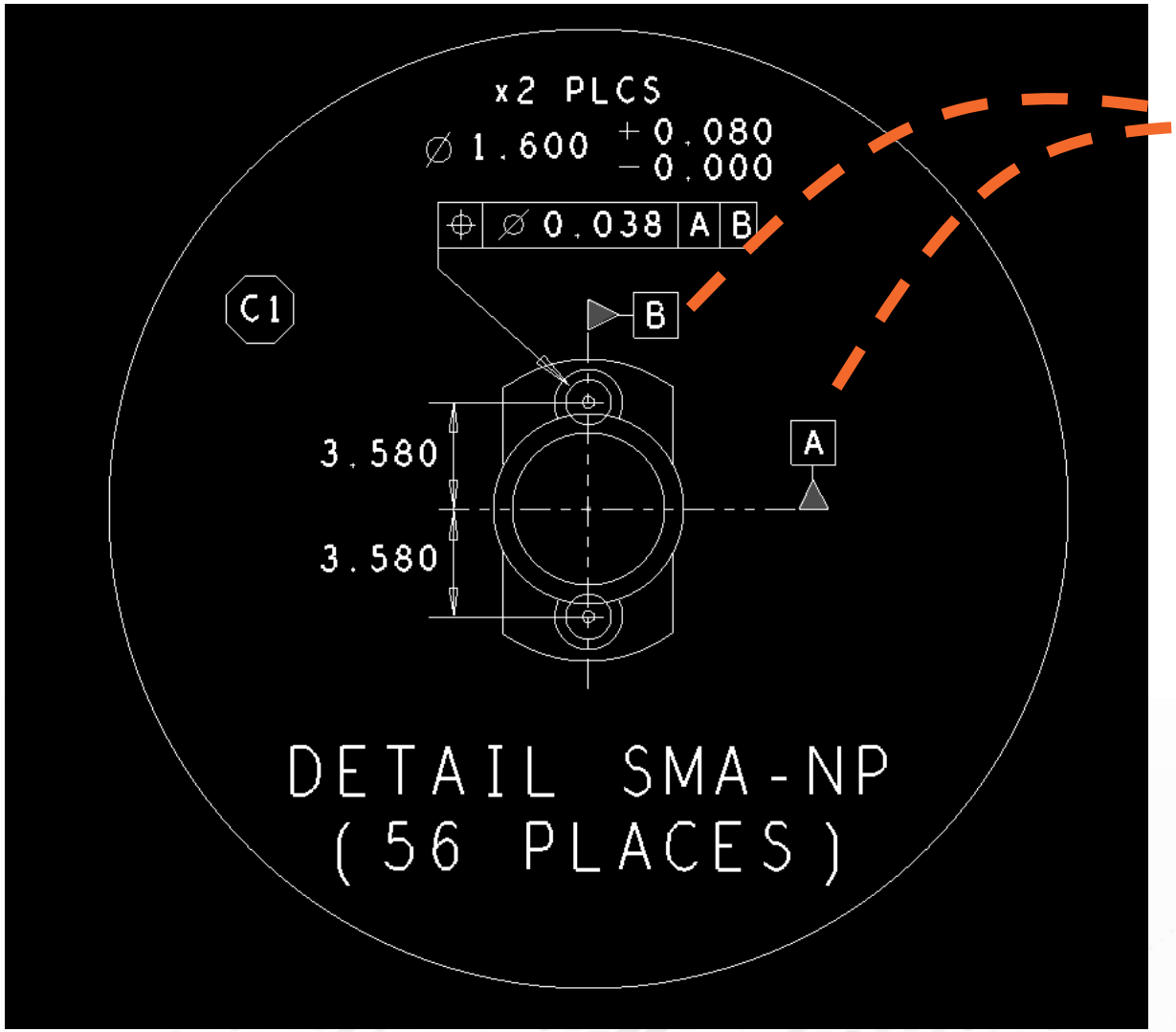
Proper alignment



Compression Mount Connector Assembly Issues

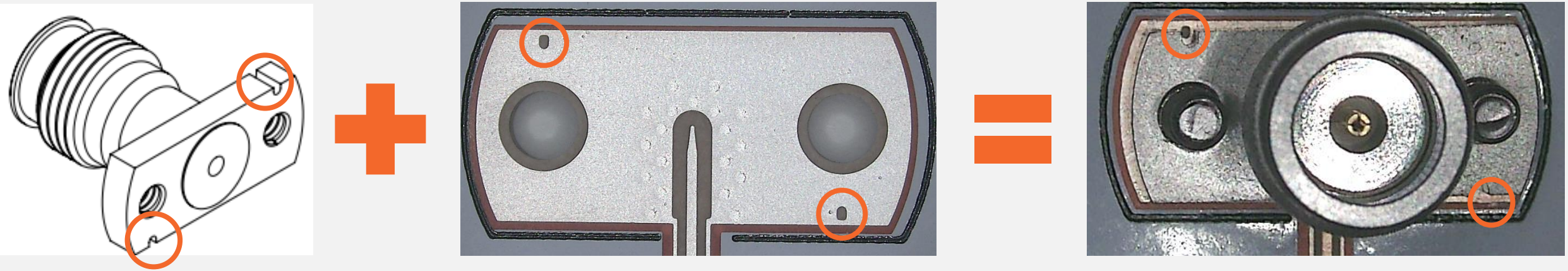


Assembly Issues Mitigation



- Constrain mounting hole position w.r.t landing pad location in X, Y
- Request tight positional tolerance and hole size tolerance
- Use landing pad as reference for hole drilling operation

Assembly Positional Verification



CONCLUSION

- A wide bandwidth connector launch allows devices to stand out from the competition → Don’t rely on just mechanical footprint
- Select small signal via drill size to maximize launch cutoff frequency
- Use short stubs for vias and tight stub length control
- Use tapered transition from via to trace; minimize launch asymmetry
- Align to copper features to minimize assembly variations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