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In PDN, Loss May Be Your Friend, But Inductance Is Your Enemy

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Outline

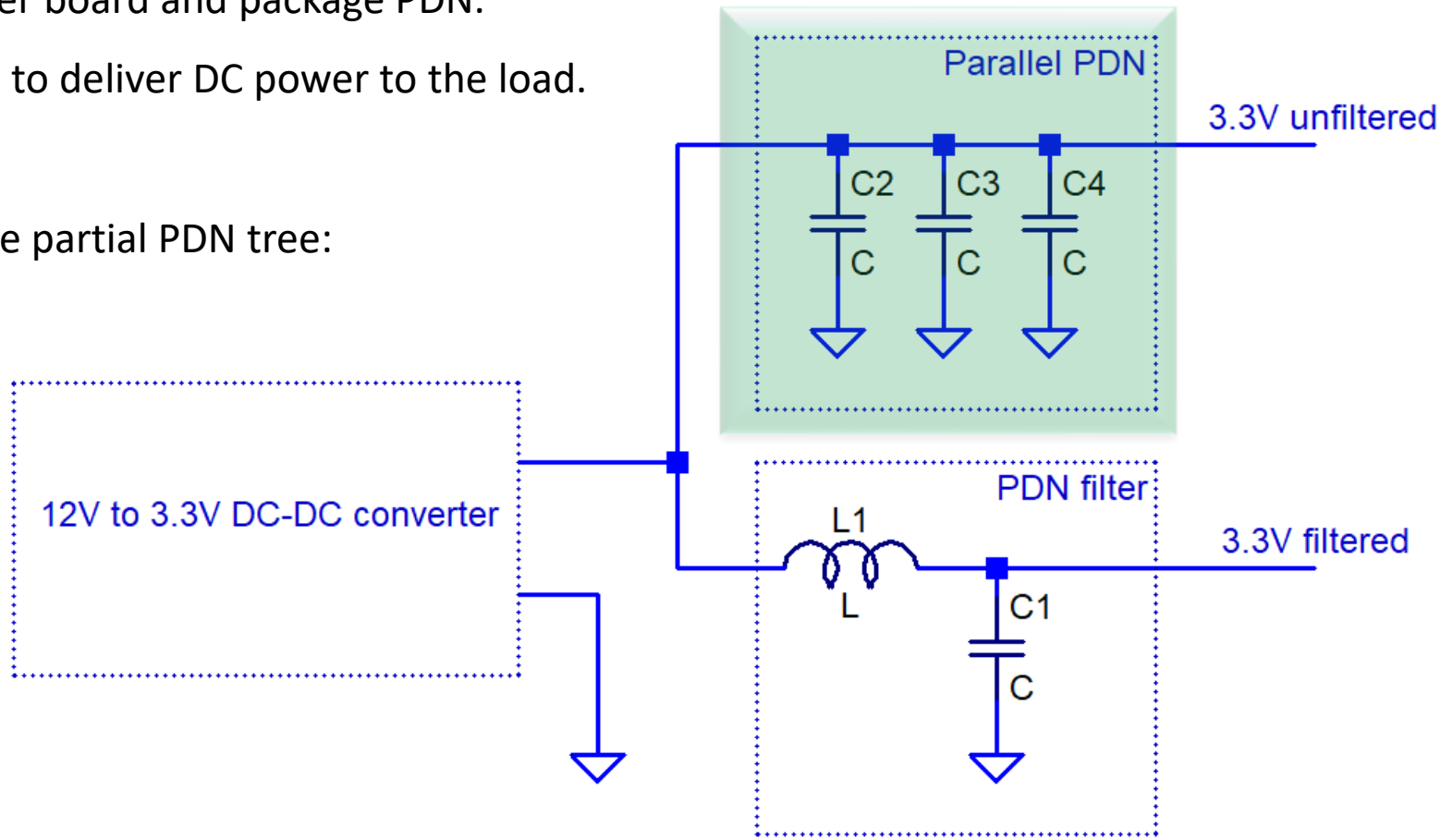
- Defining the scope
- Putting the scope into context
- Cases when we need inductance
- Our goal with parallel PDN
- Impact of inductance on parallel PDN
- Impact of losses on parallel PDN
- Summary

Defining the Scope

We consider board and package PDN.

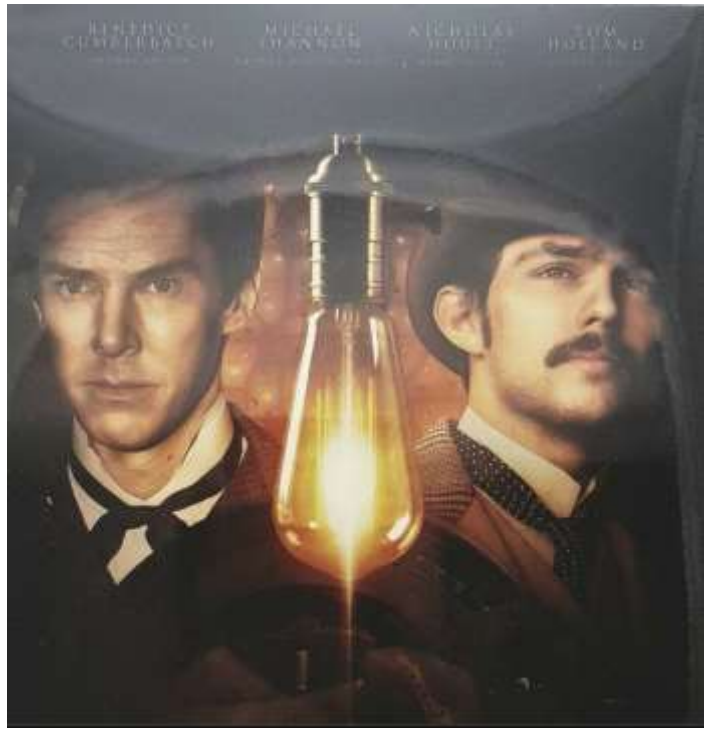
Our goal is to deliver DC power to the load.

An example partial PDN tree:



Putting the Scope into Perspective: The War of Currents

Source: https://www.imdb.com/title/tt2140507/mediaviewer/rm2604388609/



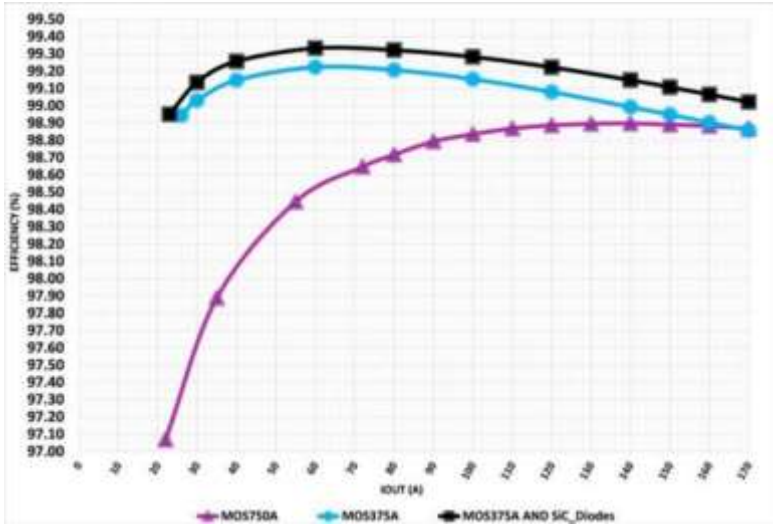
Names to remember:

- Edison, Westinghouse, Tesla
  - DC vs. AC
- Dery-Blathy-Zipernovsky
  - the transformer

- Pros and cons of DC vs. AC
- Why AC won hundred years ago
- Why DC is coming back

The Irony of War of Currents

- If we use HVDC as a source and need low-voltage DC, we still need AC to change voltage
- But DC-DC converters today can have quite high efficiency (approaching 99%)

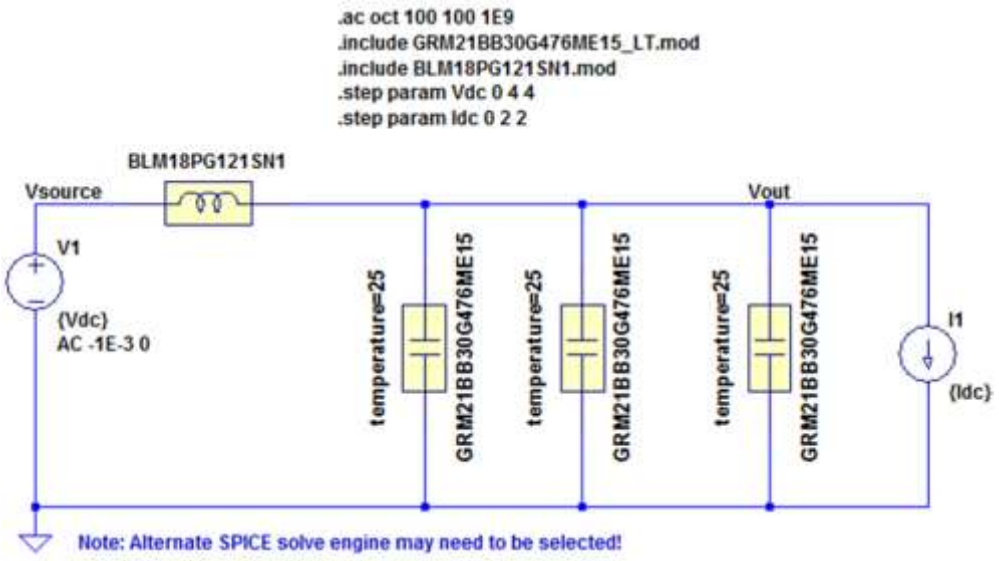


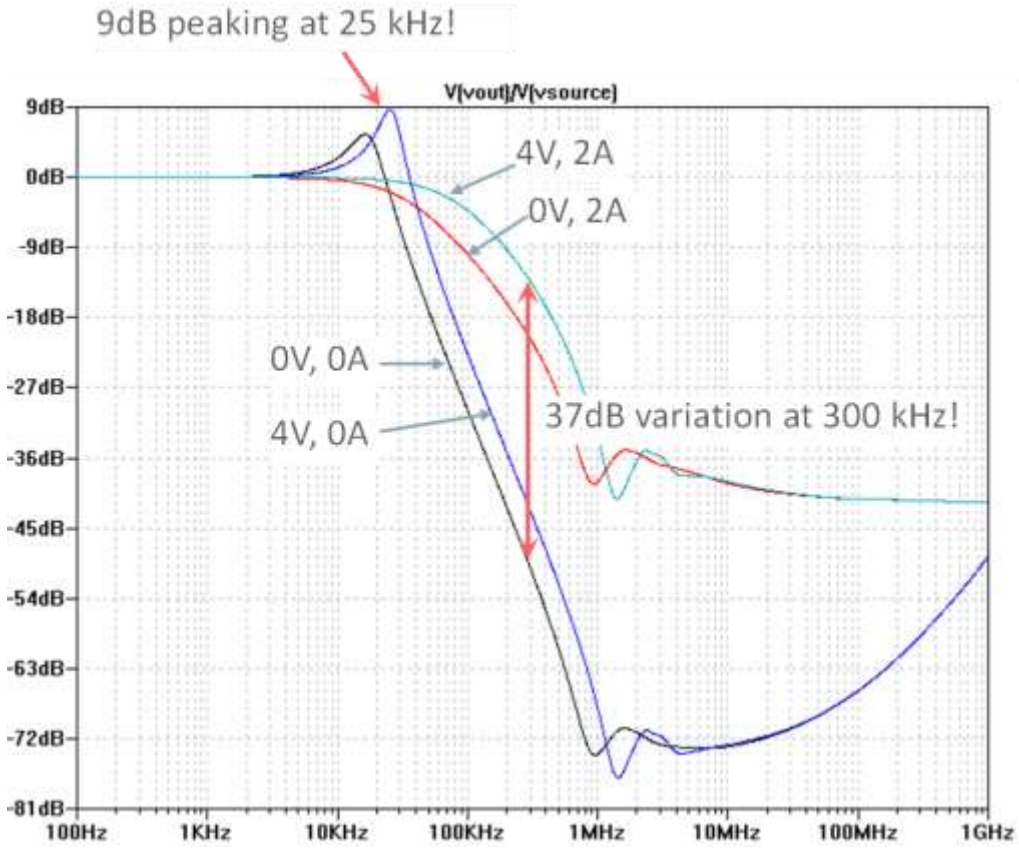
Source: Gustavo Fortes: A resonant DC/DC converter with high efficiency and power
https://www.power-and-beyond.com/a-resonant-dcdc-converter-with-high-efficiency-and-power-a-1030331/

Cases When We Do Need Inductance

LC filters may be useful to block the propagation of AC noise

DC bias impact on LC filter

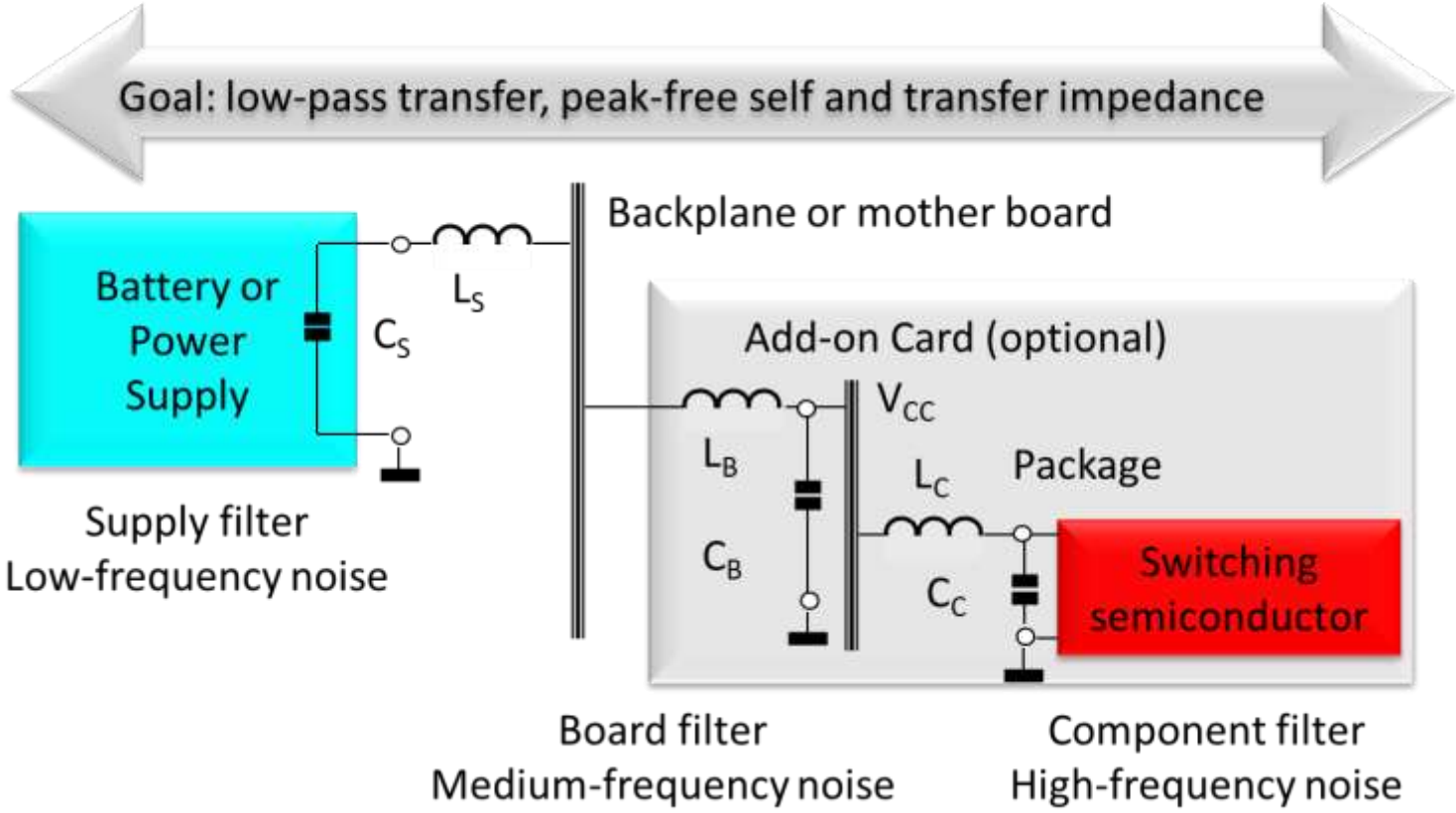




Using Ferrites and Inductors in Power Distribution Networks (PDN), https://blog.samtec.com/12_03_2020_ferrites_inductors_in_pdns/

Parallel PDN: the Goal

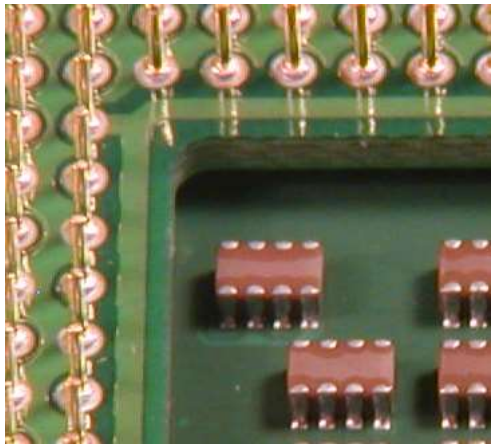
- Generic PDN tree: we want to transmit DC, want to block AC
- Series elements should have low Rdc, can have high Rac
- Parallel elements should have high Rdc, should have optimum Rac



Parallel Elements in PDN

- Voltage source(s)
  - AC-DC converter
  - DC-DC converter
  - Linear regulator
  - Battery

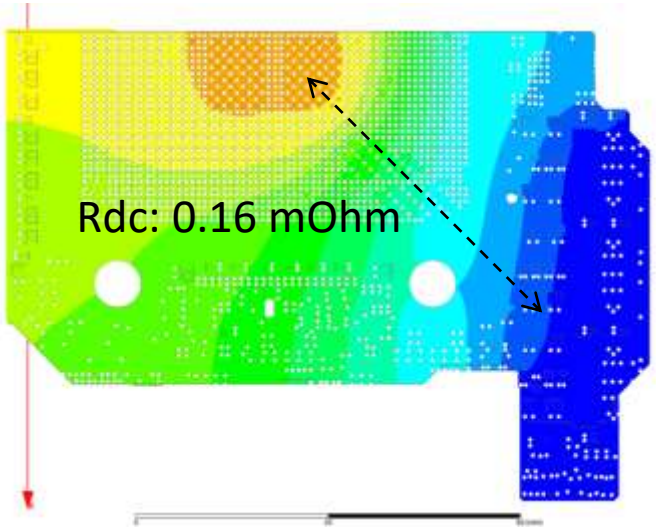
- Capacitors



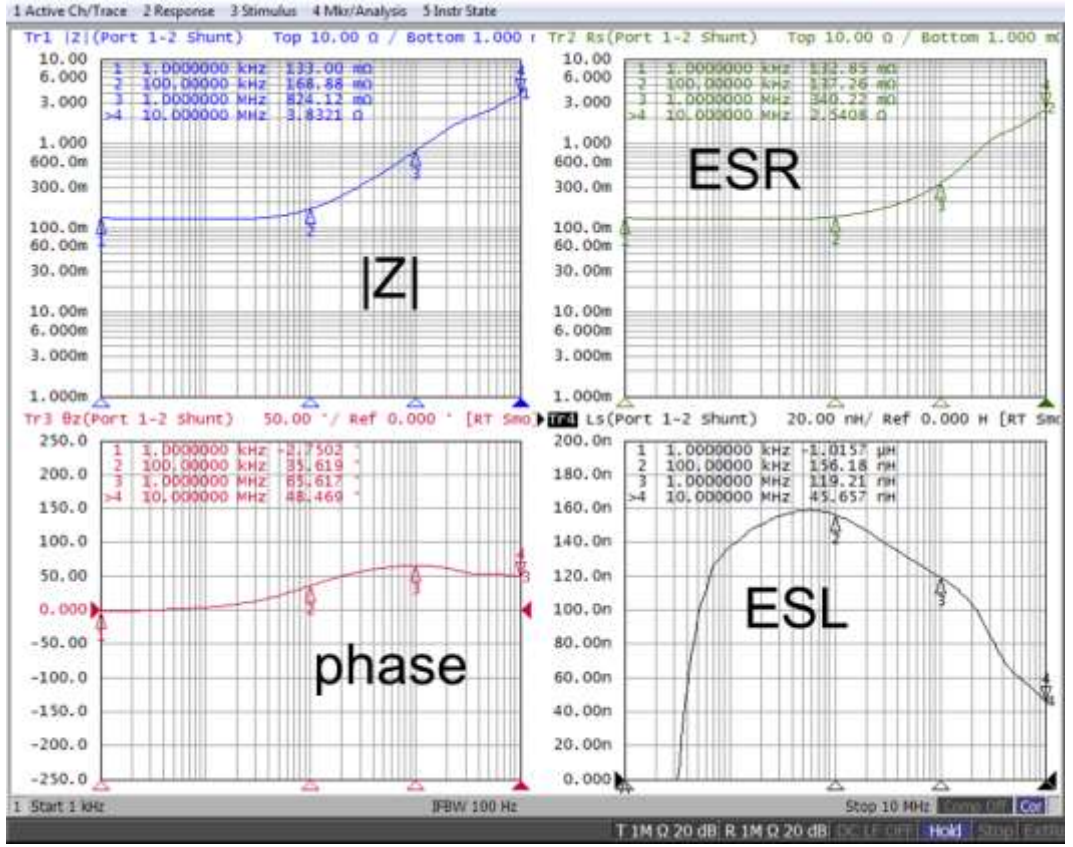
Series Elements in PDN

DC-AC resistance, inductance from

- Output resistance of DC source
- Fuse, series protection device
- **(Inductors, ferrite beads)**
- PCB planes, traces, vias
- Connectors, cables



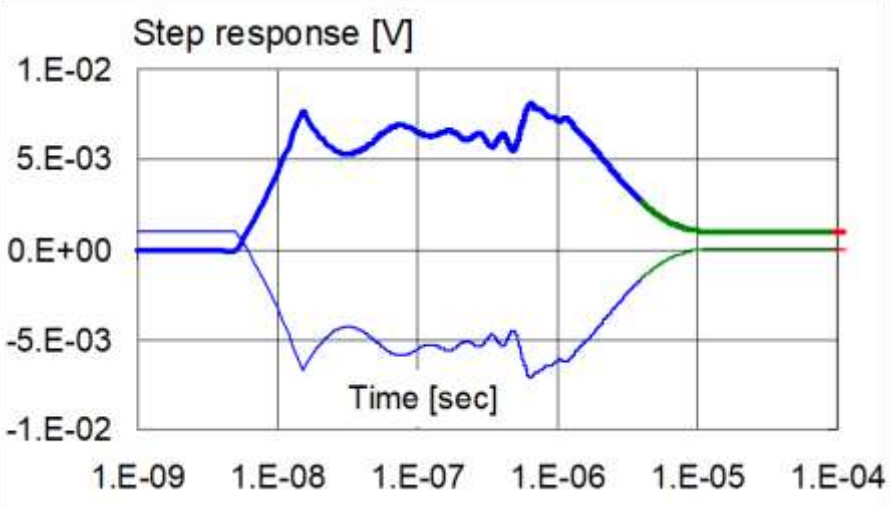
"Etch Factor Impact on SI&PI," DesignCon 2019

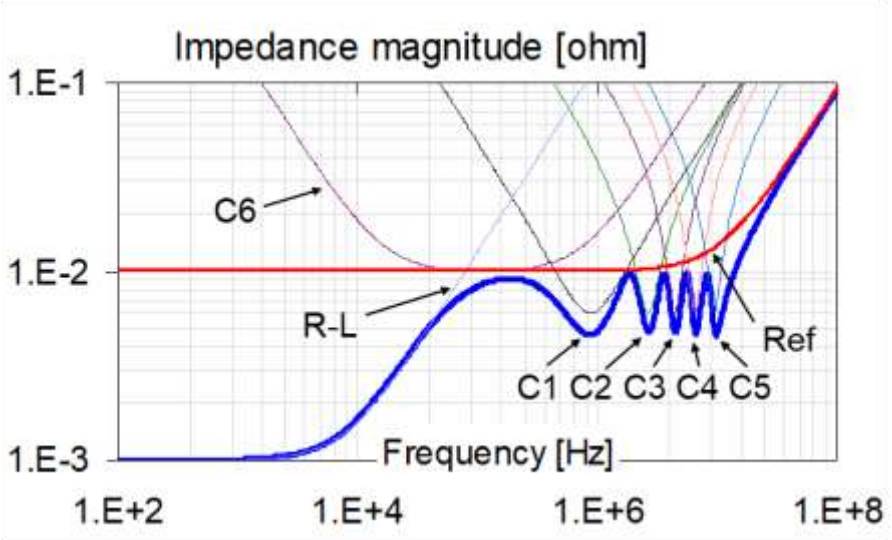


https://blog.samtec.com/05_14_2020_geek_speek_perils_ra_turns/

Our Goal with Parallel PDN

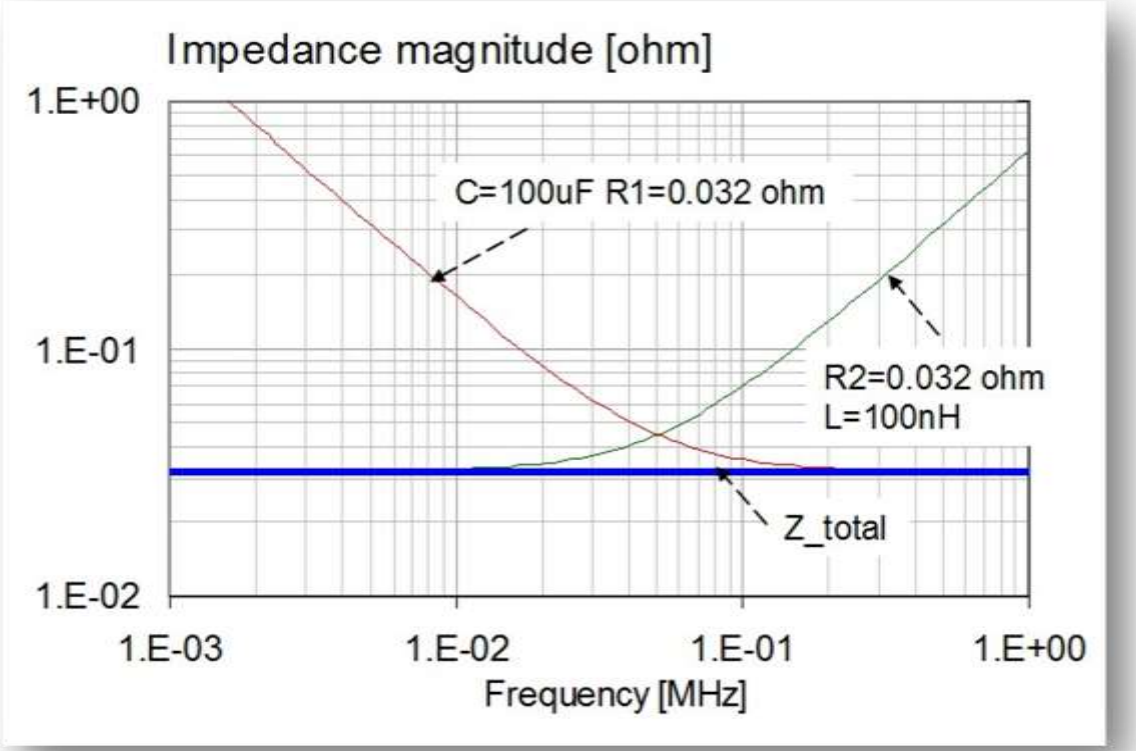
- Noise voltage should be within allowed limits
- Transient noise in LTI PDN for arbitrary load steps can be minimized by achieving
  - Monotonic step response, or
  - Flat PDN impedance





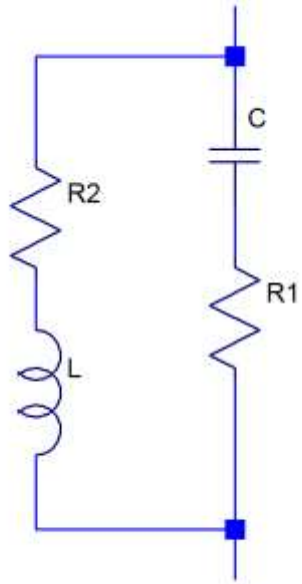
Starting with Ideal PDN

- Flat impedance requires AC (and DC) resistance



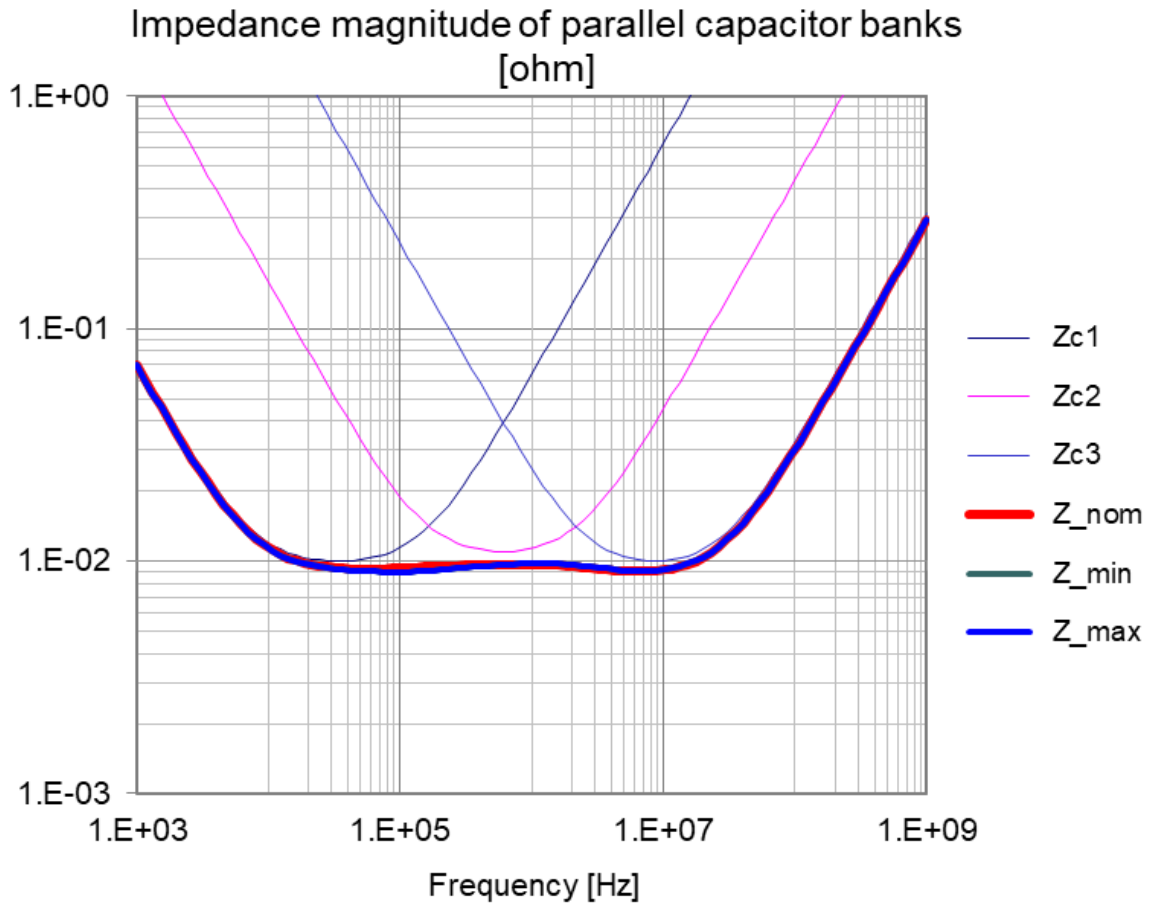
Discrete Impedance Matching:

$$\sqrt{\frac{L}{C}} = R_1 = R_2$$

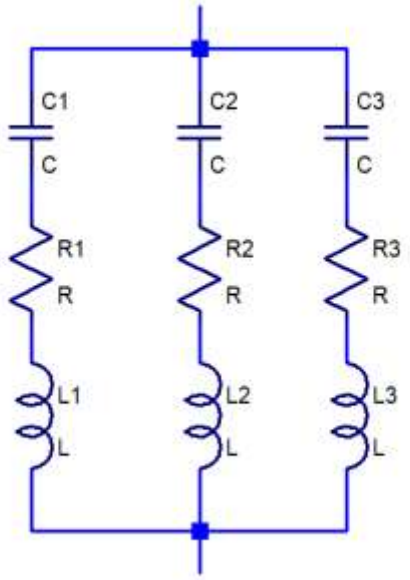


A More Realistic PDN

Three capacitor banks providing flat impedance



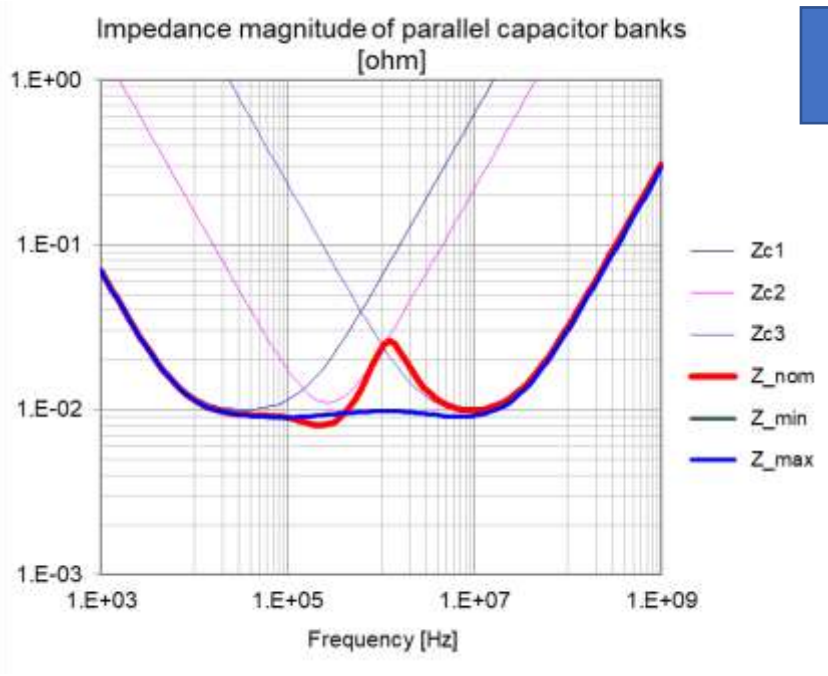
C1 bank
2200uF 10mOhm 10nH
C2 bank
100uF 11mOhm 0.7nH
C3 bank
6.8uF 10mOhm 50pH



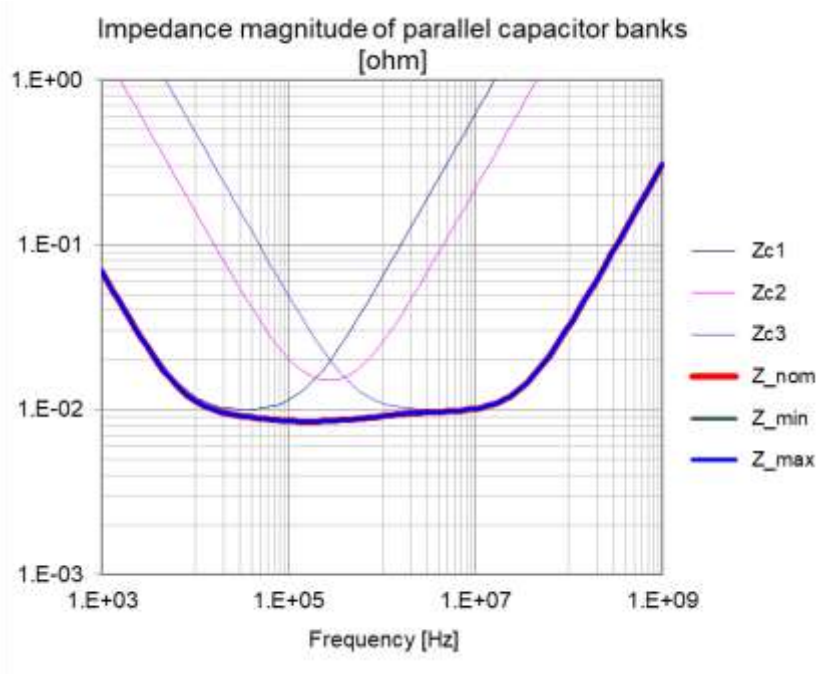
Excess Inductance

To compensate for excess inductance, we need more capacitance

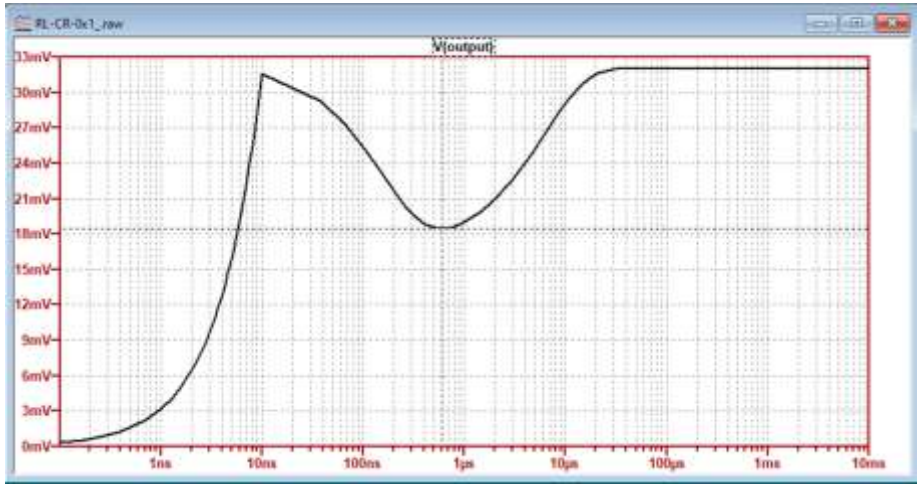
C1 bank
2200uF 10mOhm 10nH
C2 bank
100uF 11mOhm 3.5nH
C3 bank
6.8uF 10mOhm 50pH

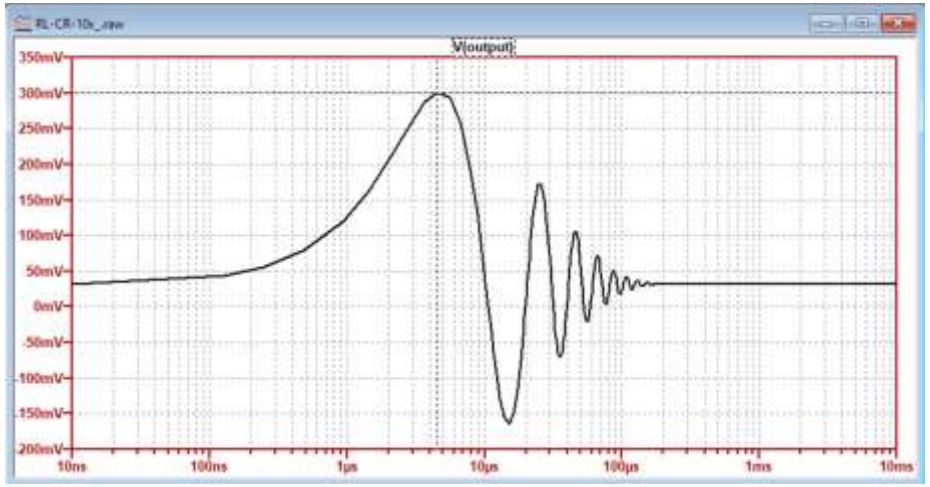


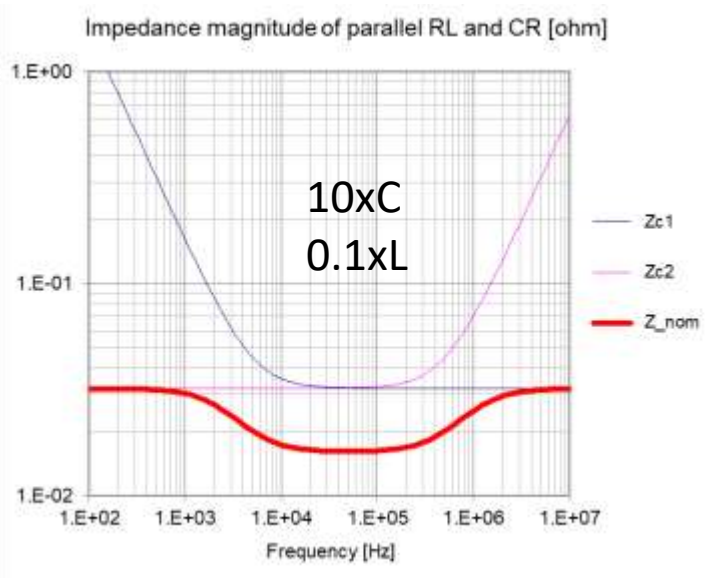
C1 bank
2200uF 10mOhm 10nH
C2 bank
100uF 15mOhm 3.5nH
C3 bank
33uF 10mOhm 50pH



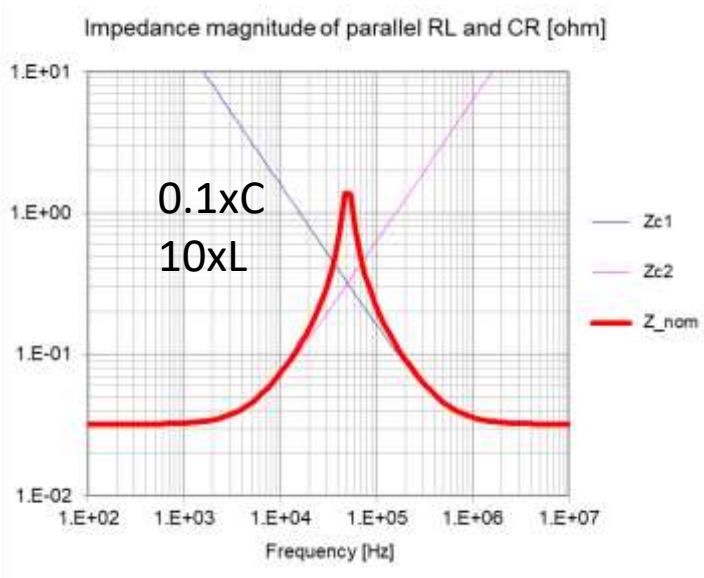
Is There Such a Thing As Too Much Capacitance or Too Little Inductance?







WC noise:
1.9x
Saturated

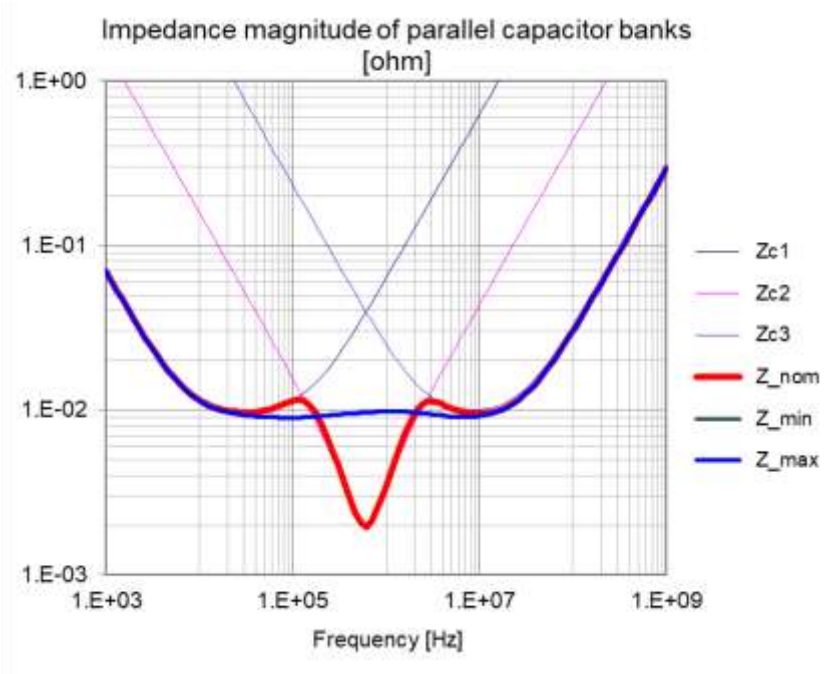


WC noise:
61x
No bound

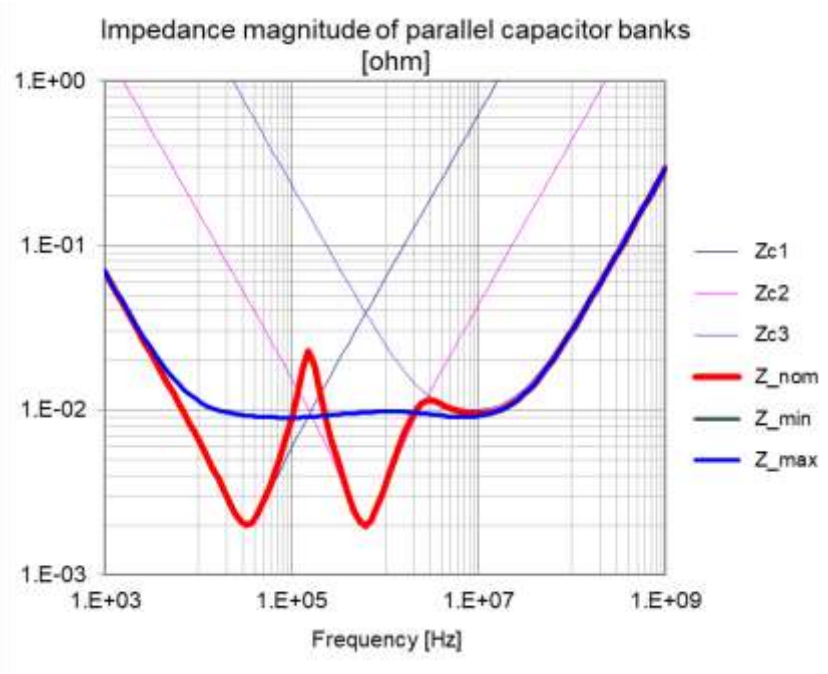
Non-Optimum Resistance

Non-optimum resistance increases impedance peak magnitudes

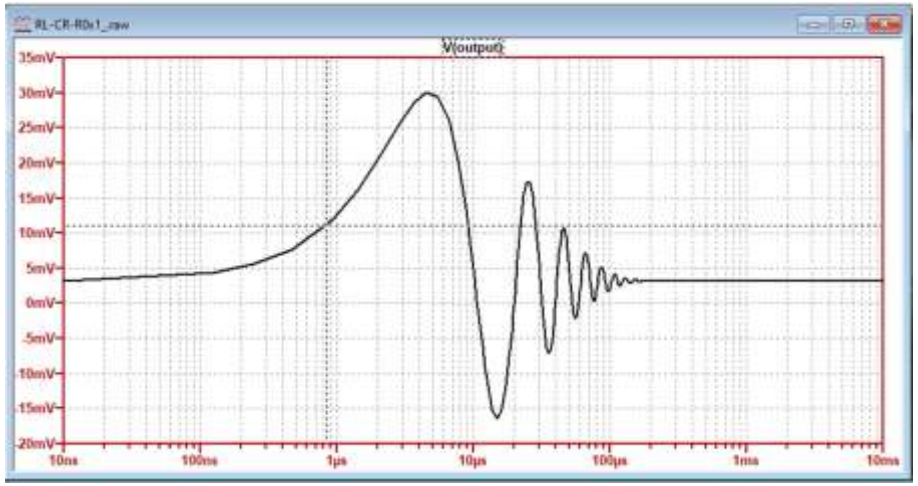
C1 bank
2200uF 10mOhm 10nH
C2 bank
100uF 2mOhm 0.7nH
C3 bank
6.8uF 10mOhm 50pH

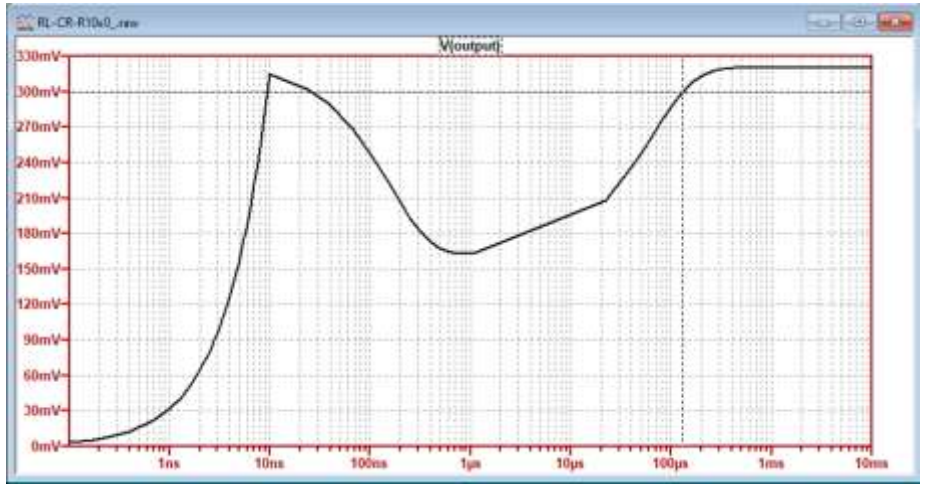


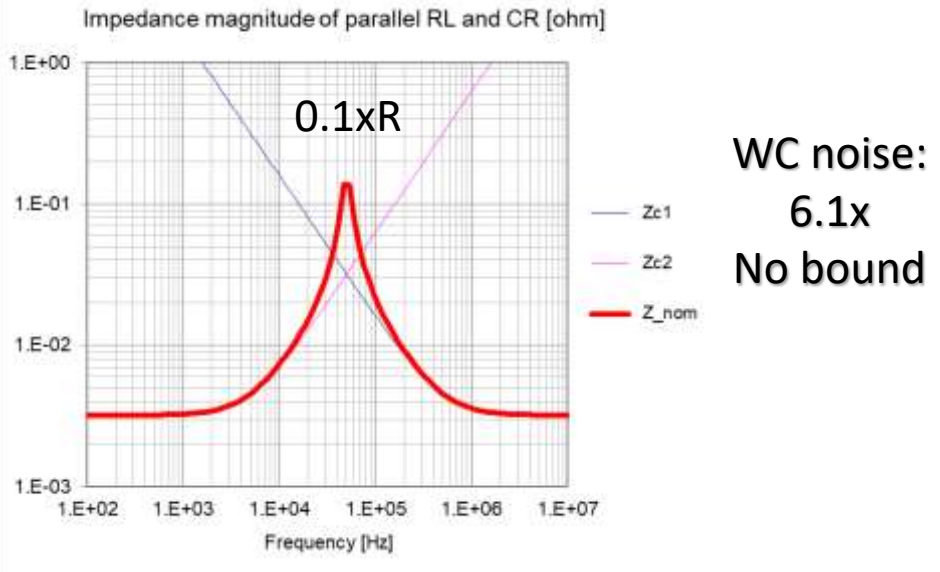
C1 bank
2200uF 2mOhm 10nH
C2 bank
100uF 2mOhm 0.7nH
C3 bank
6.8uF 10mOhm 50pH



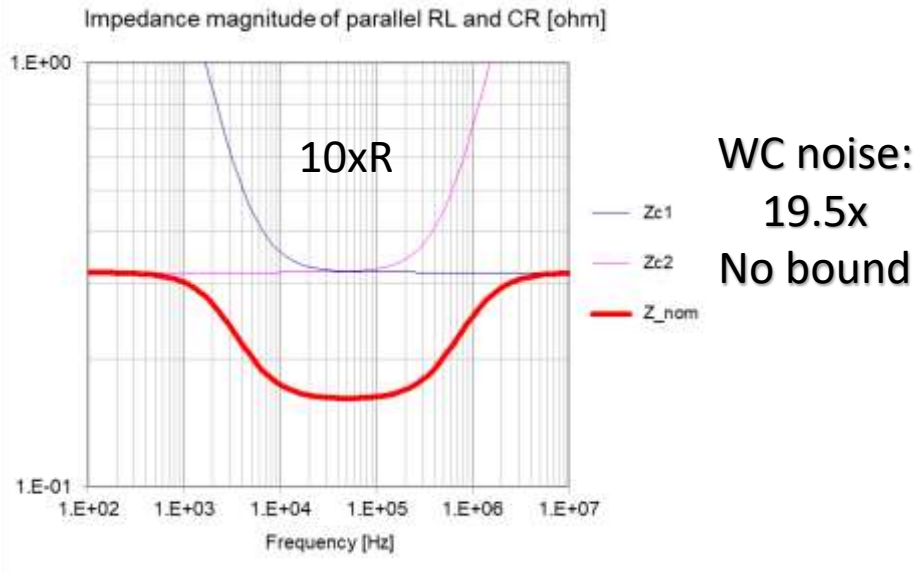
Worst-Case Noise with Non-Optimum Resistance







WC noise:
6.1x
No bound



WC noise:
19.5x
No bound

Summary and Conclusions

- PDNs in DC distribution systems should pass DC and block/attenuate AC
- In parallel PDNs monotonic step response or flat impedance minimizes worst-case transient noise
- Excess inductance can be compensated for by more capacitance
- Non-optimum resistance (either higher or lower) increases noise with no bound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