samtec

gEEk® spEEk

Key Development Steps of 112 Gbps PAM4 Test Platforms

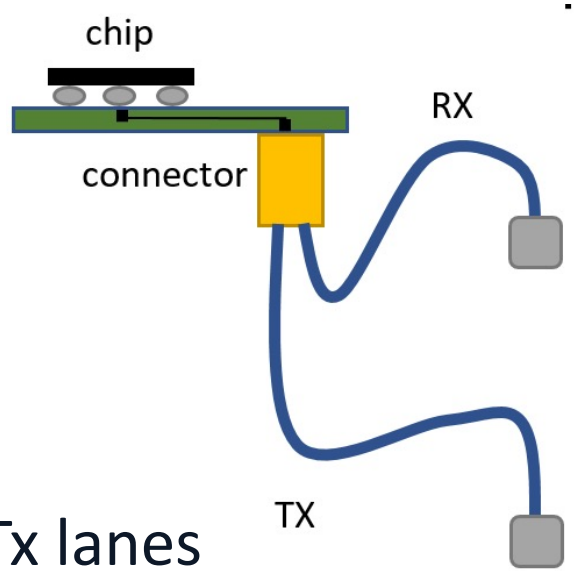
Jean-Remy Bonnefoy

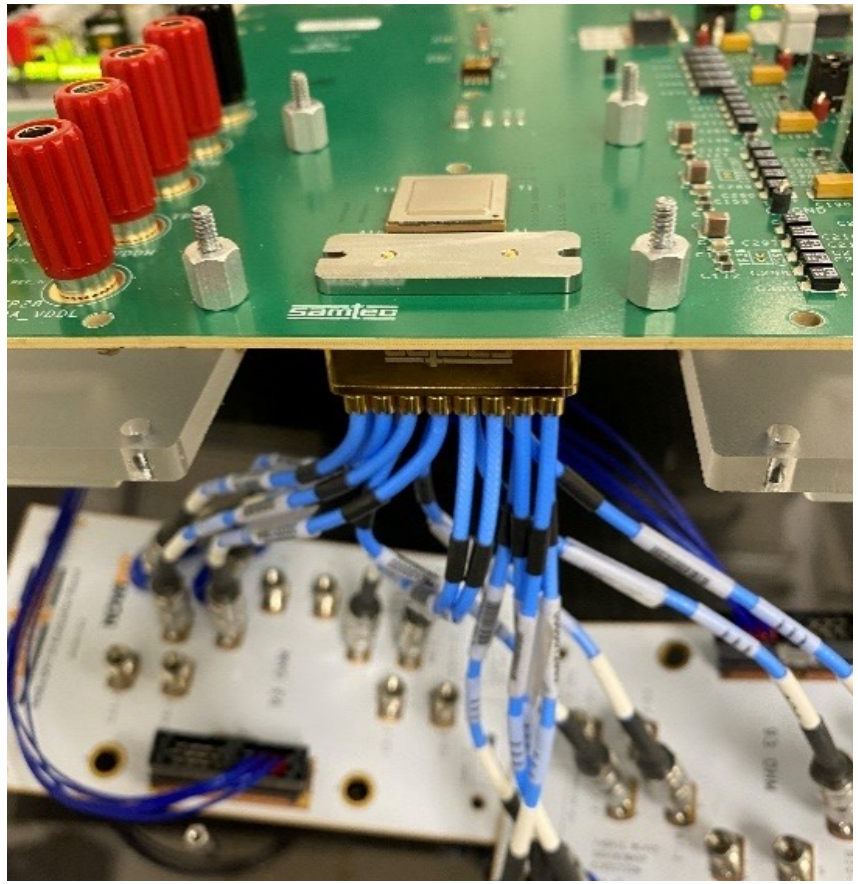
Introduction and Outline

- With great data rate comes great responsibility
  - At 112G-PAM4 optimization for loss, reflections, crosstalk and power integrity needs extra care
- Case study of an evaluation board that uses 112G-PAM4 silicon and connector
  - Optimizing a 112G test channel
  - Power delivery network design process
  - A look at the channel performance
  - Lessons learned

Optimizing a 112G-PAM4 Test Channel

- The Channel:
  - Top mounted BGA
  - Bottom mounted connector
    - Thermal/Mechanical constraint
  - 6" low loss coax cables



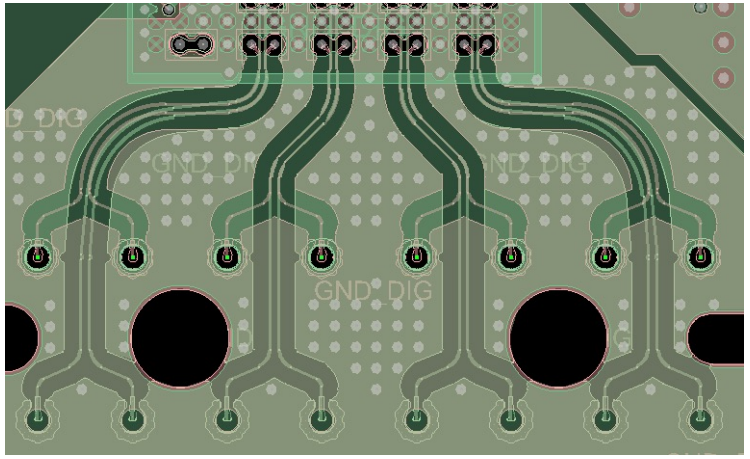


- 3 dB total IL at 28 GHz for Tx lanes
- Use affordable, readily available material

PCB Design

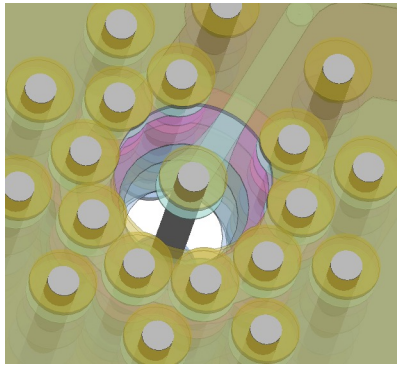
- Stack-up:
  - I-Tera MT40
  - Core out construction
  - Dielectric with 1067 weave
- Impedance:
  - 90 Ohm package / 50 Ohm single ended coax cables
    - 92 Ohm BGA escape and open routing
- Routing:
  - Two routing layers (RX, TX)
  - Short TX traces, 11 mm
  - Board rotation to mitigate periodic fiber weave effects

Layer	Calc Thickness	Primary Stack	Description	Dk / Df
	0.0010		Taiyo 4000-MP	3.60 / 0.0190
Layer - 1	0.0026		1/2oz Mix (Std Plt)	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 2	0.0006		1/2oz Sig	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 3	0.0006		1/2oz P/G	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 4	0.0006		1/2oz Sig	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 5	0.0006		1/2oz P/G	
	0.0140	0.0140 (2-2116/1-3313)	I-Tera MT40	3.56 / 0.0033
Layer - 6	0.0006		1/2oz P/G	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 7	0.0006		1/2oz Sig	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 8	0.0006		1/2oz P/G	
	0.0052	1067 - 76% / 1067 - 76%	I-Tera MT40	3.08 / 0.0020
Layer - 9	0.0006		1/2oz Sig	
	0.0050	0.0050 (2-1067)	I-Tera MT40	3.17 / 0.0023
Layer - 10	0.0026		1/2oz Mix (Std Plt)	
	0.0010		Taiyo 4000-MP	3.60 / 0.0190

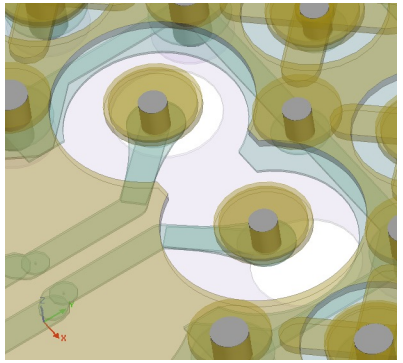


Via Breakout Optimization

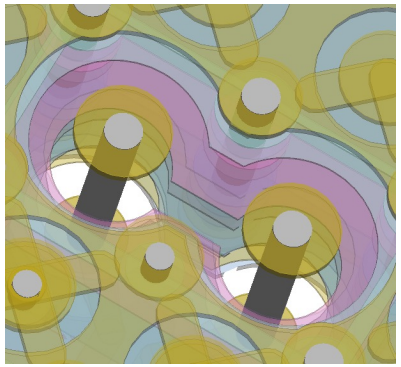
- Topology:
  - Top-mounted BGA / Bottom-mounted connector
  - CDD and through vias, inherent minimal stubs
- Optimized via design:
  - Auxiliary ground vias
  - Teardrops
  - Offset ground relief on lower reference plane



Connector via



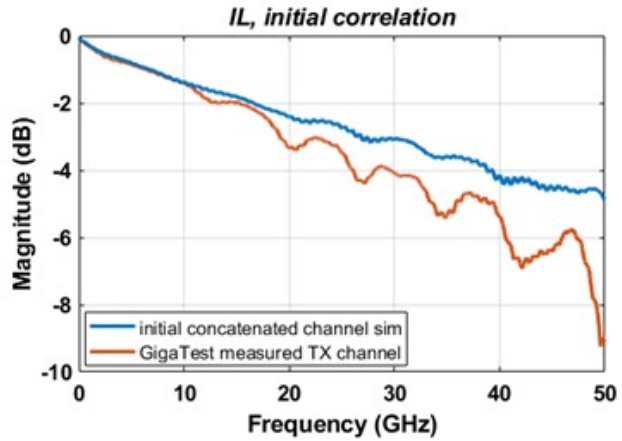
CDD via

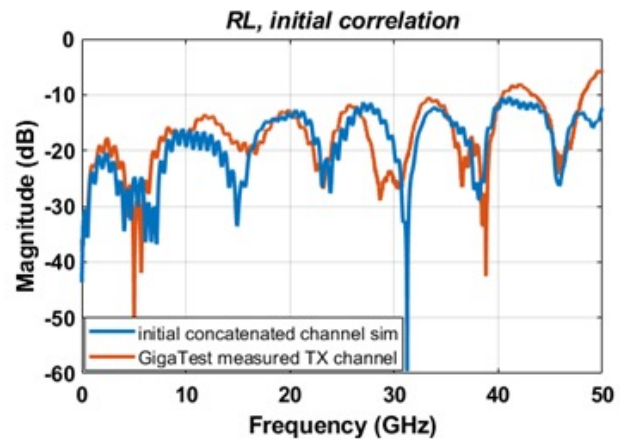


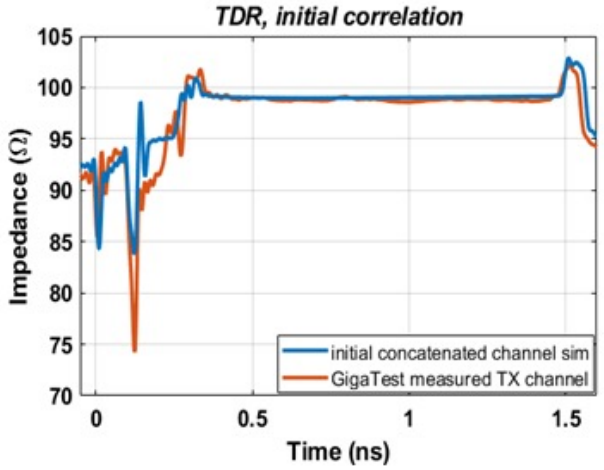
Thru via

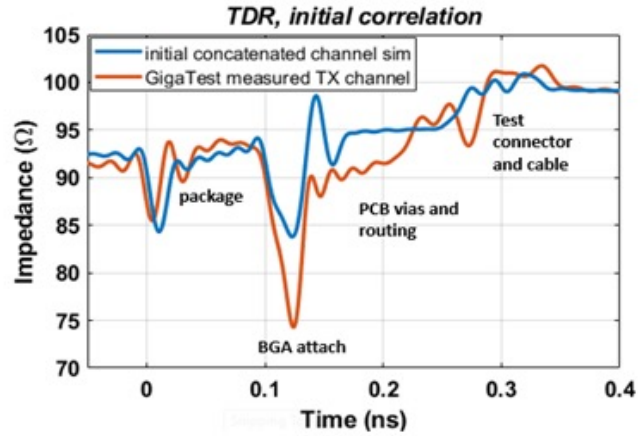
Initial Simulations and Measurements

- Concatenated 4-port channel:
  - Extracted package layout
  - Simulated GL102 dielectrics
  - Vias, PCB and cabling simulated separately
- Measurements:
  - Bare-die BGA package
- Miscorrelation:
  - Under-modeled impedance discontinuities
  - Missing resonances in the IL



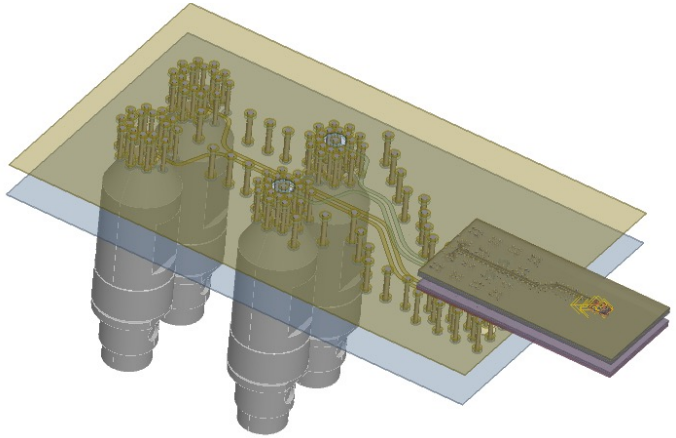




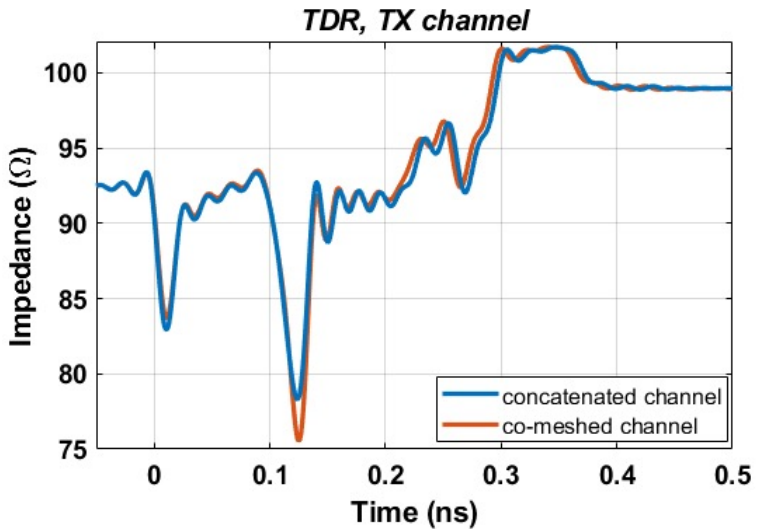


Examining Root Cause

- Deep dive simulation review:
  - Package vias pads and diameters
  - Package copper roughness
  - PCB thru vias tolerance
  - Connector model initially truncated
  - Improved co-meshed simulation

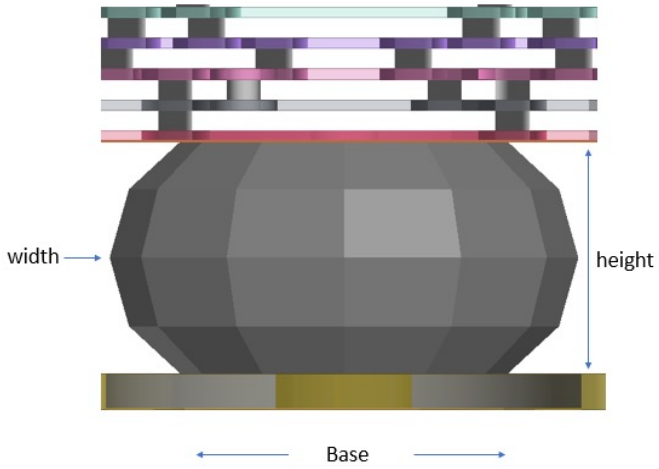


Combined co-meshed simulation model

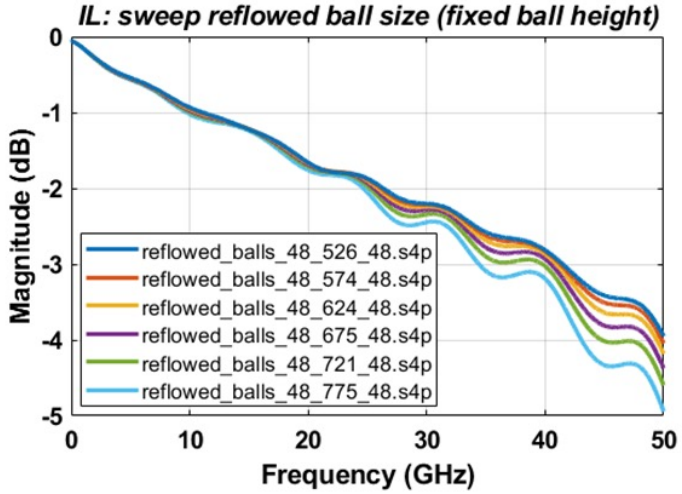


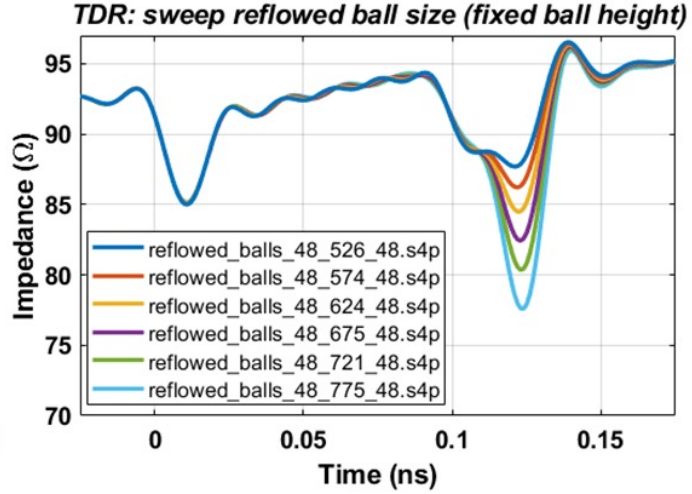
Solder Ball Model Sweep

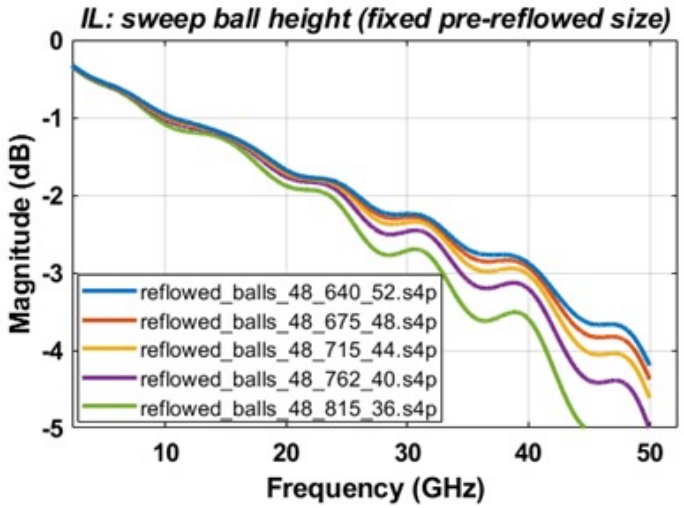
- Reflowed ball size (width) sweep

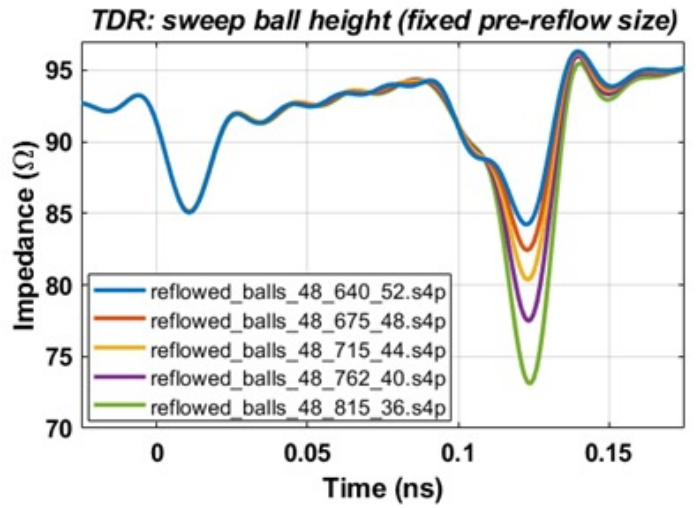


- Ball shape (height) sweep
  - More predictive of TDR discontinuities



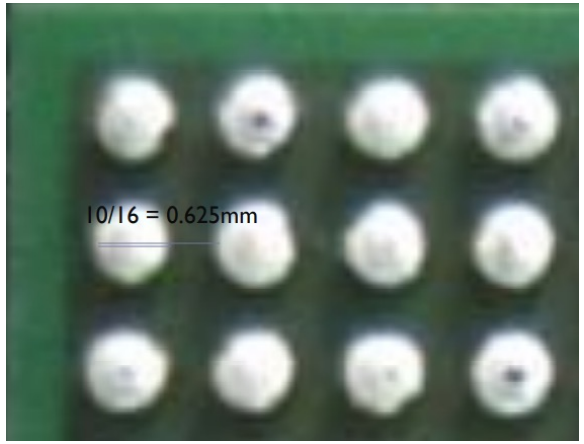






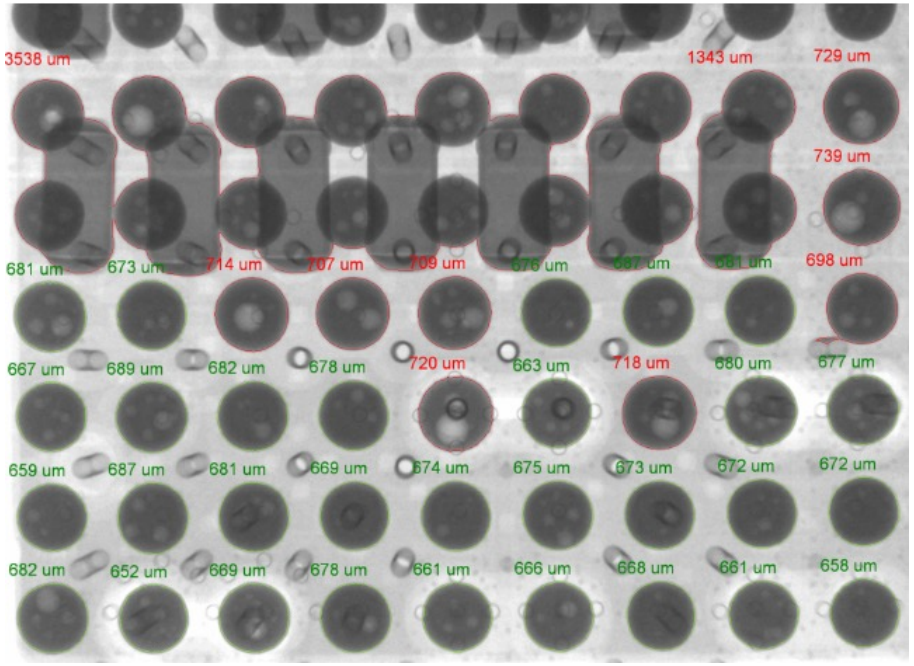
Reflowed Ball Size Approximation

- Pre-reflowed size measurements
- Wide range of reflowed ball shapes
- CT-scan and feeler gauge



Pre-reflow solder ball

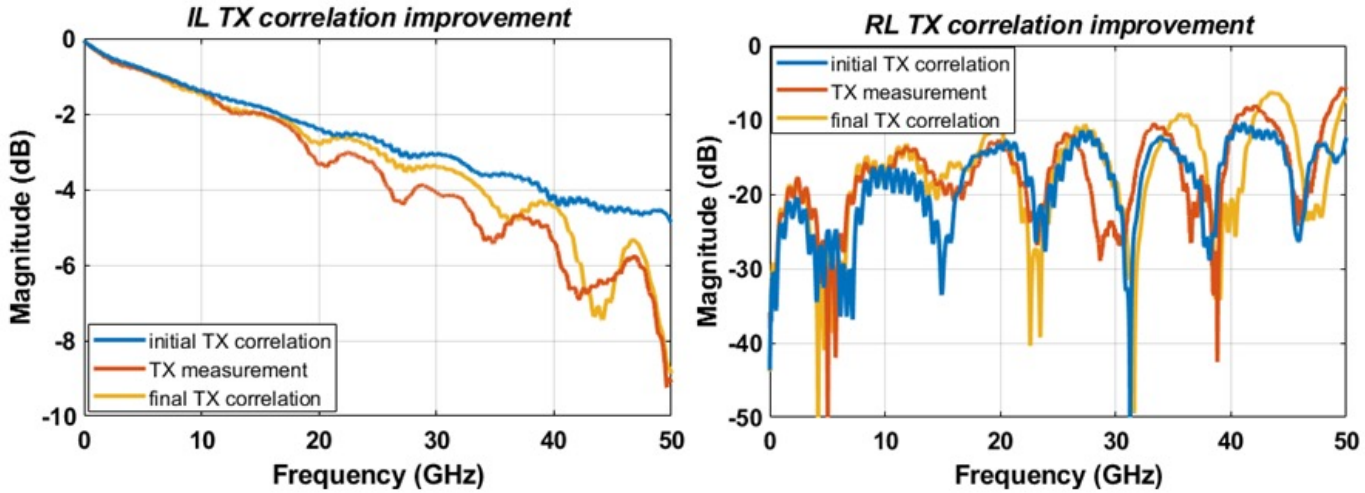
Real solder ball shapes

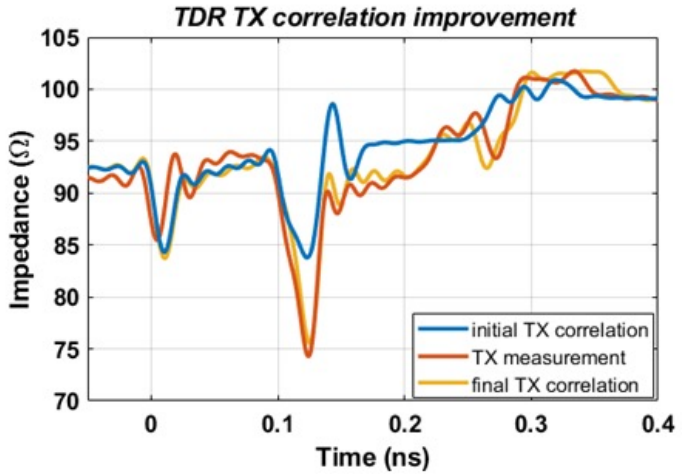


CT-scan of soldered BGA

Improved Correlation

- Co-meshed simulation:
  - Trace impedance updates
  - Improved reflowed solder ball model
- Correlation:
  - Still missing some IL resonance at higher frequencies
    - Ball model approximation
    - Die probe calibration impact
    - Small uncertainty in VNA accuracy



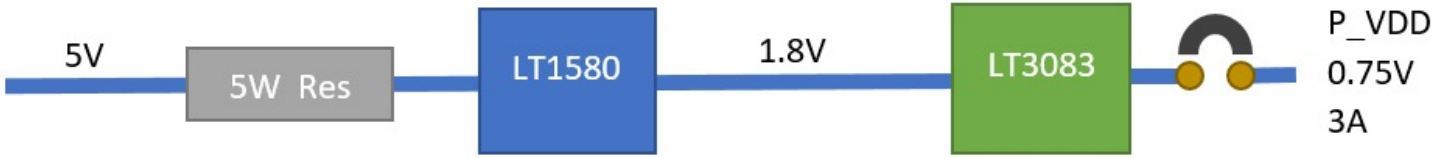


Power Delivery

- Goals:
  - Power the board from single 5V supply
  - Provide option to feed each rail from its own supply
  - Neglect impact of noise on the board PDN
  - Target impedance = 2 mOhms

Net	DC voltage [V]	Max current [A]	Max transient current [A]	Allowed deviation [mV]	Target impedance [mOhm]
P_VDD	0.75	3	1.5	3	2
PA_VDDL	0.75	2	1	2	2
PA_VDDH	1.2	2	1	2	2
P_VDDH	1.8	1	0.5	1	2

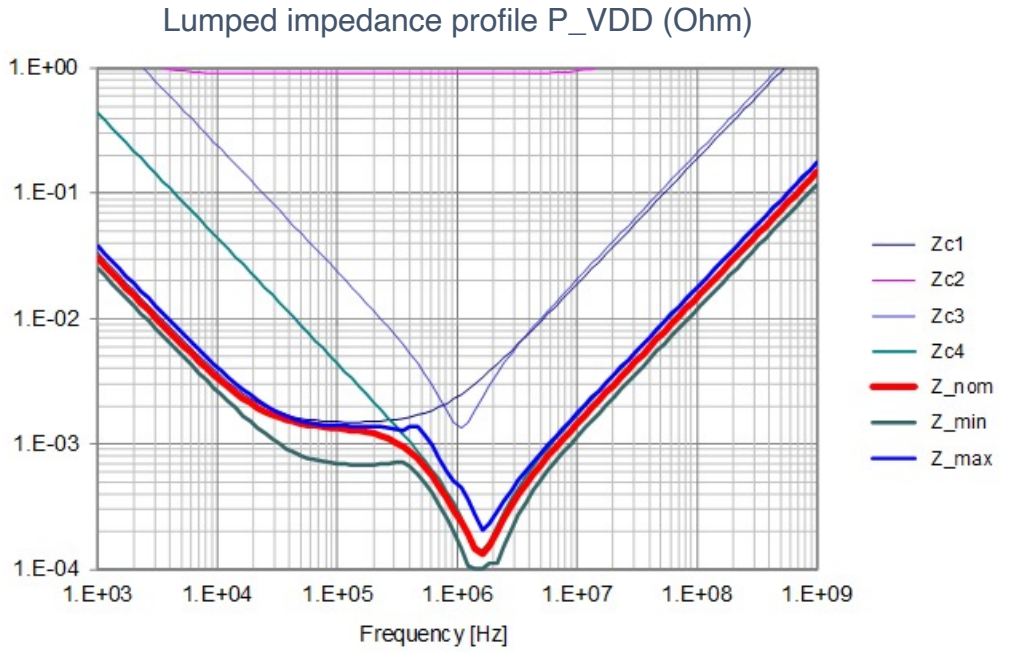
- Architecture:
  - Relatively low current = cascaded linear regulators and jumper selectable supply options.



Capacitor Selection

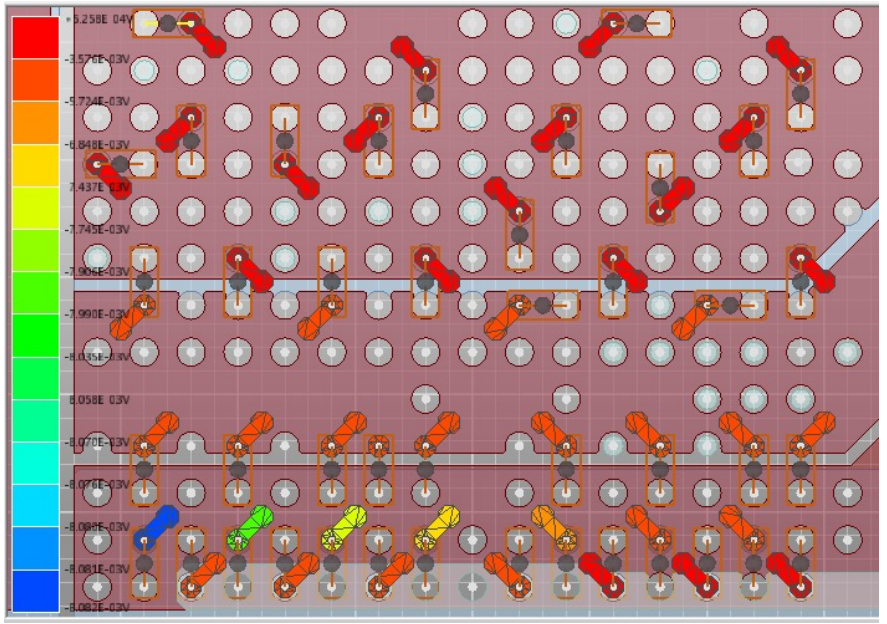
Four parallel capacitor banks	C1	tol. [%]	C2	tol. [%]	C3	tol. [%]	C4	tol. [%]	
Capacitance C [F]:	4.70E-04	20	1.00E-04	20	2.20E-05	20	1.00E-05	20	Fmin[Hz]
		-20		-20		-20		-20	1.E+03
Ser. resistance ESR [ohms]:	0.015	0	0.9	0	0.004	20	0.005	20	Fmax[Hz]
		-50		-50		-20		-20	1.E+09
Ser. inductance ESL [H]:	3.00E-09	20	5.00E-09	20	1.00E-09	20	1.00E-09	20	
		-20		-20		-20		-20	Total:
Number of parts in bank:	10		1		3		36		50

- Big-V impedance profile:
  - 10 uF 0402 ceramic opposite the BGA
    - Single value
    - Directly on Power/GND vias
  - 470 uF polymer bulk capacitors help regulator maintain low impedance
  - 22 uF ceramic at the output of the regulators for stability



Plane Optimization

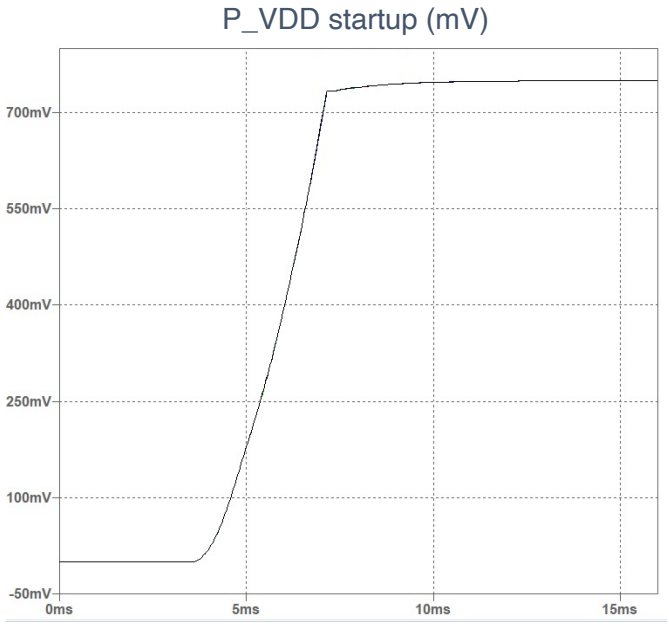
- Optimize DC-drop <1% nominal
  - 1 oz copper power layers
  - Hybrid solder iterations to optimize shape size
- Minimize rail-to-rail crosstalk
  - Avoid overlap between power planes of different nets.
    - Especially analog vs digital nets

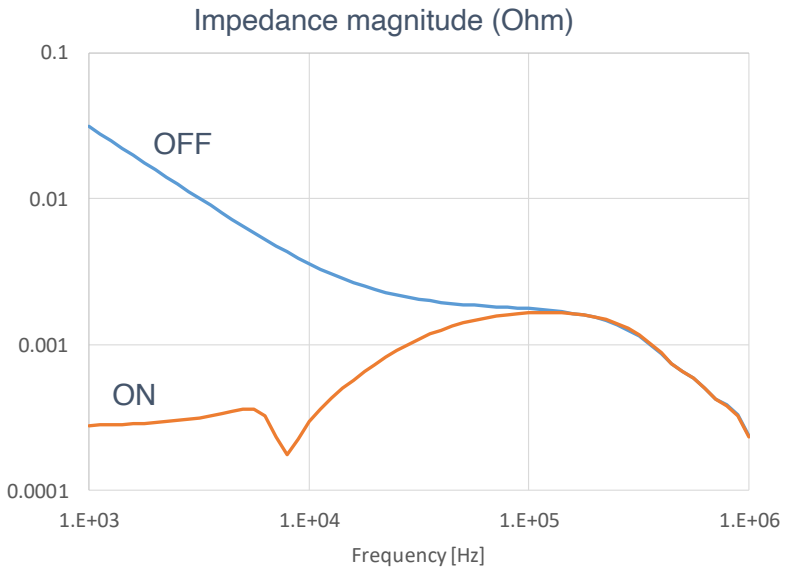


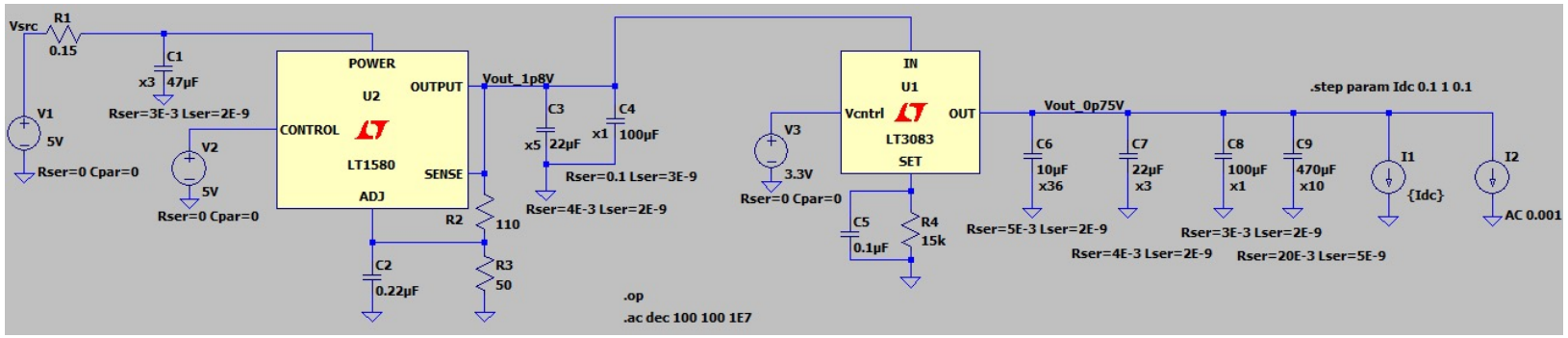
Net	DC voltage [V]	Max current [A]	Max DC drop [mV]	Max rel. DC drop [%]
P_VDD	0.75	3	5.1	0.68
PA_VDDL	0.75	2	4.3	0.57
PA_VDDH	1.2	2	8.1	0.675
P_VDDH	1.8	1	0.53	0.03

PDN Analysis

- Spice simulations
  - Vendor supplied models and simulator
  - Simulated startup behavior to ensure stability of cascaded regulators
  - Simulated output impedance with lumped external components

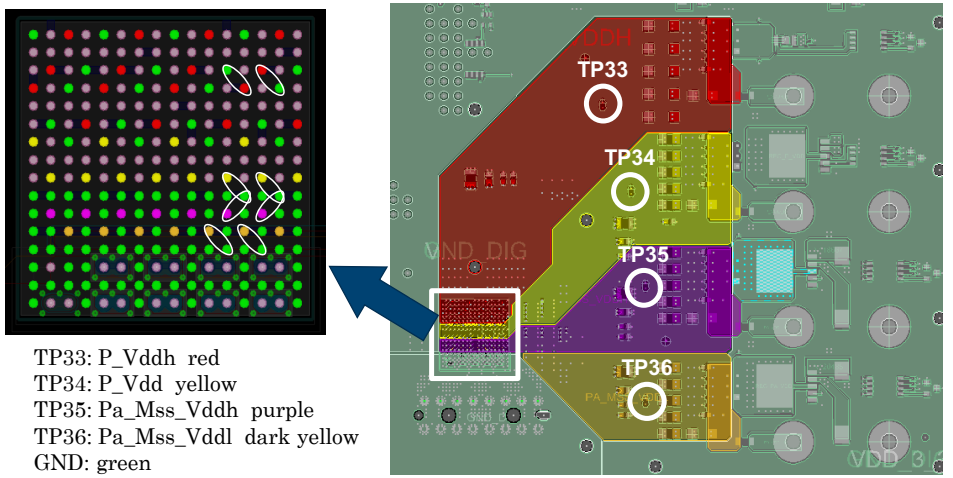




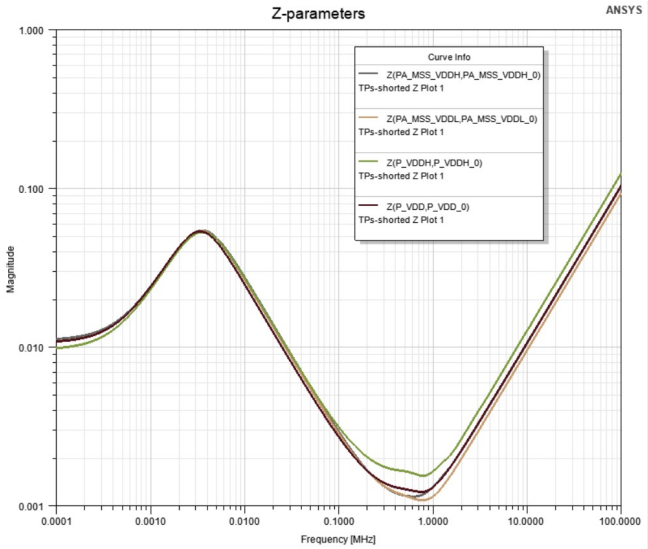


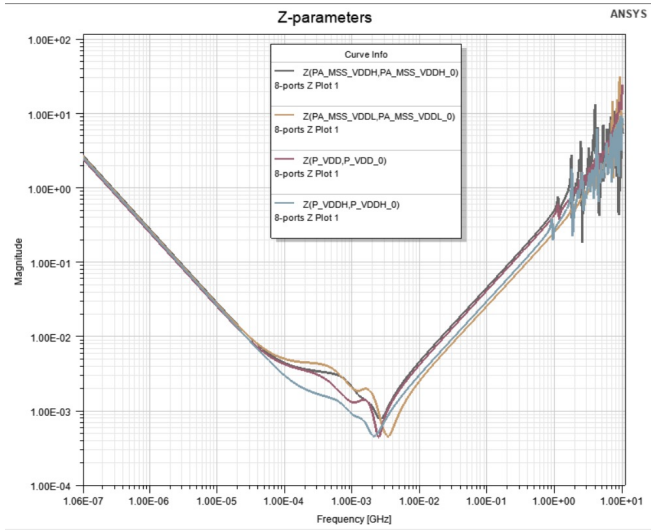
PDN Analysis

- AC impedance simulations
  - Dedicated test points and chip's pin field location
  - Mimicking two-port shunt-through measurement
- Two scenarios:
  - Voltage regulator output open (right)
  - Series R-L element mimicking regulator output impedance (left)
    - Equivalent inductance intentionally high to see bulk capacitance impedance



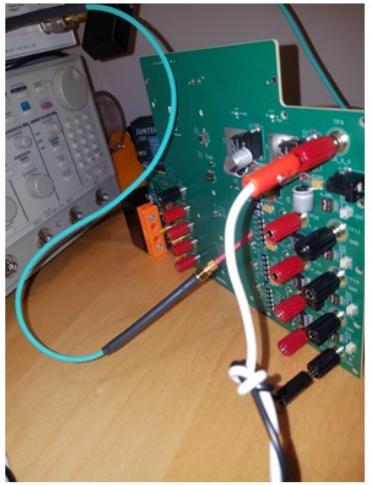
TP33: P_Vddh red
TP34: P_Vdd yellow
TP35: Pa_Mss_Vddh purple
TP36: Pa_Mss_Vddl dark yellow
GND: green



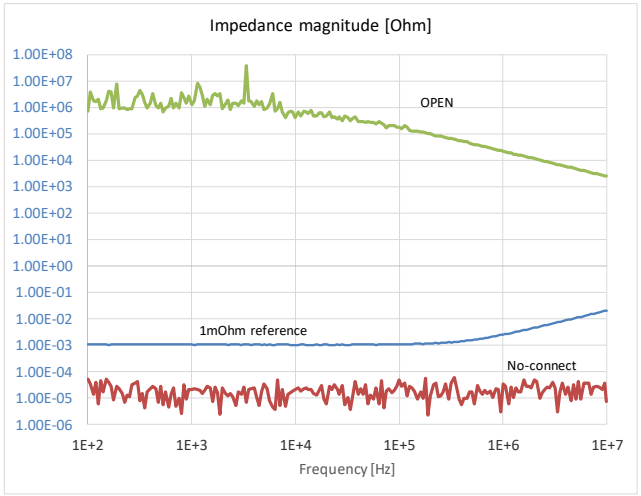


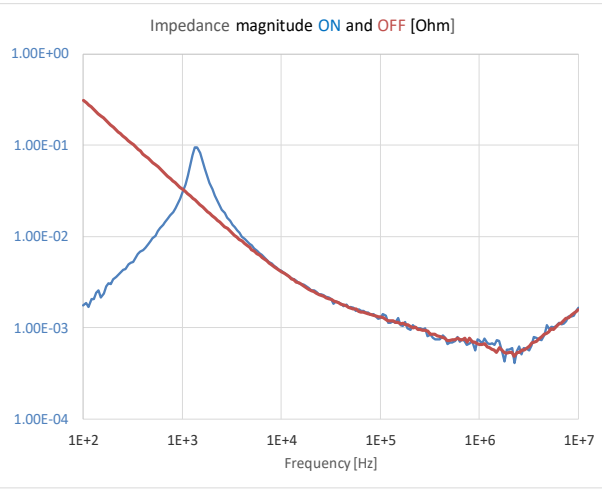
Measurements and Correlation

- Measurements:
  - VNA with common-mode toroid suppresses cable-braid ground-loop error
  - Custom made semirigid probes
  - 100 Hz – 10 MHz measurements with and without power applied



- Miscorrelation:
  - DC resistance above 10 mOhm
    - Selection jumpers simulated with zero resistance
    - Not shown – jumpers were shorted with solder
  - Impedance peak at 12 kHz around 100 mOhm with minimum load current

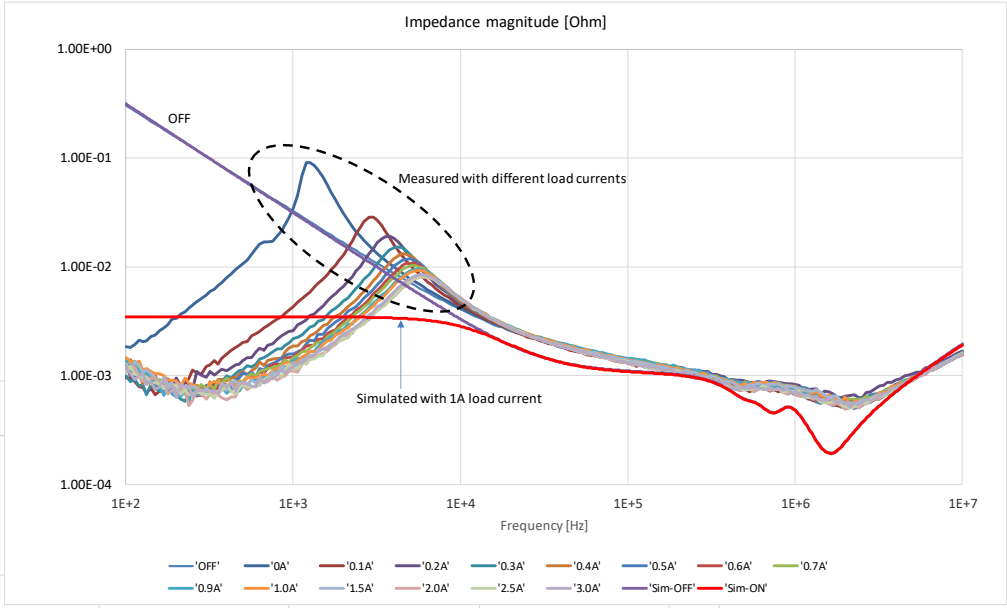


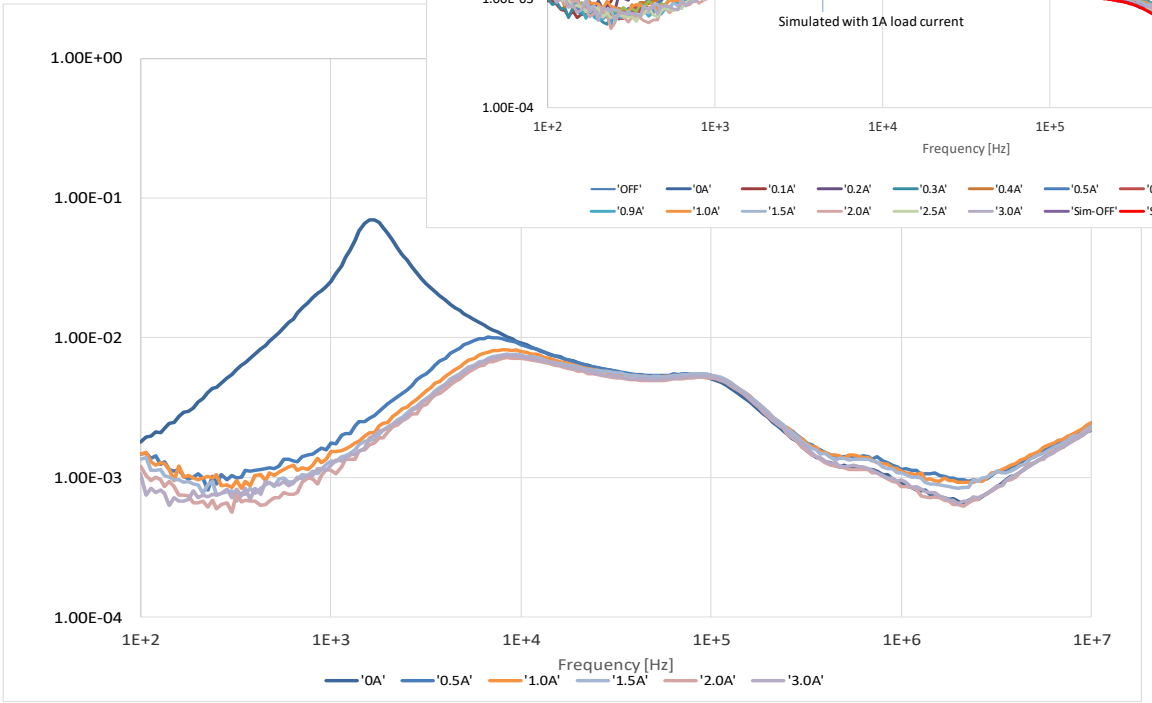


Root Cause Analysis

- Investigation:
  - Disabled upstream regulator
  - Added lossy bulk capacitors
  - Altered the regulator's feedback circuit
  - Measured evaluation board of regulator

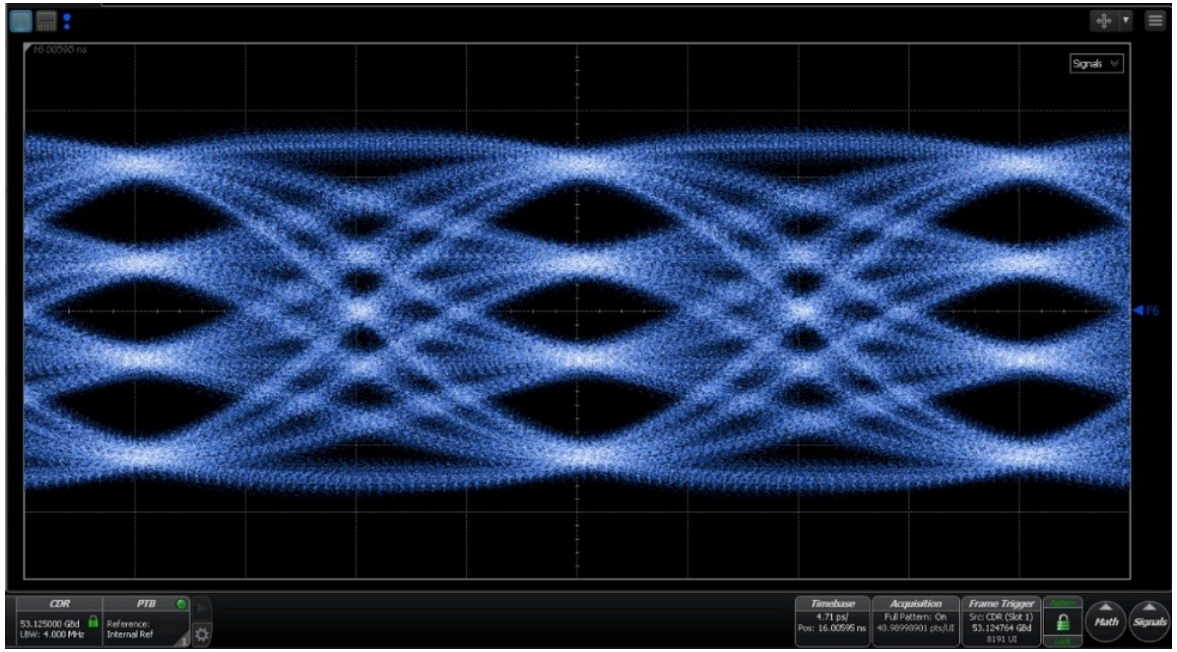
- Improvements:
  - Updated model's closed loop bandwidth
  - BOM change, higher ESR bulk capacitor





Channel Performance

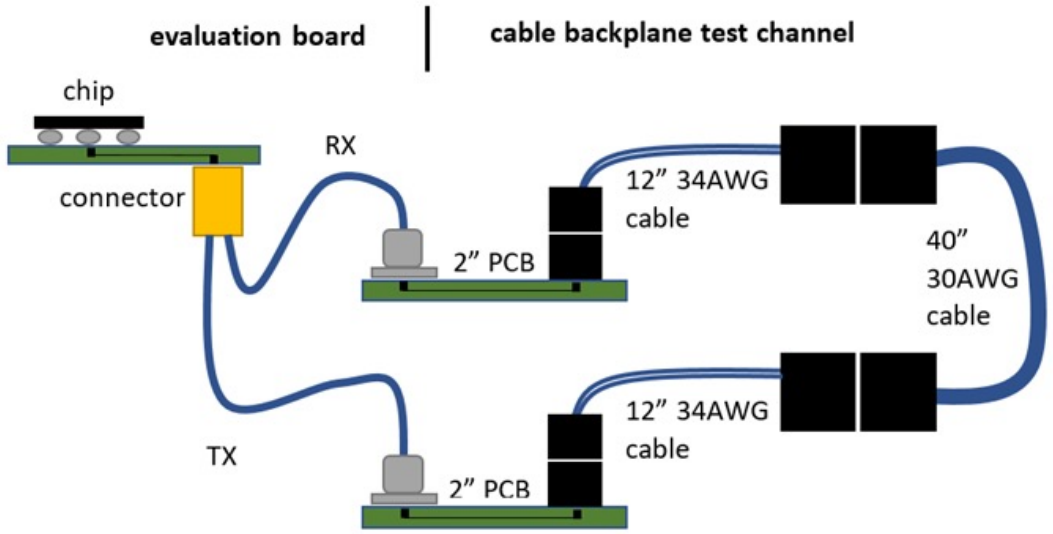
- Powered with onboard regulators
- PRBS31 test signals
- Sampling scope with de-embedding tool
- Clean transmitter PAM4 eye diagram at 106.25Gbps

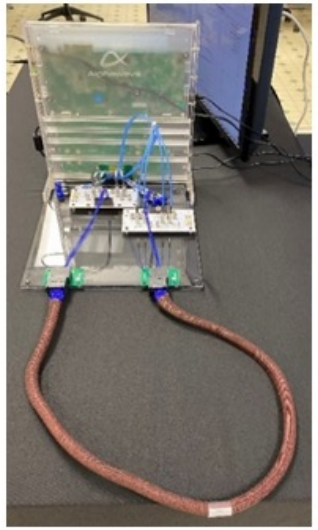


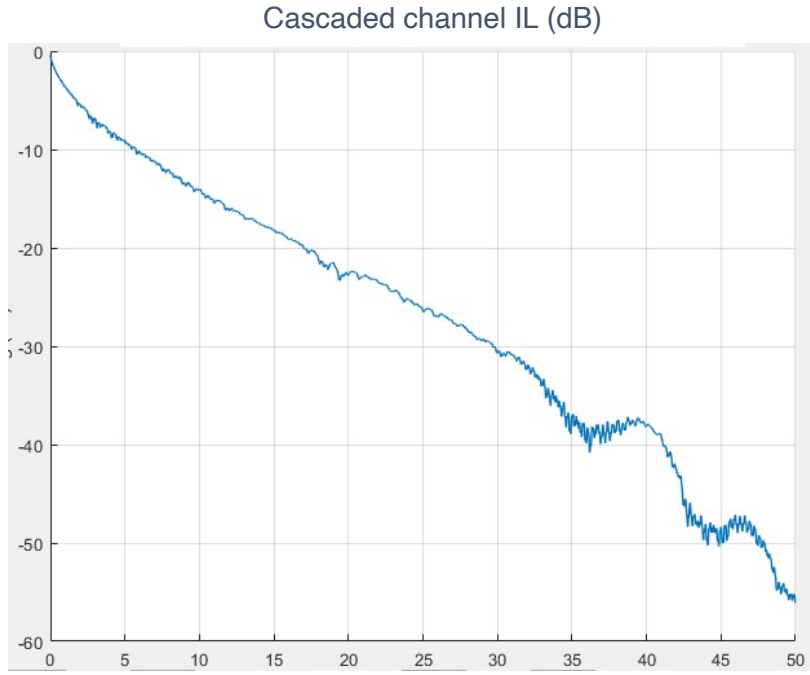
TX Eye Diagram measured with N1060A Precision Waveform Analyzer module

Real Life Channel

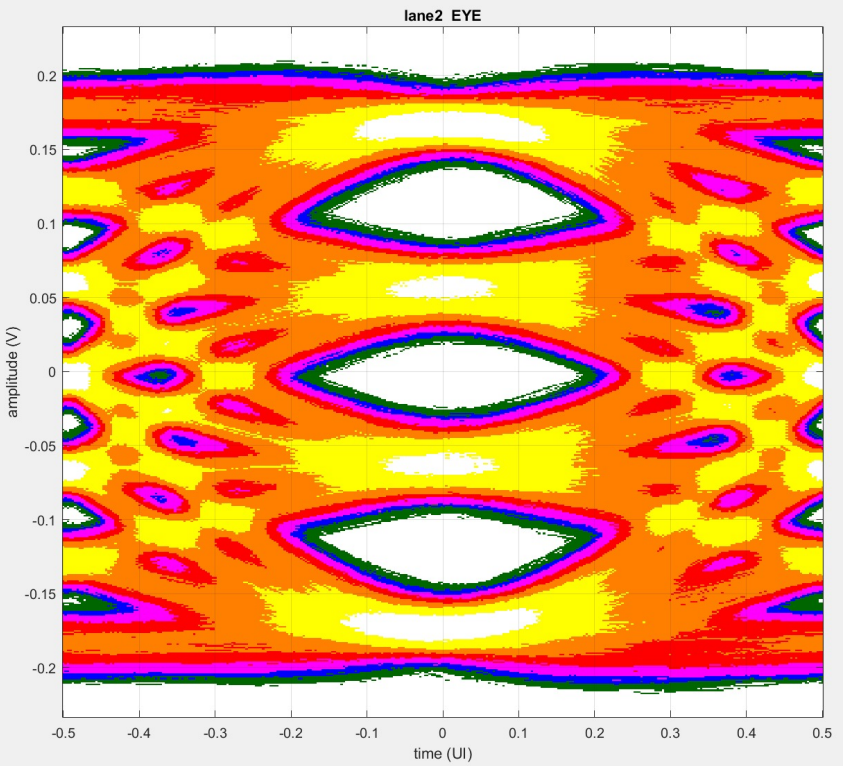
- Cable backplane test channel



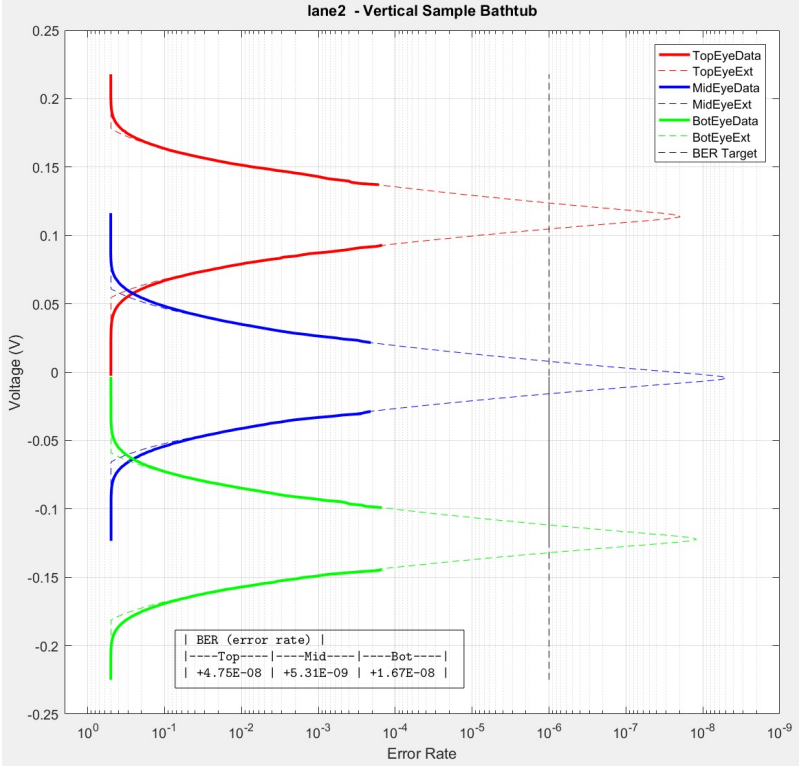




BER Results



Receiver eye diagram

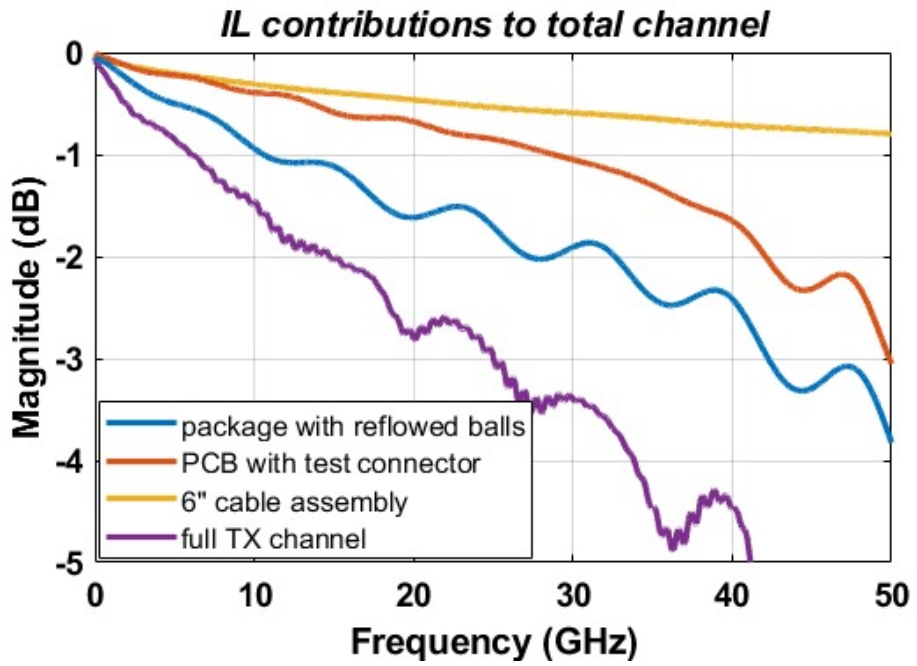


BER curve

- Good margins at the receiver
- BER ~1e-8 pre-FEC

Summary

- Successful design enabling 112G-PAM4 silicon evaluation
  - Low insertion loss TX and RX design
  - Clean power distribution
  - Good channel performance
- Important learnings
  - Under-modeled loss contribution of the package
  - BGA package attach cannot be neglected for high data rates
  - Testing power converters prior to design



gEEk® spEEk


samtec.com/geekspeek


geekspeek@samtec.com


SIG@samtec.com