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How to Read the ESR Curve of Capacitors

Istvan Novak

Outline

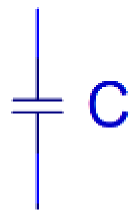
- What is ESR, why should we care
- The impedance of capacitors
- Frequency dependency of ESR
- Sources of ESR
- Getting the series equivalent circuit
- Measured examples
- ESR: what is guaranteed by spec
- How much ESR varies
- Consequences of ESR variations
- Secondary effects
- Summary

Effective Series Resistance (ESR)

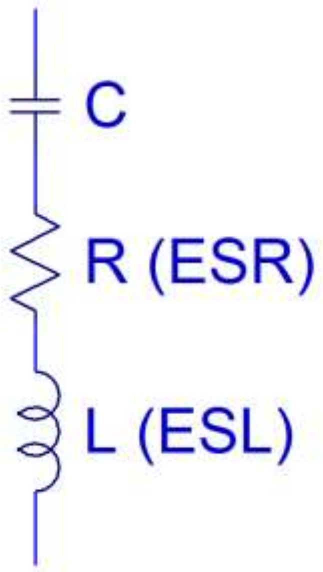
Why should we care for ESR?

- RF/MW: dissipative losses, unloaded Q of circuit
- PI: PDN impedance, ripple dissipation
- SI: loss in DC blocking applications

Ideal capacitor
No parasitics

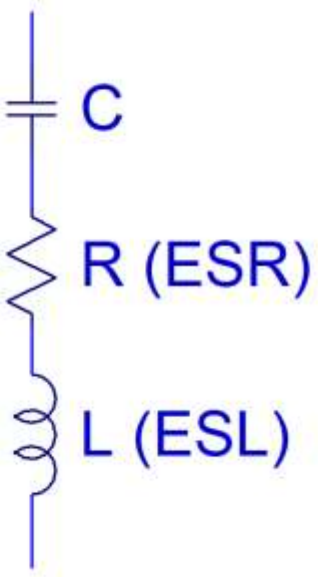


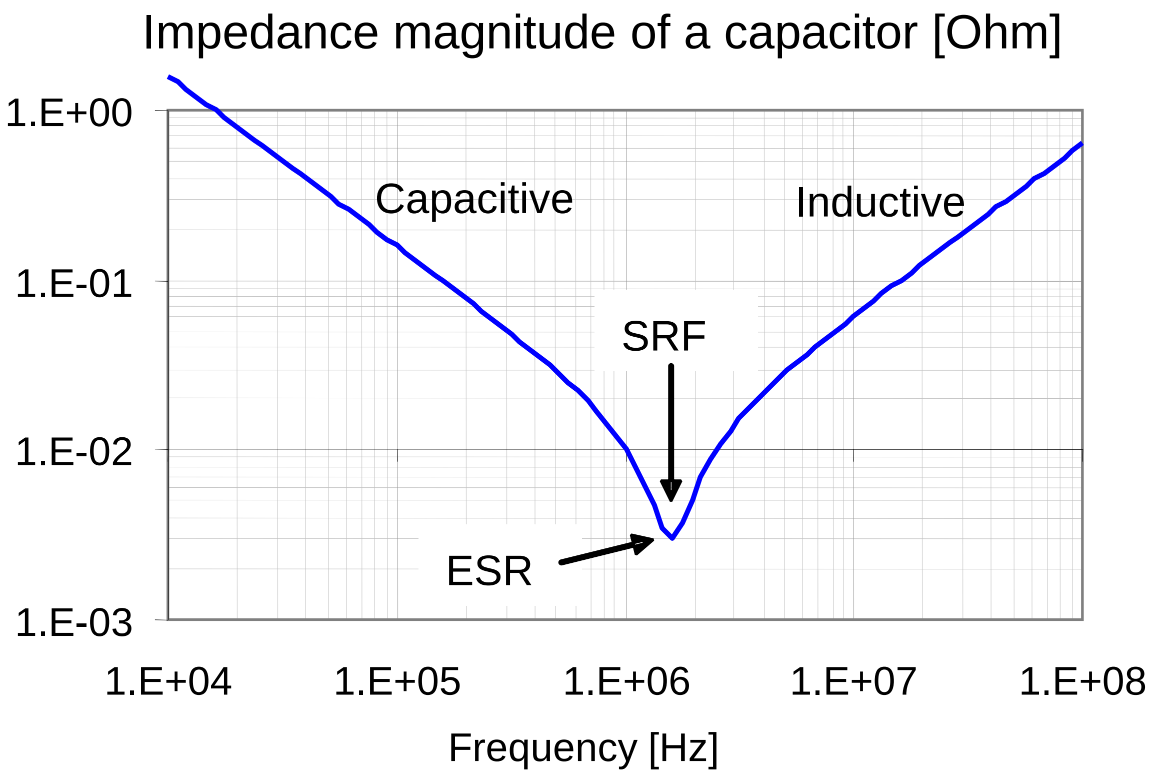
Real capacitor
ESR and ESL parasitics



The Impedance of Capacitors

A simple equivalent circuit of a capacitor including its resistance and inductance



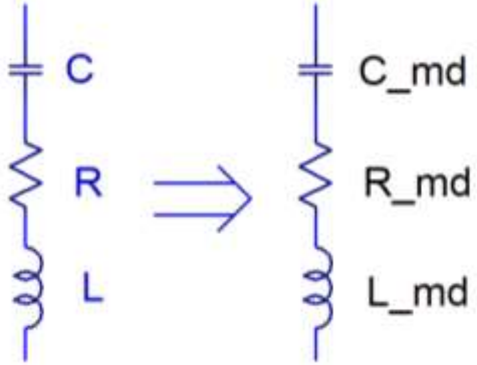


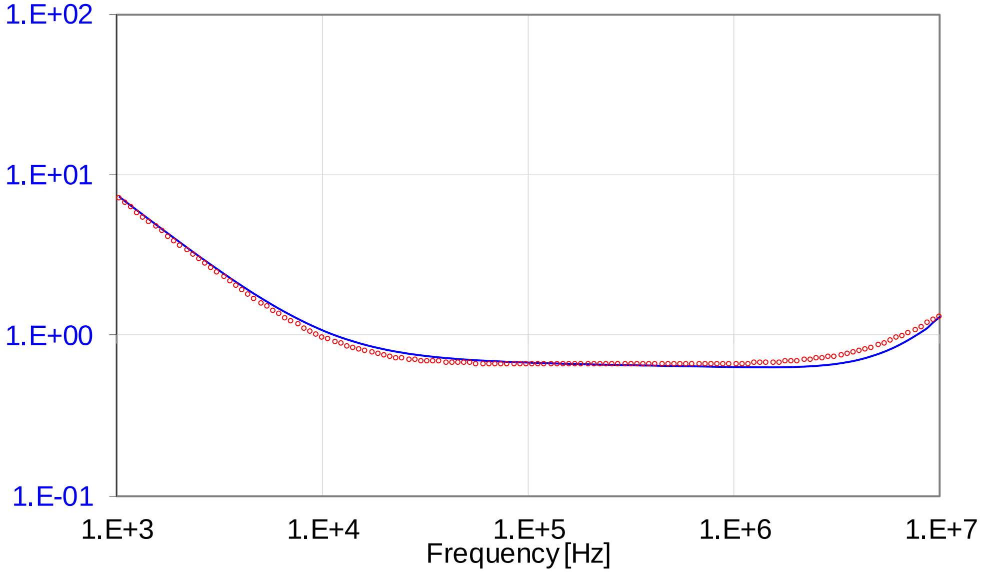
How Accurate Is the C-R-L Model?

A simple equivalent circuit of a 22uF electrolytic capacitor with frequency-independent resistance and inductance

MODEL PARAMETERS:

C_md	R_md	L_md
2.20E-05	6.50E-01	1.80E-08





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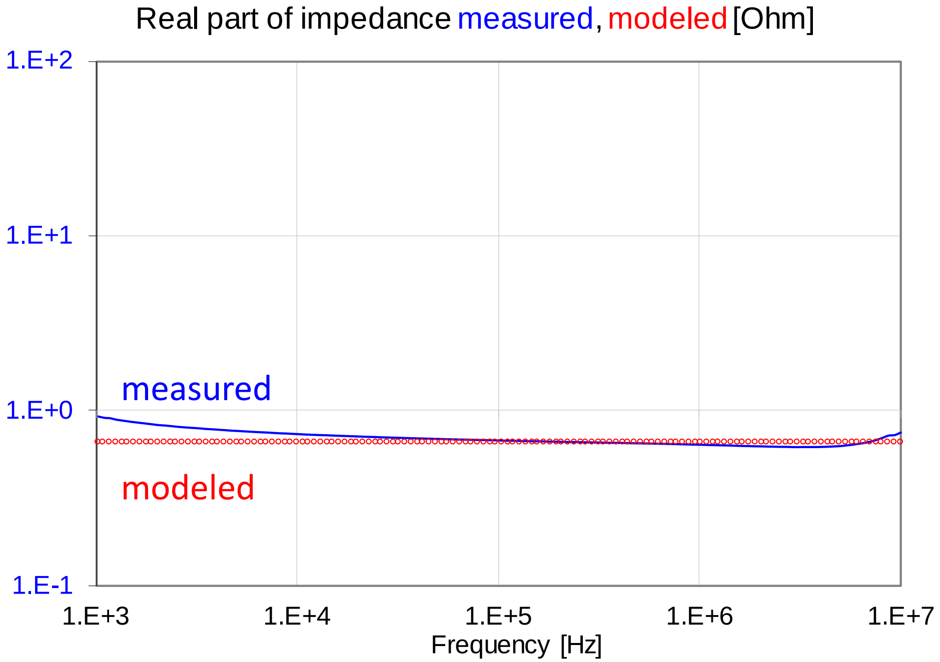
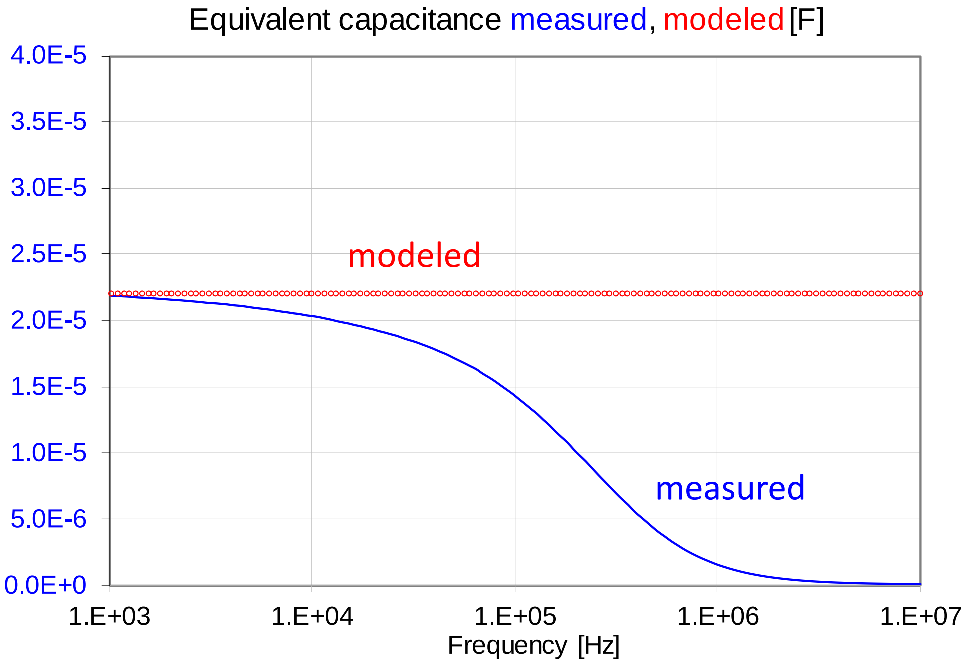
How Accurate Is the C-R-L Model?

The frequency-independent ESR is fairly accurate (for this part, in this frequency range)

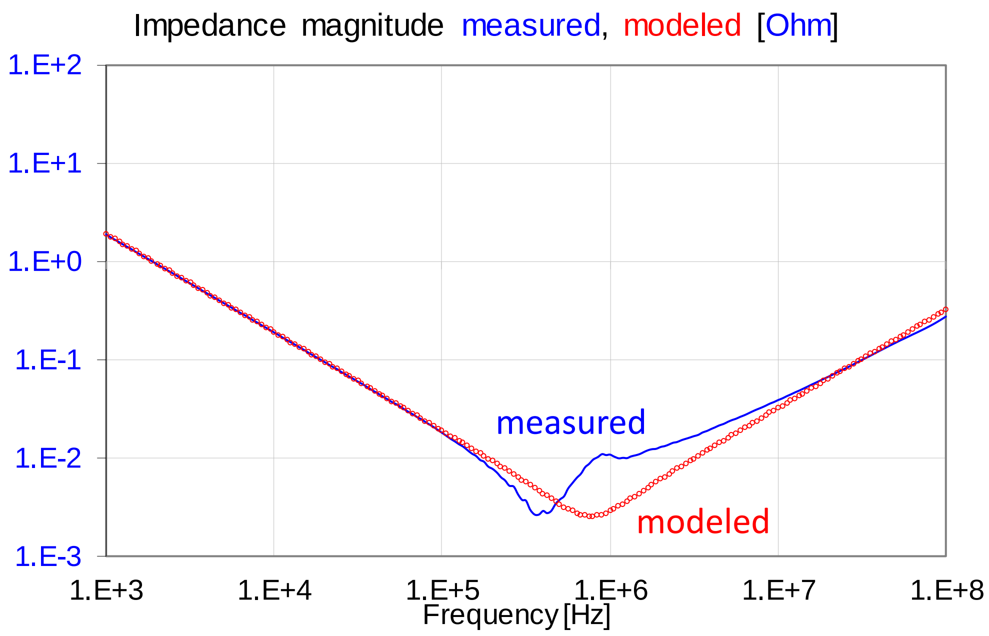


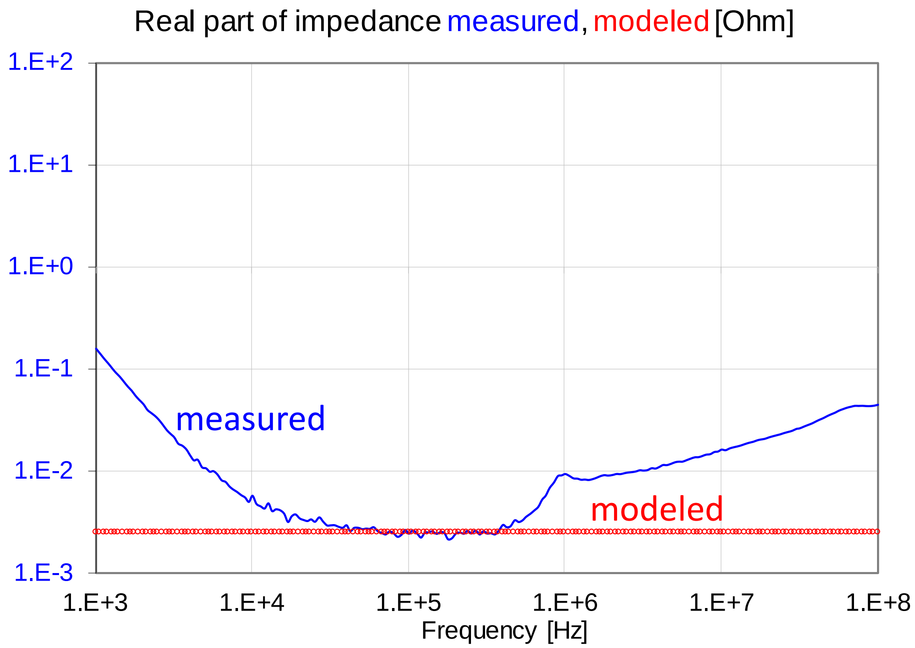


How Accurate Is the C-R-L Model?

The frequency-independent ESR is a fairly bad fit for a 100uF MLCC part

MODEL PARAMETERS:		
C_md	R_md	L_md
8.50E-05	2.50E-03	5.00E-10

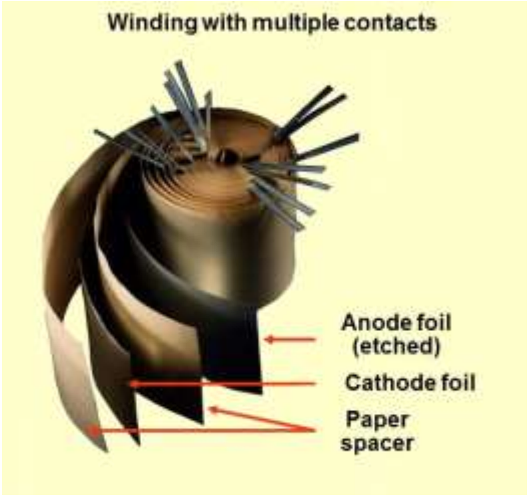




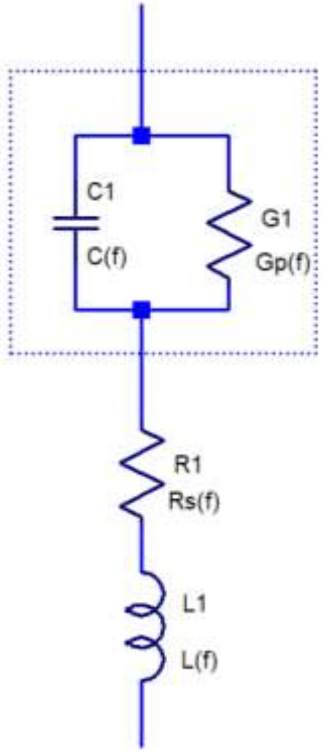
Effective Series Resistance: Its Sources

- Conductor loss (R1): terminals, capacitor plates
- Dielectric loss (G1): dielectric loss tangent of insulating material, surface leakage

Source https://go.kemet.com/en-us/en-us/06-2020-webinar-mlcc-and-film-construction-characteristics



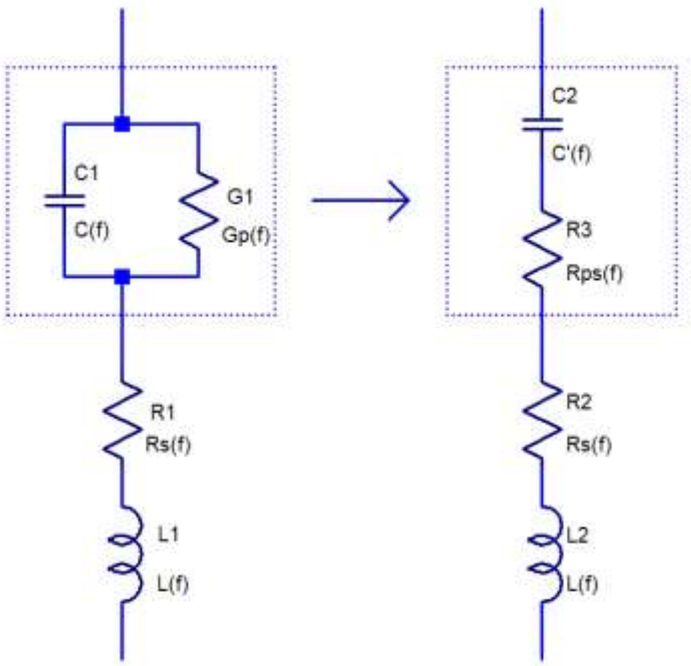
Source https://en.wikipedia.org/wiki/Aluminum_electrolytic_capacitor#/media/File:Al-e-cap-winding-multi-tabs.jpg



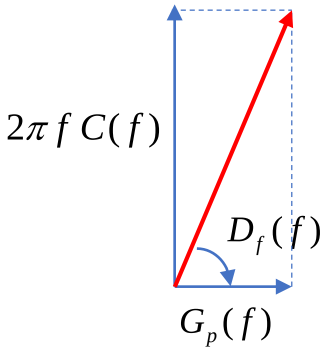
What Makes ESR Frequency Dependent?

Multiple reasons:

- G1 is frequency dependent
  - For a given Df(f) dielectric loss tangent G1 is
- R1 is frequency dependent due to current redistribution
- G1 and R1 are mixed through opposite-sign reactance



Admittance of capacitors



Frequency dependence of capacitance and dielectric loss

$$C(f) = C(f_0)\left(1 - Df(f_0) Ln(\frac{f}{f_0}) \frac{1}{\pi/2}\right)$$

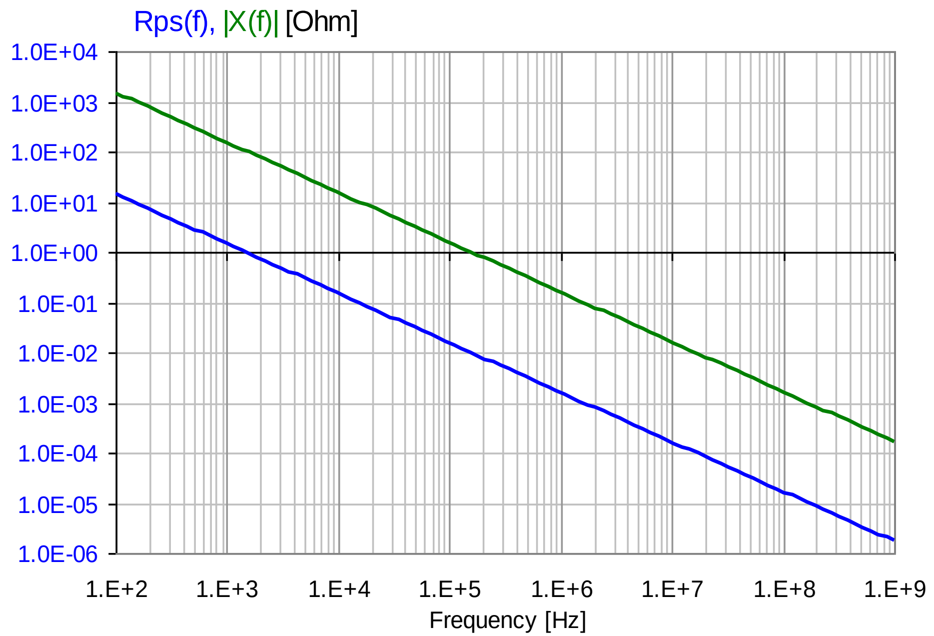
$$Df(f) = Df(f_0)\frac{C(f_0)}{C(f)}$$

Frequency dependence of conductive loss due to skin effect

The Combination of Series and Parallel Losses

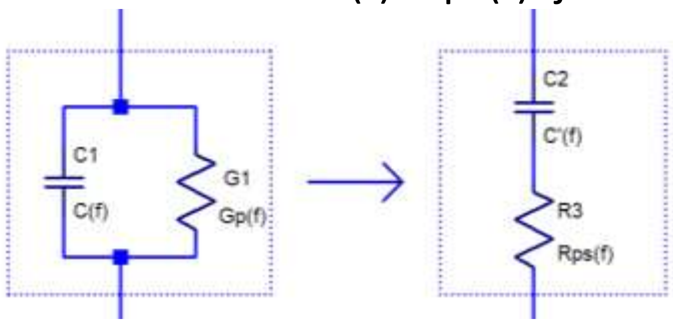
The conversion:

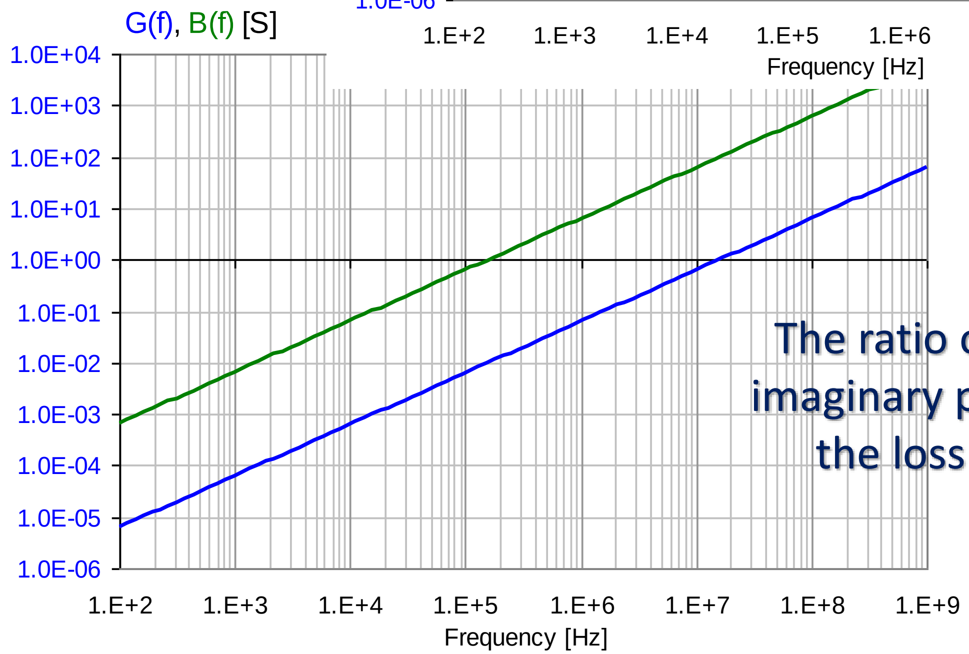
- Step 1: Convert the parallel R-C to a series R-C network
- Step 2: Add the series R-L network related to conductive losses
- Converting parallel to serial circuit mixes the real and imaginary parts



$Yp(f)=Gp(f)+j2\pi f\ C(f)$

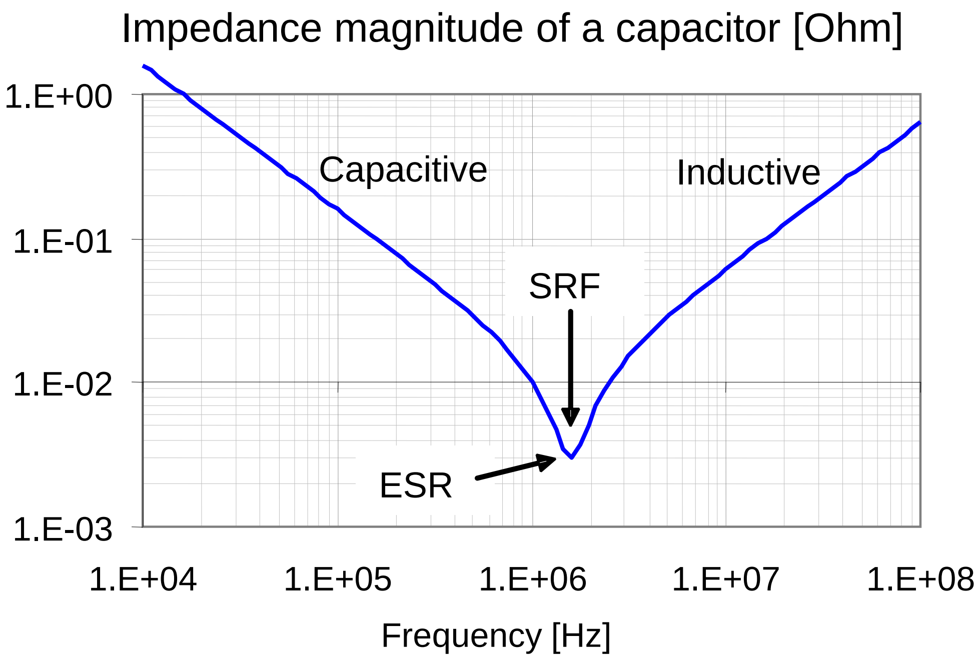
$Zs(f)=Rps(f)+j2\pi f\ C(f)$

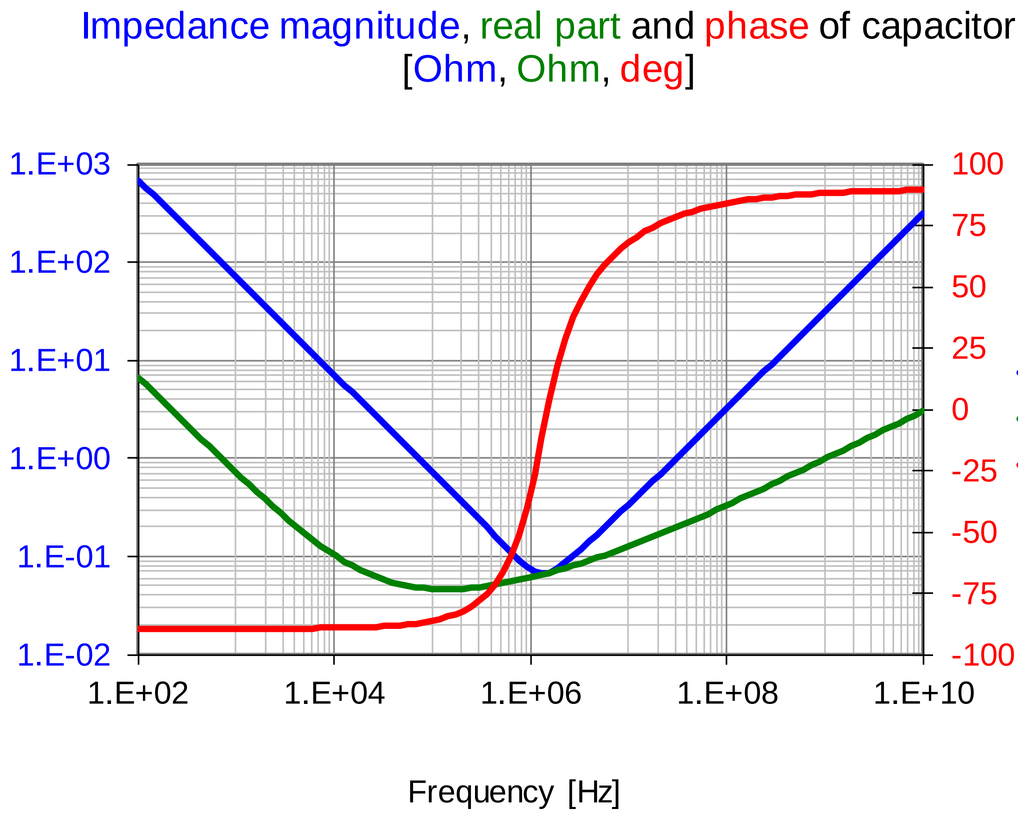




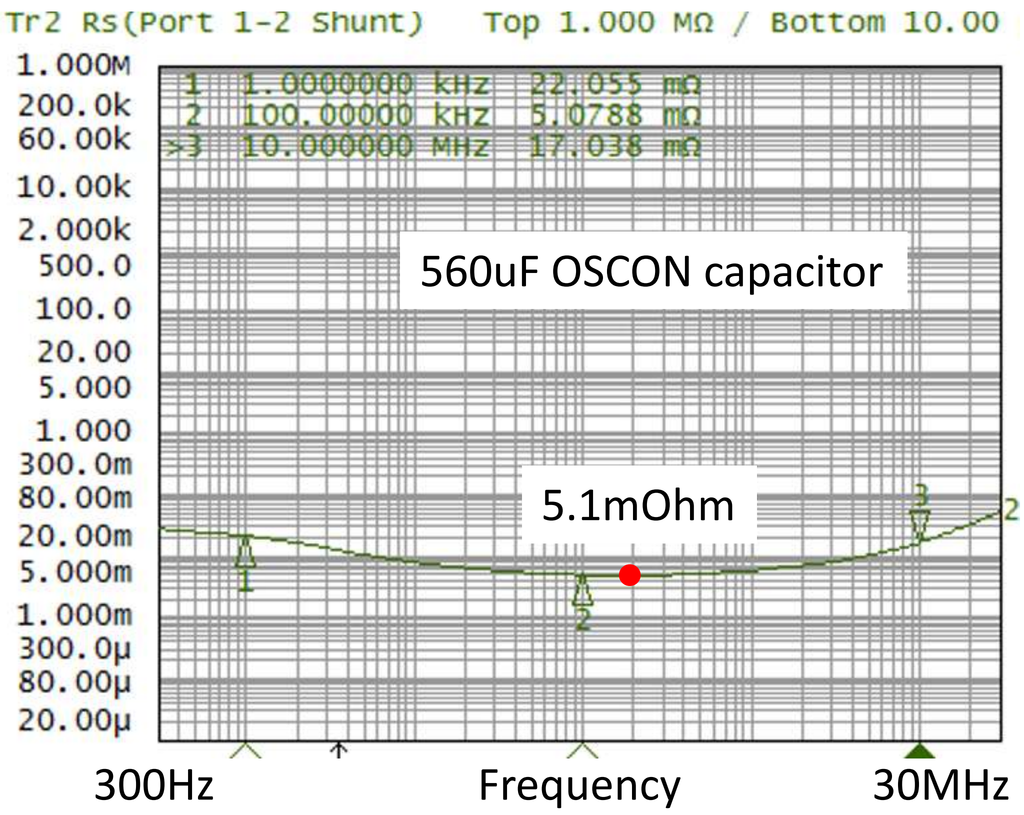
The ratio of real and imaginary parts equals the loss tangent

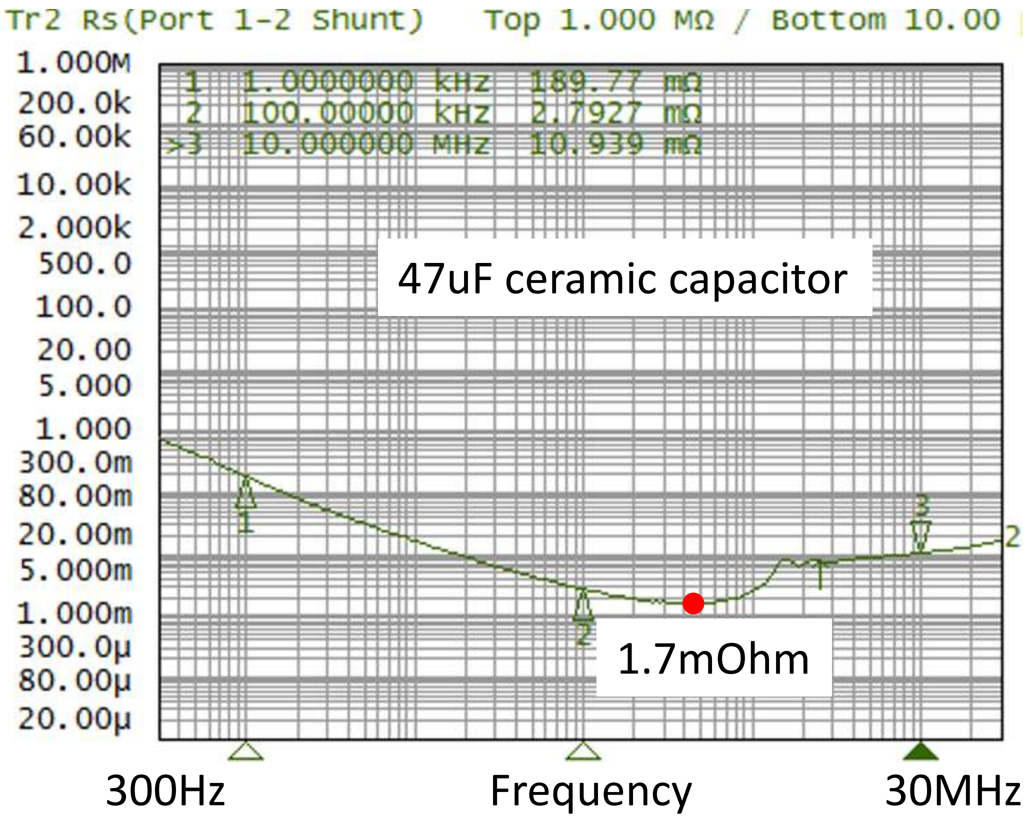
The Combined Series and Parallel Losses





Some Measured ESR Examples





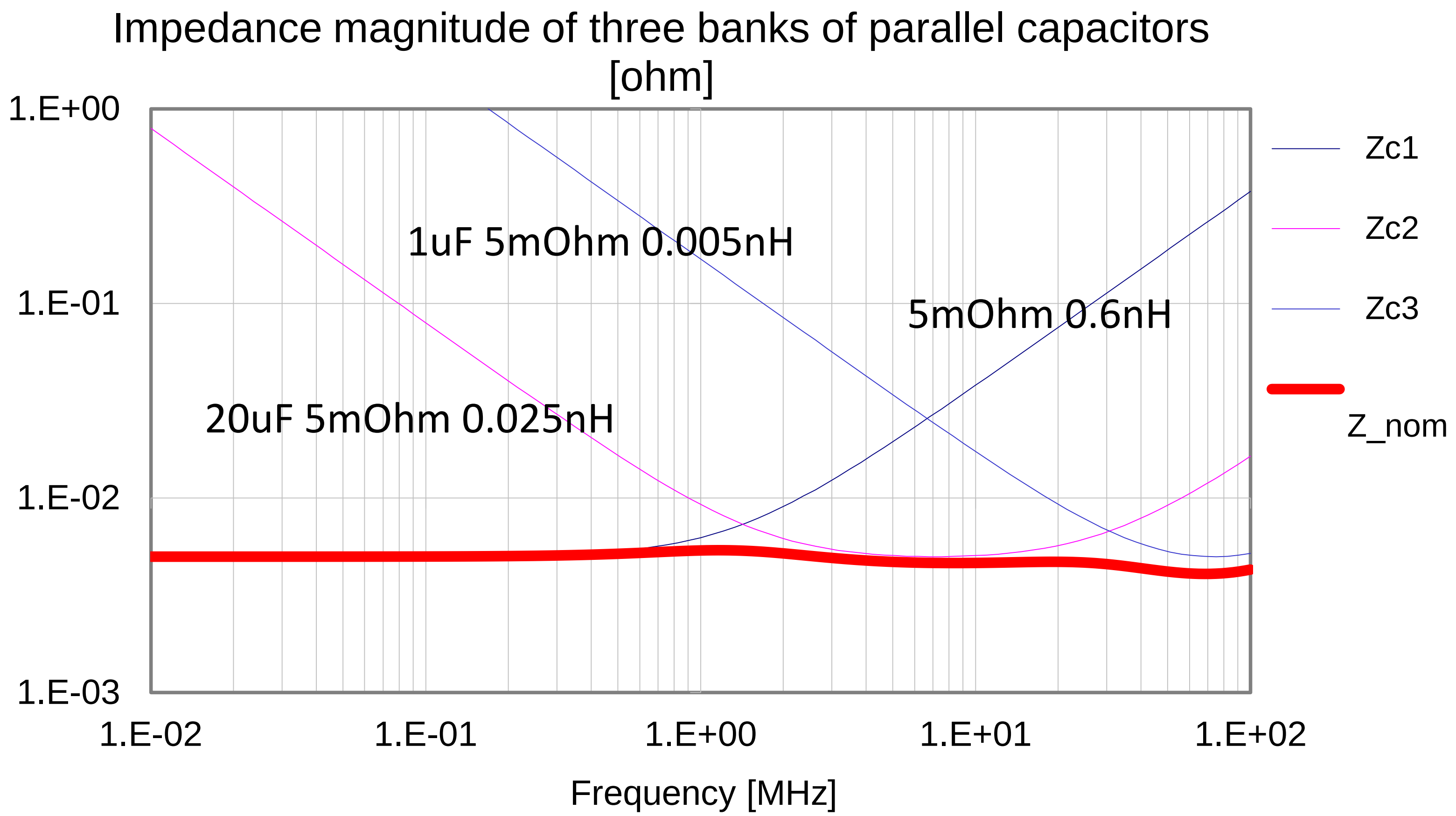
ESR: What is Guaranteed by Spec?

- MLCC: we get typical ESR values at best
- Tantalum, electrolytic capacitors: at best we get the maximum ESR values
- Exception: controlled-ESR capacitors
- Don’t forget some additional conditions: aging, thermal shock, etc

See more in: “History of Controlled-ESR Capacitors at SUN,” DesignCon 2007

ESR Uncertainty: Why Should We Care?

An example with three banks of PDN parts, nominally producing flat 5mOhm lumped impedance

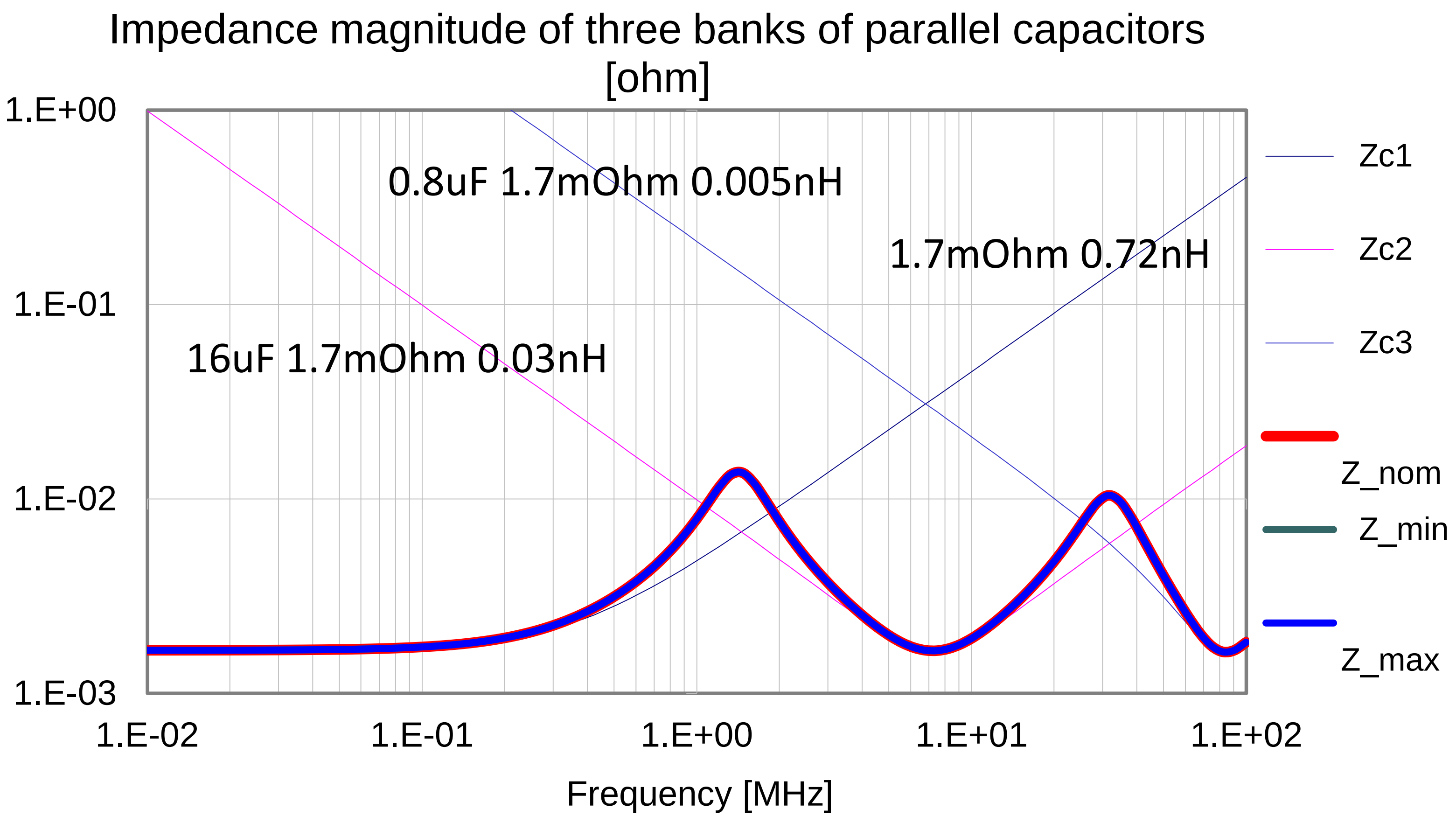


WC transient noise: 5 mVpp/A

See examples in: "Electrical and Thermal Consequences of Non-flat Impedance Profiles," DesignCon 2016

ESR Uncertainty: Worst Case

Assume 1/3x…3x ESR variation and +-20% C and L variations



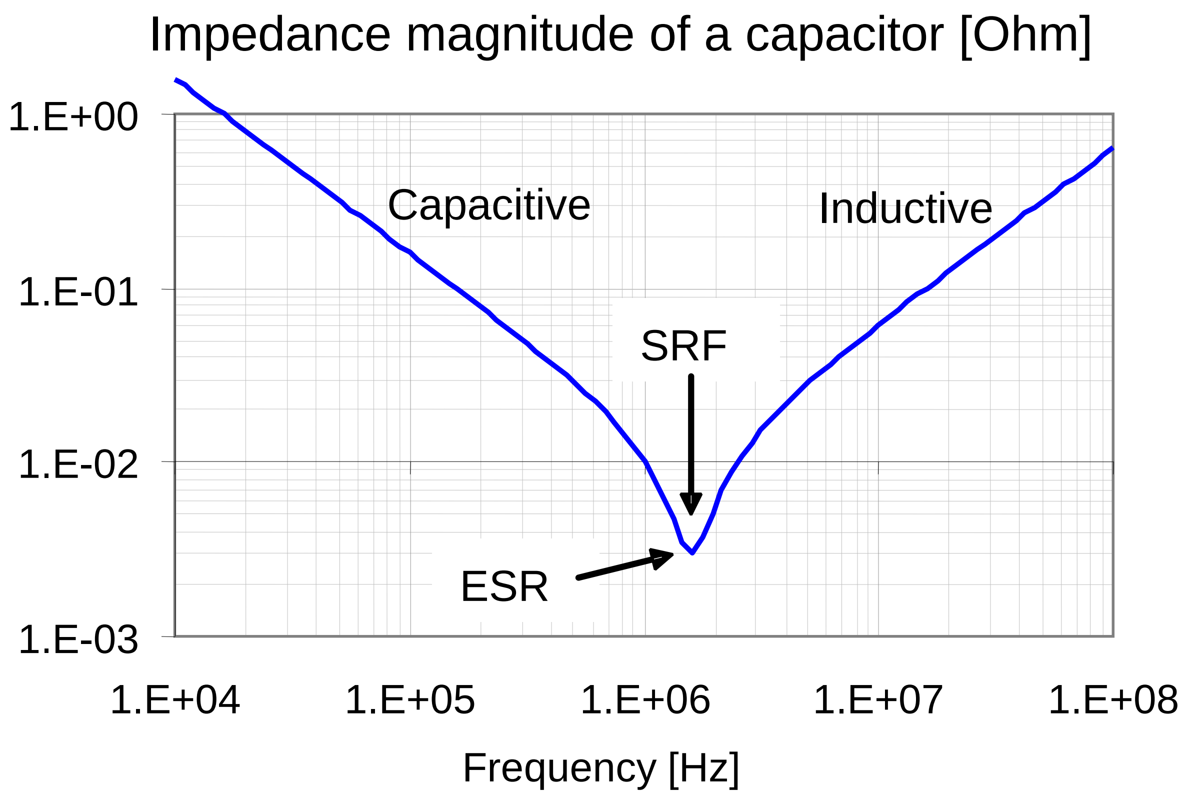
WC transient noise: 19 mVpp/A

What Frequency Range Should We Care?

Usually, the vicinity of SRF matters

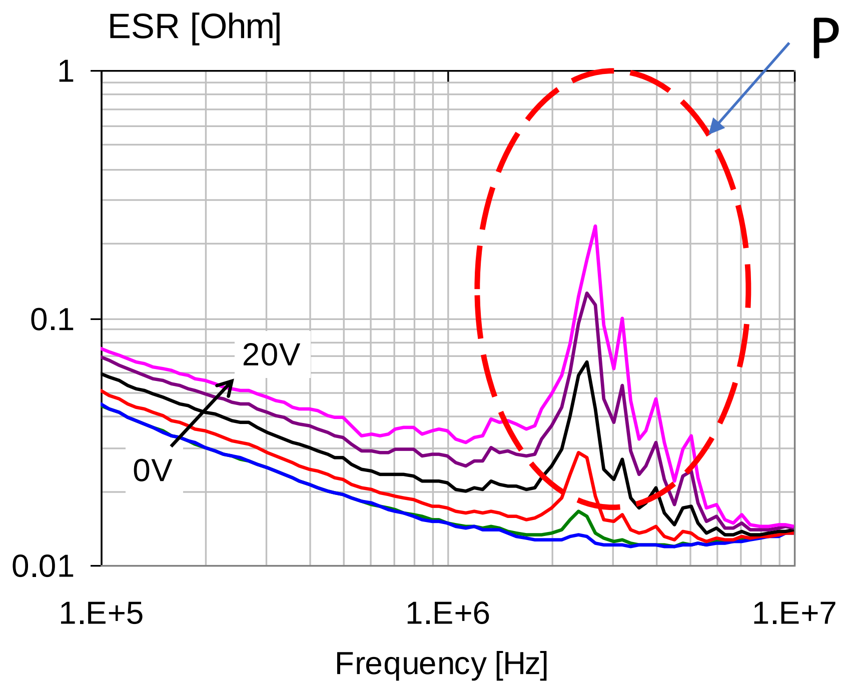
At much lower and higher frequencies other PDN components will dominate

Note: some simulators may use truncated values

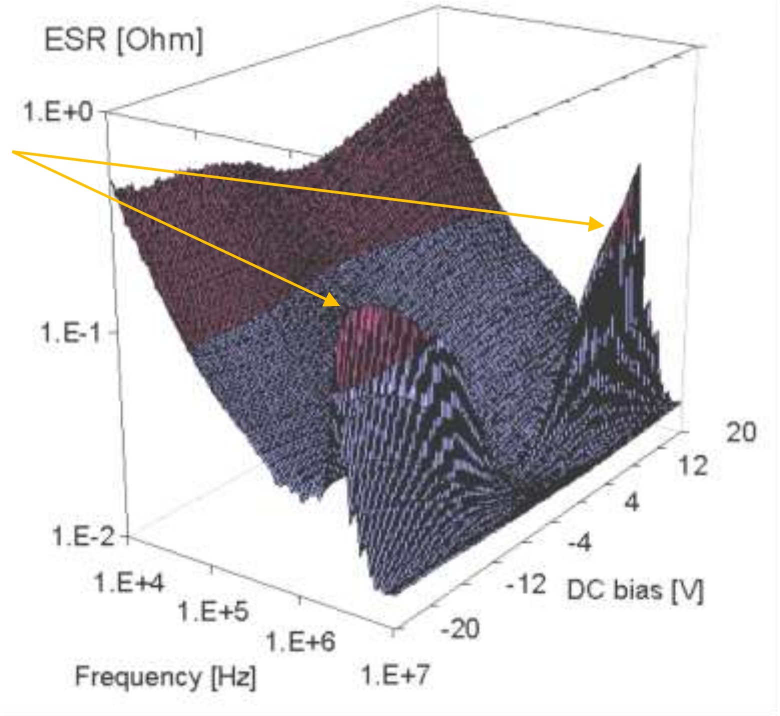


ESR and DC Bias in Class II MLCC

- ESR does not change above SRF
- ESR increases below SRF as C drops
- Piezo effect shows up with increasing bias

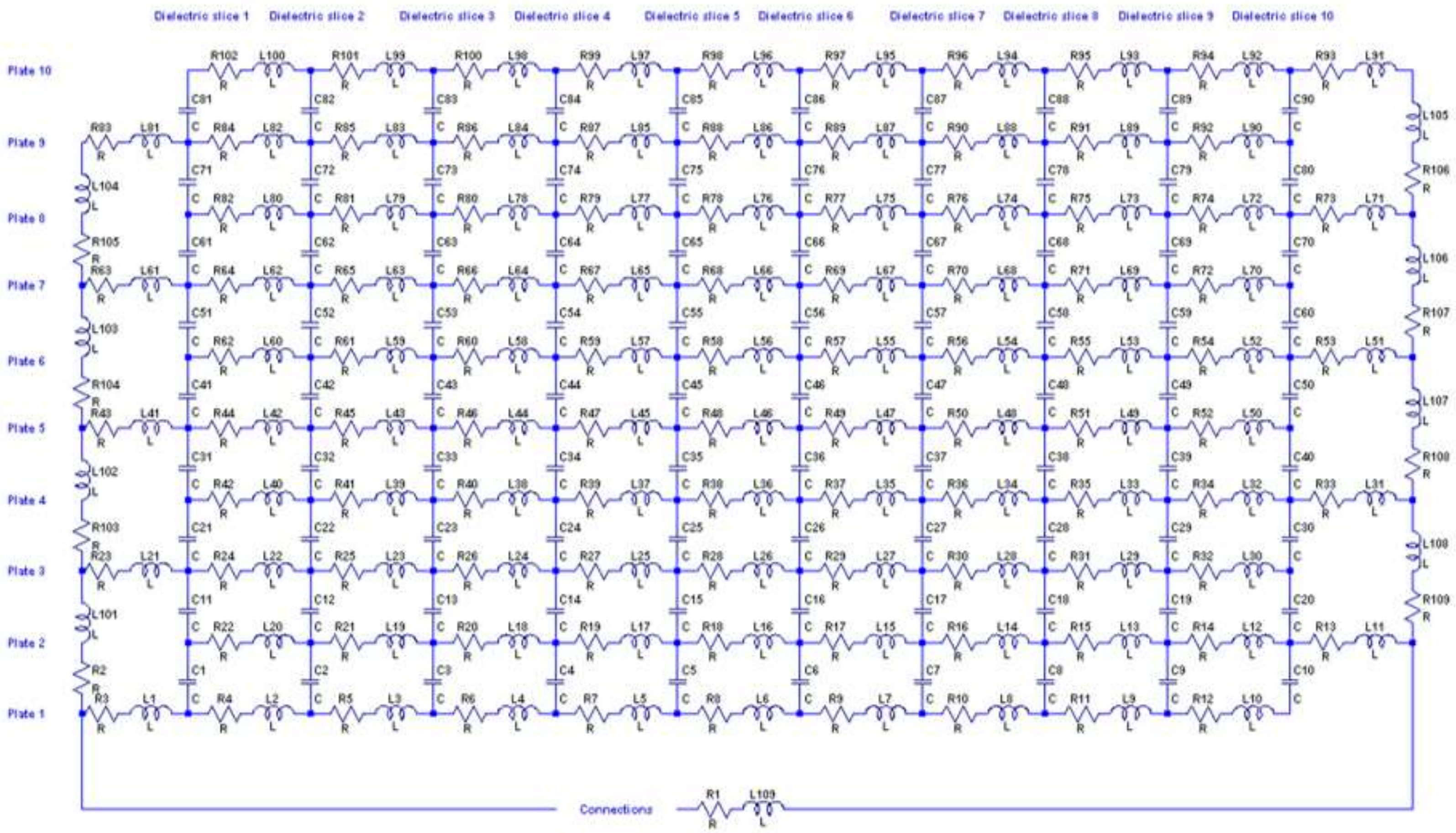


Piezo effect



Secondary Effects: 2D Models

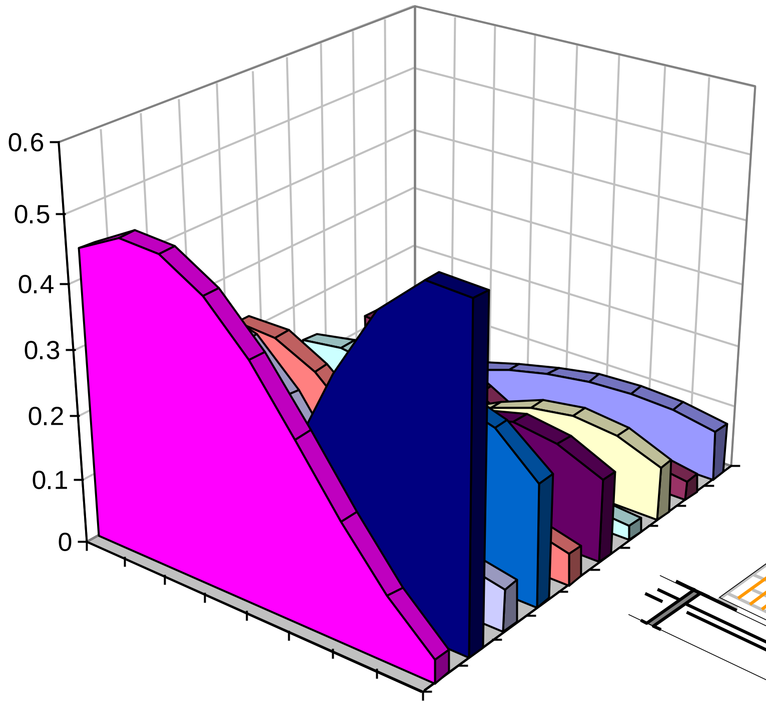
Two-dimensional bedspring model

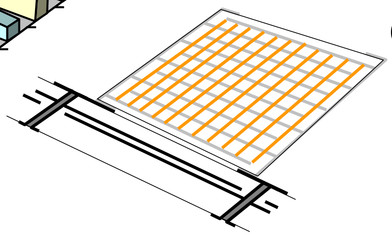


Secondary Effects: 2D Models

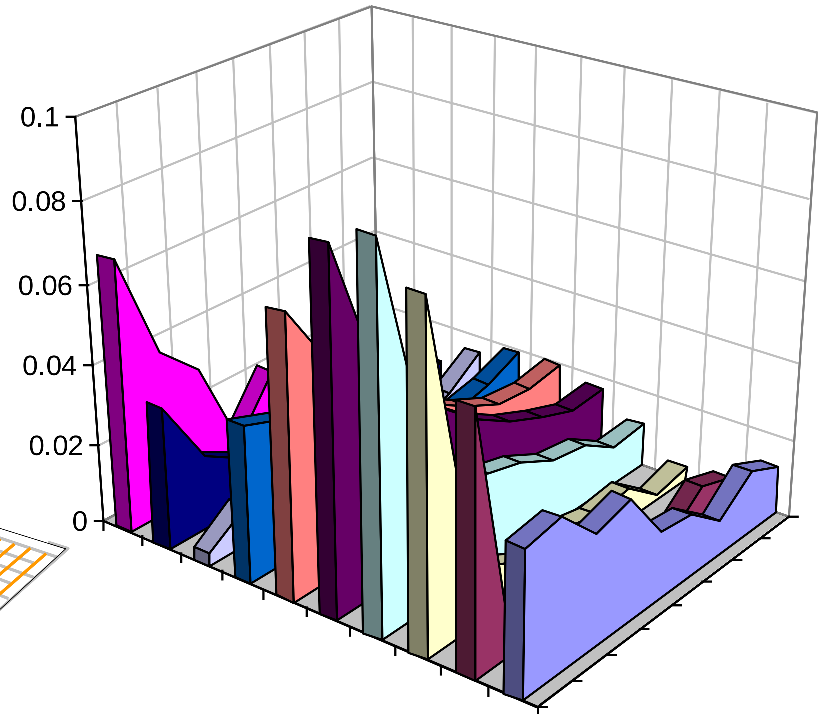
Internal current flow of MLCC at high frequencies captured with the 2D bedspring model.
Note: the horizontal and vertical resonances

Plate current at high frequency [A]



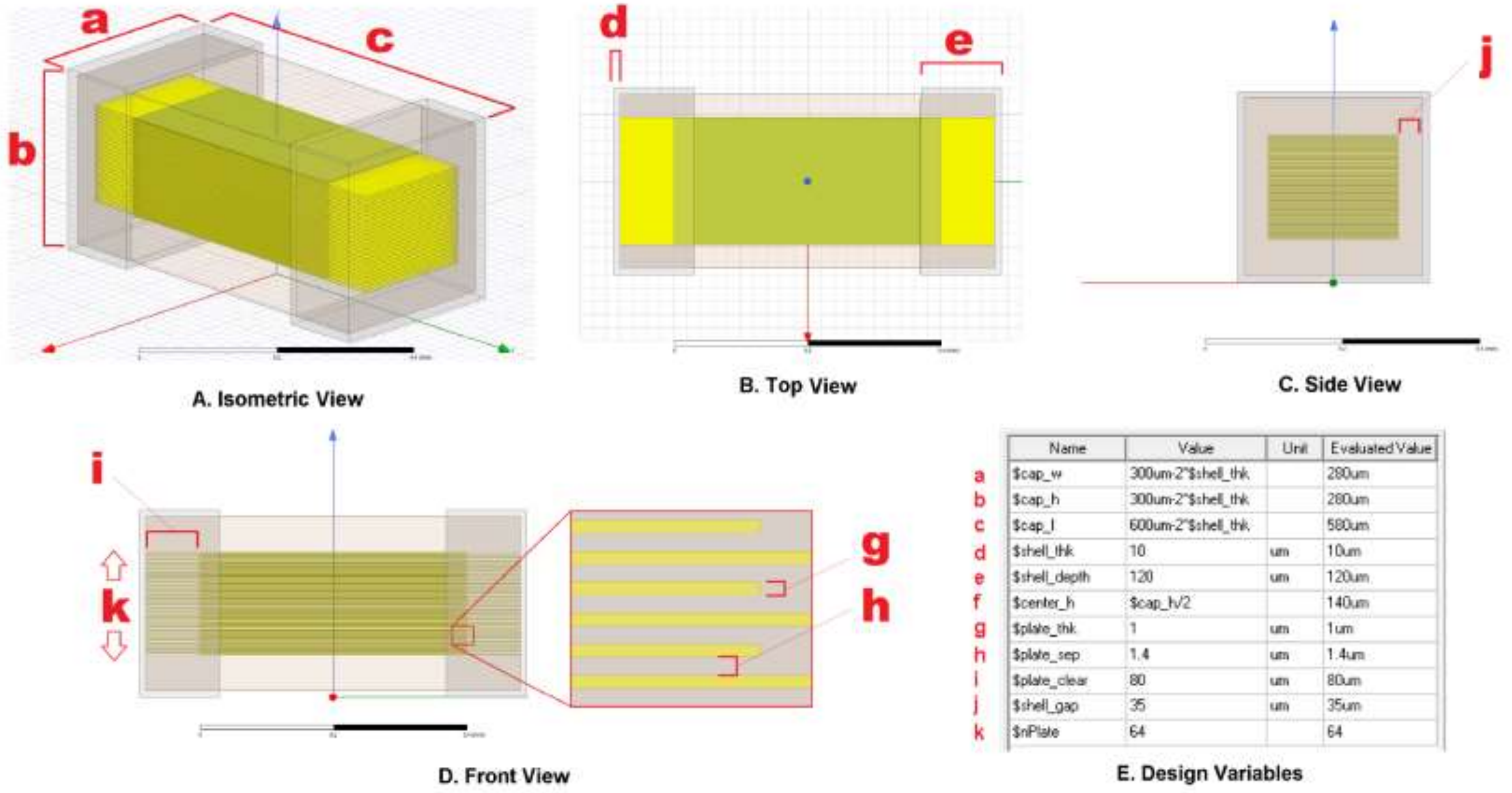


Dielectric current at high frequency [A]



Secondary Effects: 3D Models

Simulates the internal geometry of the capacitor together with its immediate vicinity
Produces S-parameter data



	Name	Value	Unit	Evaluated Value
a	$cap_w	300um-2*$shell_thk		280um
b	$cap_h	300um-2*$shell_thk		280um
c	$cap_l	600um-2*$shell_thk		580um
d	$shell_thk	10	um	10um
e	$shell_depth	120	um	120um
f	$center_h	$cap_h/2		140um
g	$plate_thk	1	um	1um
h	$plate_sep	1.4	um	1.4um
i	$plate_clear	80	um	80um
j	$shell_gap	35	um	35um
k	$nPlate	64		64

Figure 5 – HFSS 3D MLCC Model

Source: "Designing DC-Blocking Capacitor Transitions to Enable 56Gbps NRZ & 112Gbps PAM4," DesignCon 2018

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Summary and Conclusions

- Capacitor ESR represents the combined conductive and dielectric losses
- The frequency dependency is a complex function of material and geometry
- High-density ceramic capacitors can exhibit secondary resonances and piezo effect
- ESR variation drives up PDN worst-case transient noise
- Secondary effects can be simulated by 2D and 3D models

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