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Advanced Test Fixture Design

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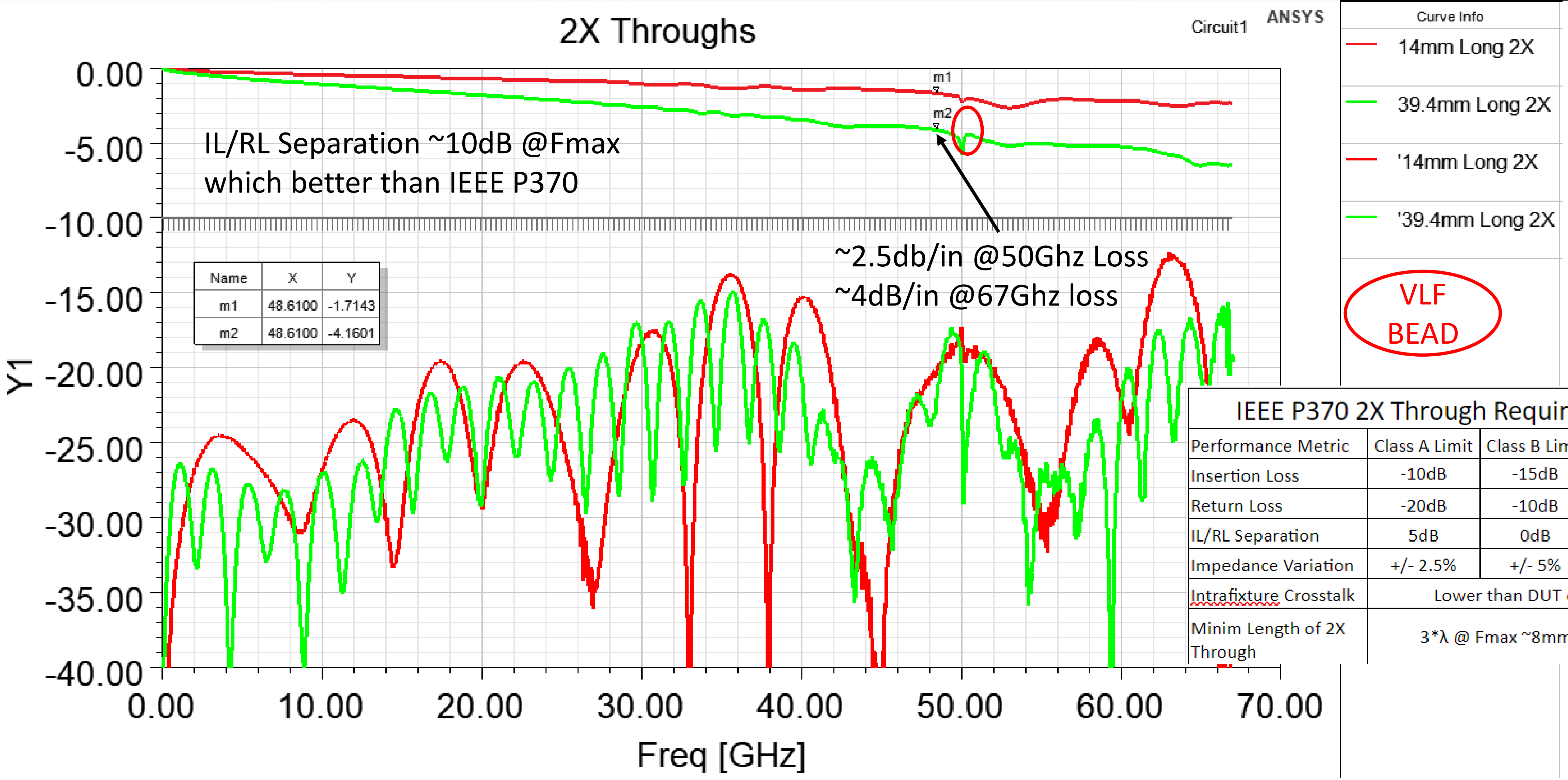
INTRODUCTION

The purpose of today's discussion is to demonstrate techniques necessary for successful SI test fixture design.

- **Some key points:**
  - IEEE P370
    - Return Loss margining vs. Insertion Loss an your 2X through
  - Transparent test fixtures are key to your program's success
    - Perfect launches
  - Tips and tricks to mitigate common design problems
    - Phase matching bends
    - Weave induced skew
    - Periodic loading
  - Bert/Serdes testing vs. S-parameter measurements & de-embedding
  - Key elements for making fully de-embedded measurements

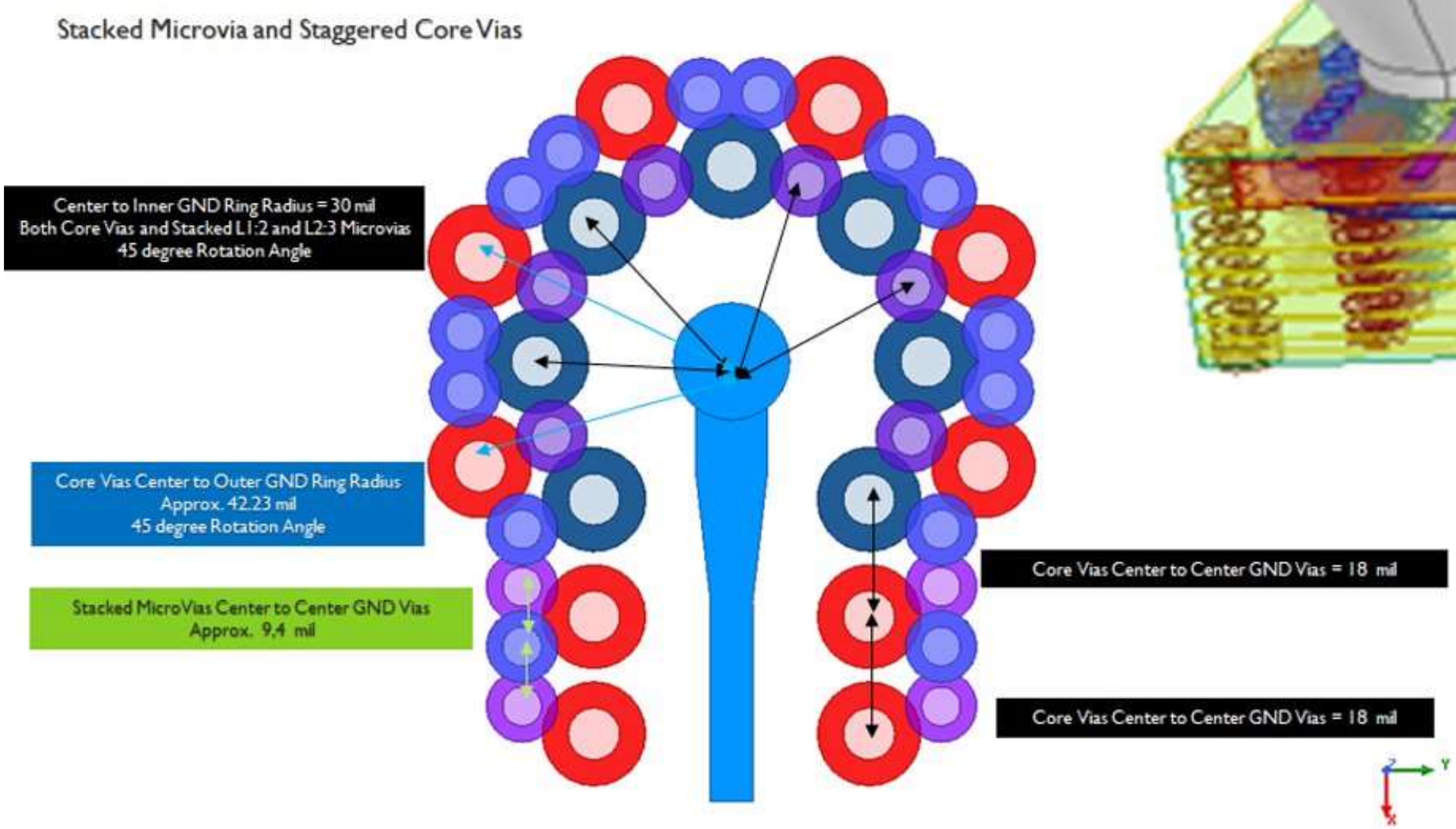
IEEE P370: Tachyon 100G Test Fixture

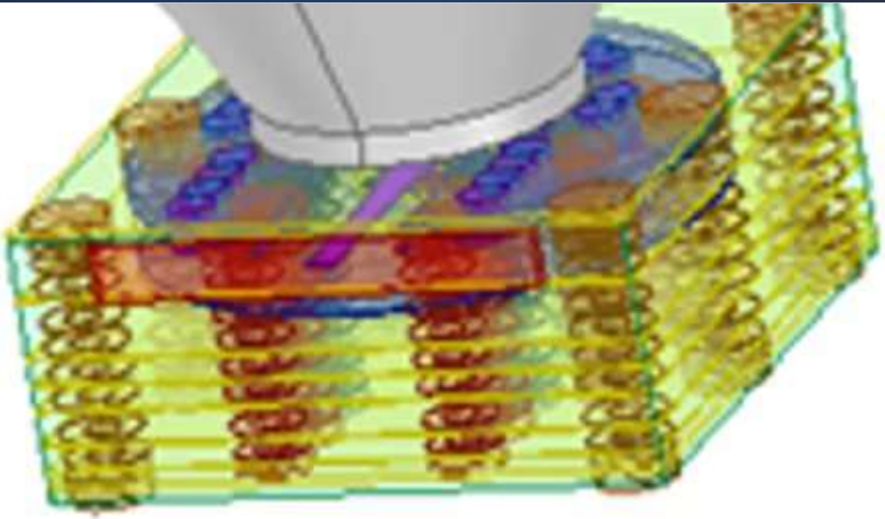


IEEE P370 2X Through Requirements

Performance Metric	Class A Limit	Class B Limit	Class C Limit
Insertion Loss	-10dB	-15dB	-15dB
Return Loss	-20dB	-10dB	-5dB
IL/RL Separation	5dB	0dB	0dB
Impedance Variation	+/- 2.5%	+/- 5%	+/- 10%
Intrafixture Crosstalk	Lower than DUT crosstalk		
Minim Length of 2X Through	3*λ @ Fmax ~8mm @ 67Ghz		

Transparent Test Fixtures: Vertical Launches





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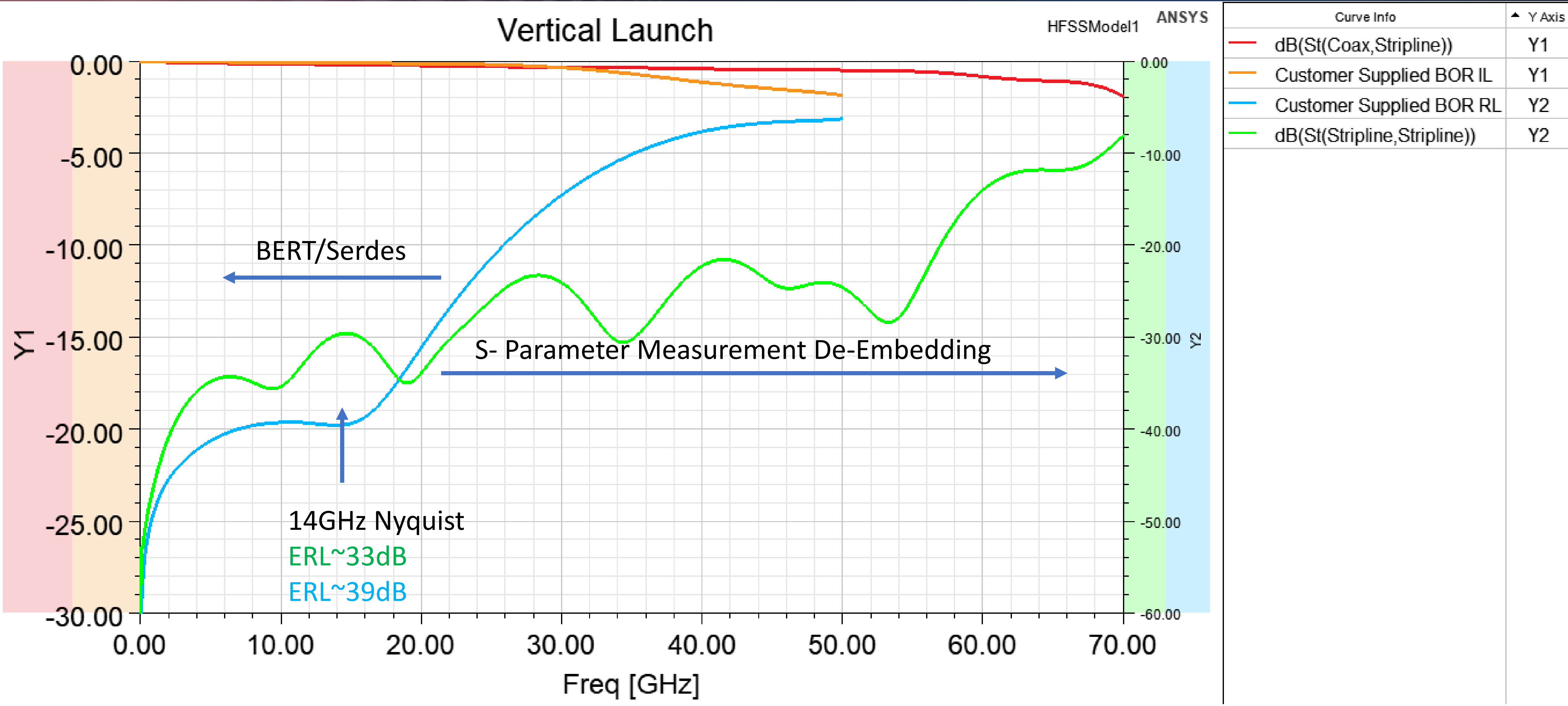
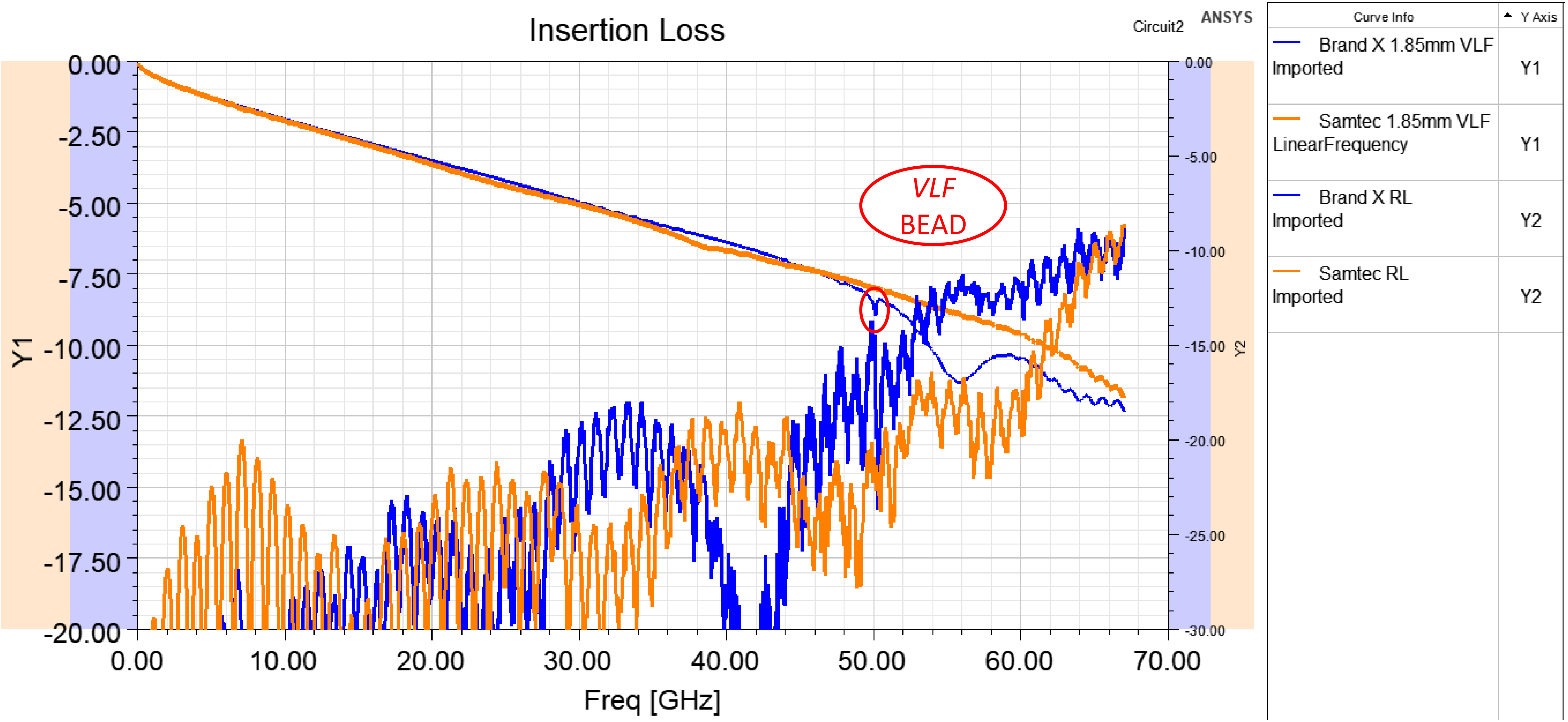
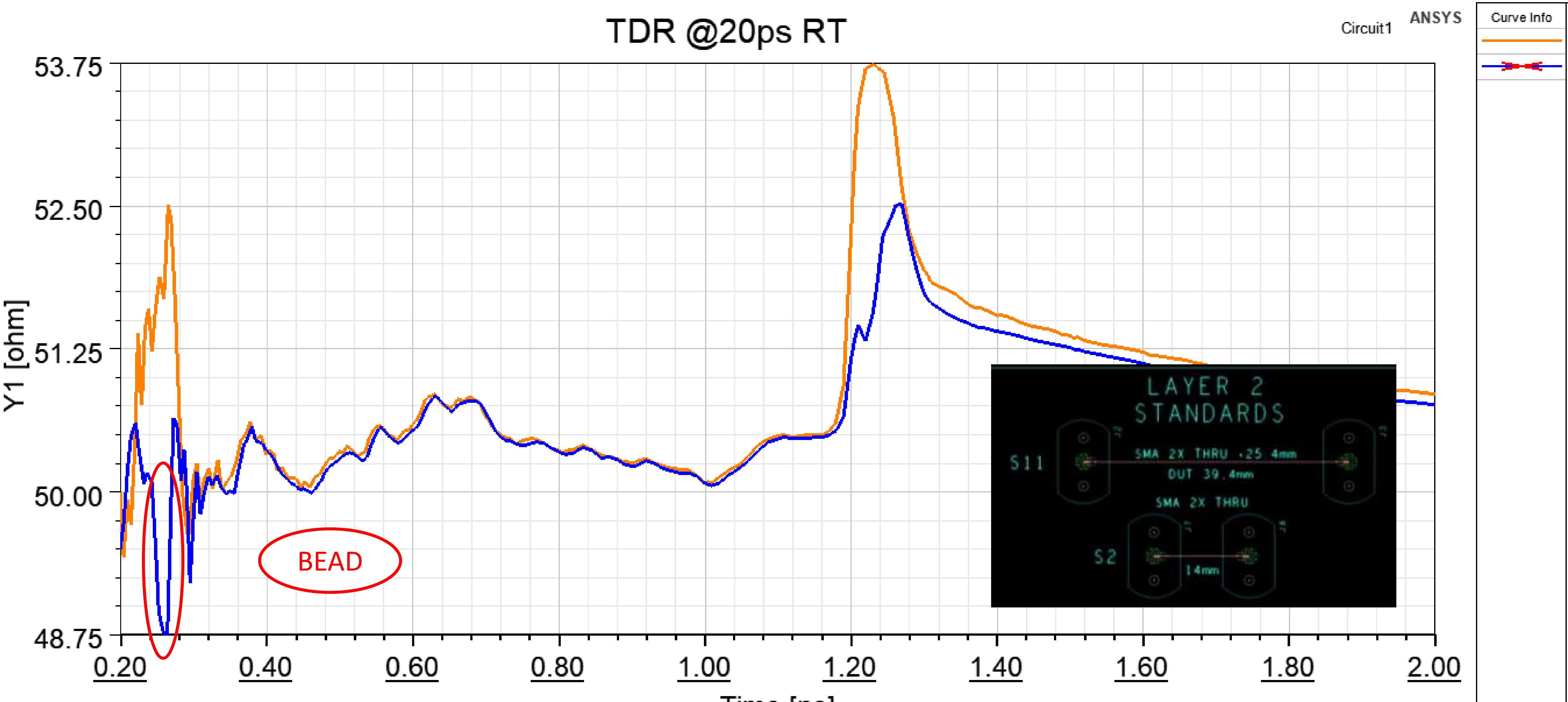


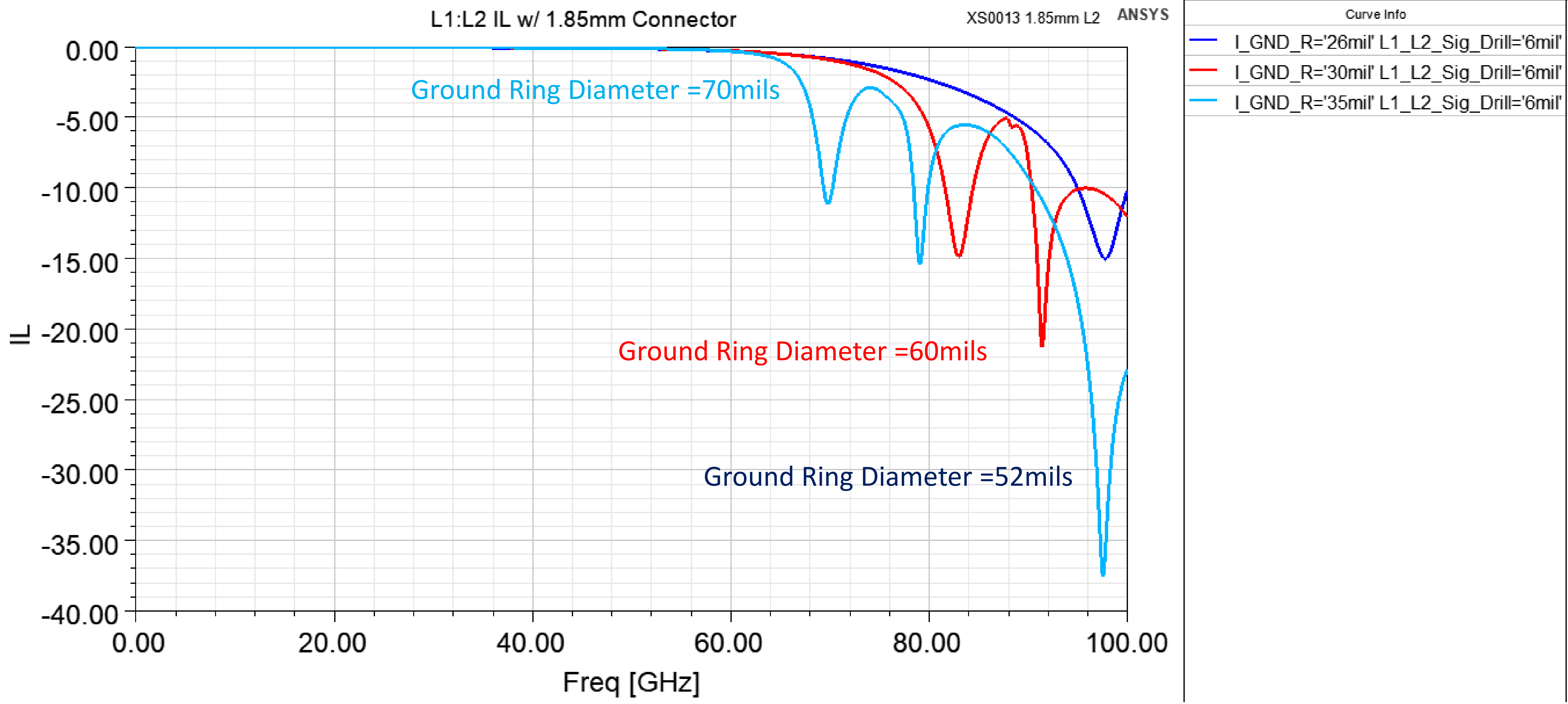
Bead Issues: Same Exact Test Structure



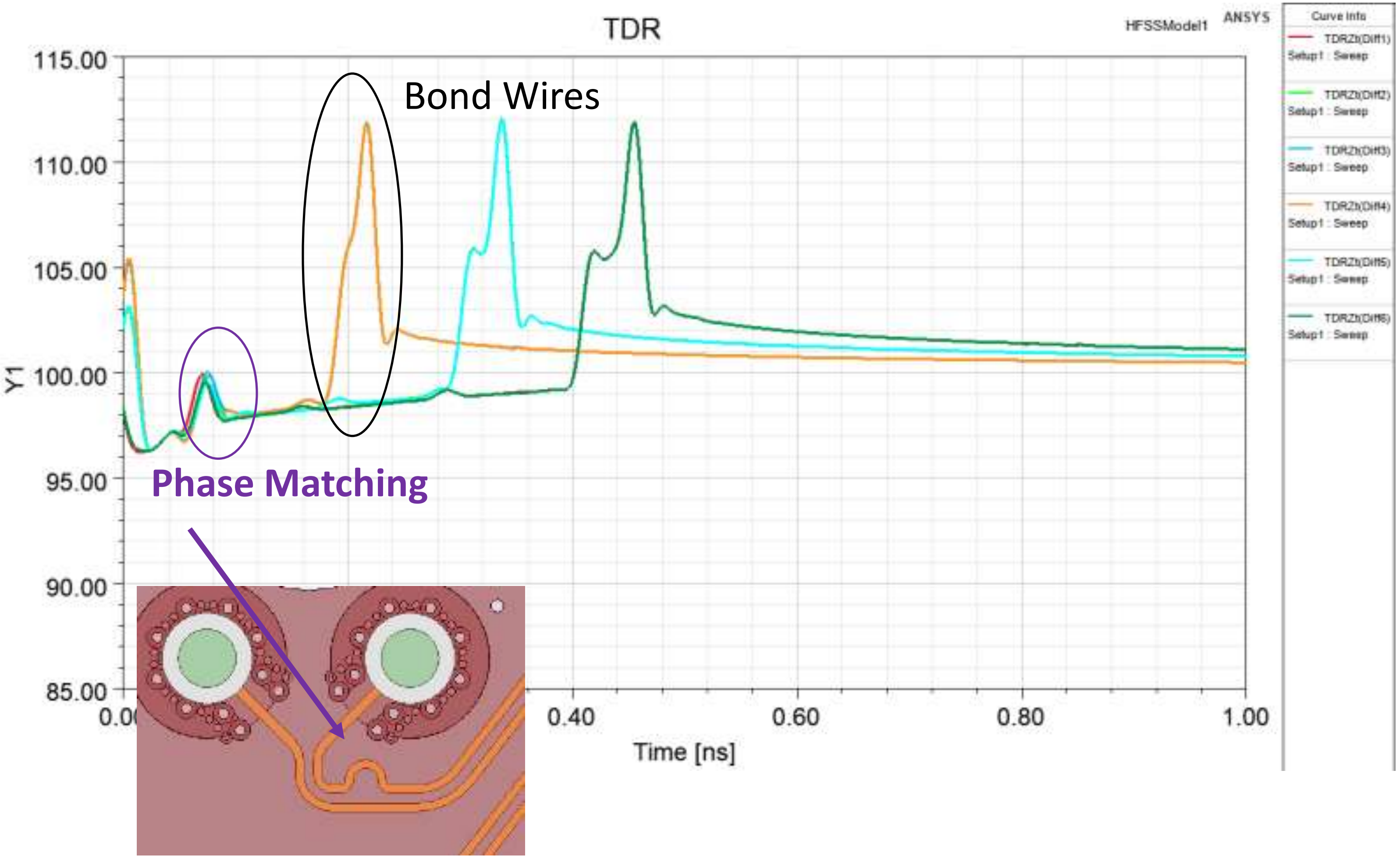
TDR Tea Leaves: Tachyon 100G Test Fixture



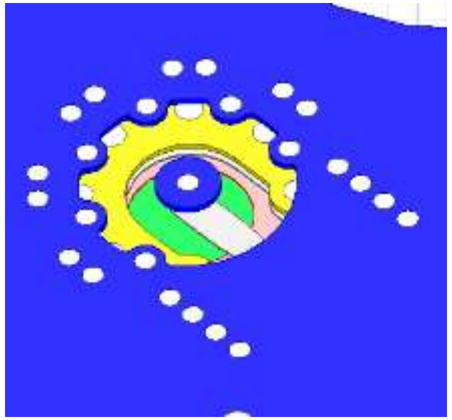
VLF: Cavity Resonance



Tips and Tricks: Phase Matching Bends



0.25mm Radius



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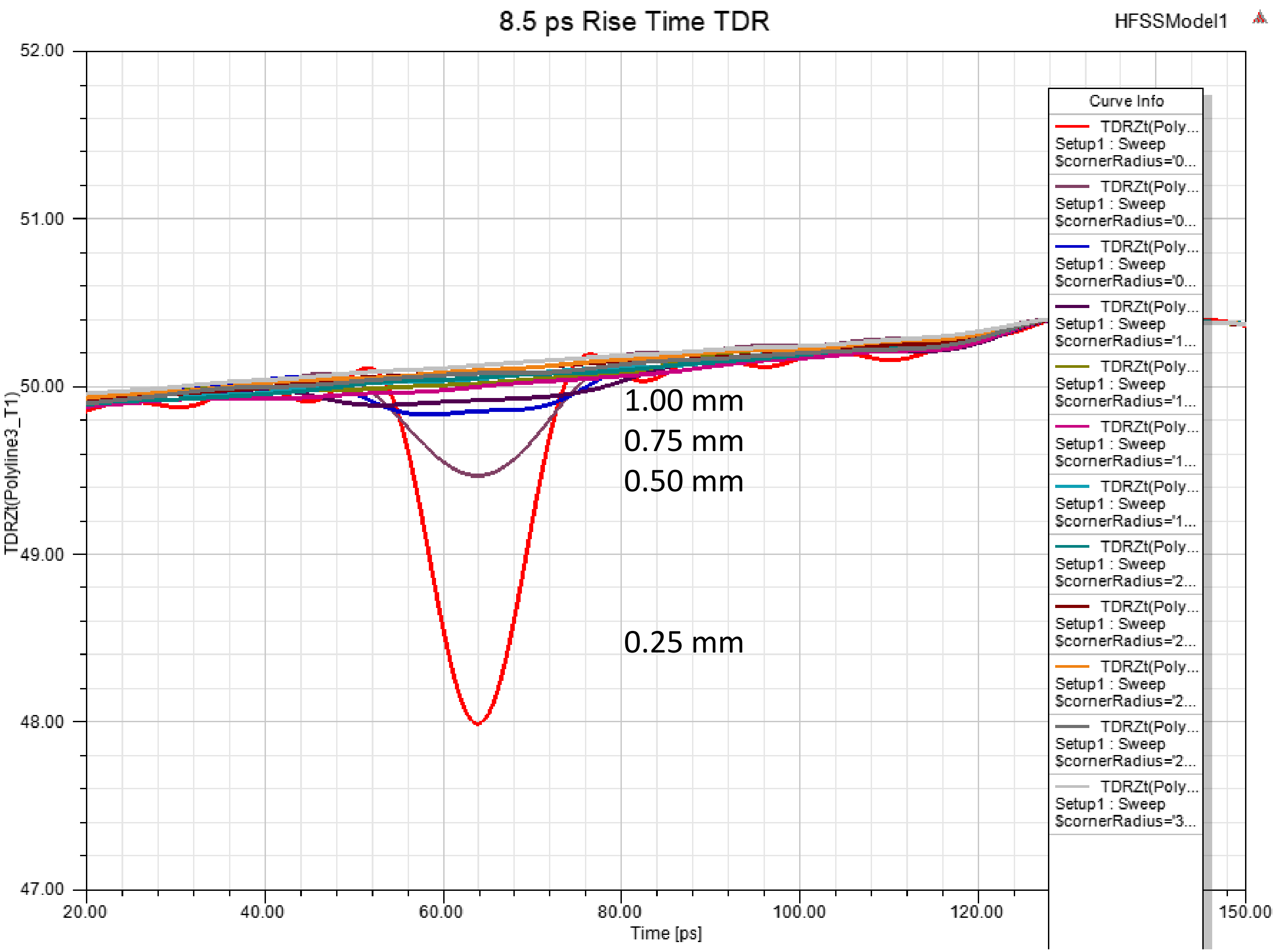
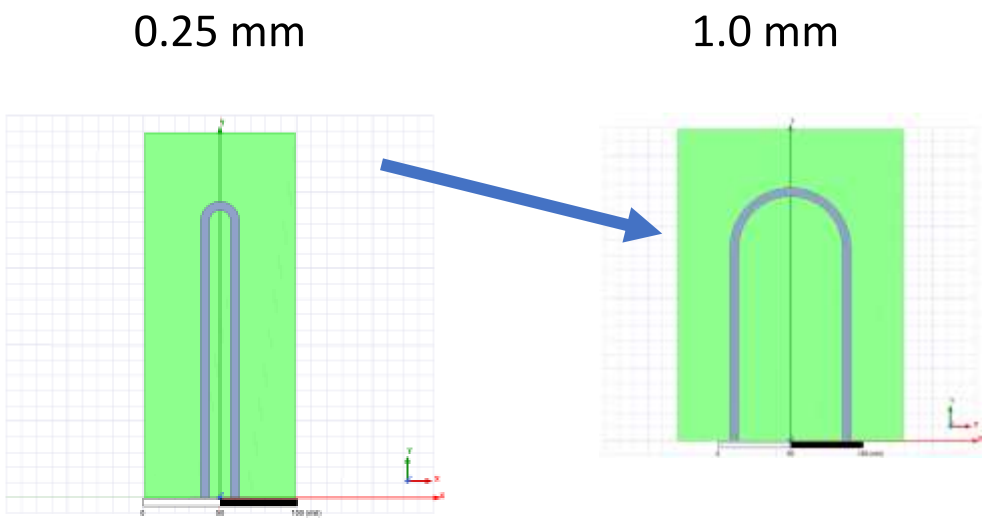
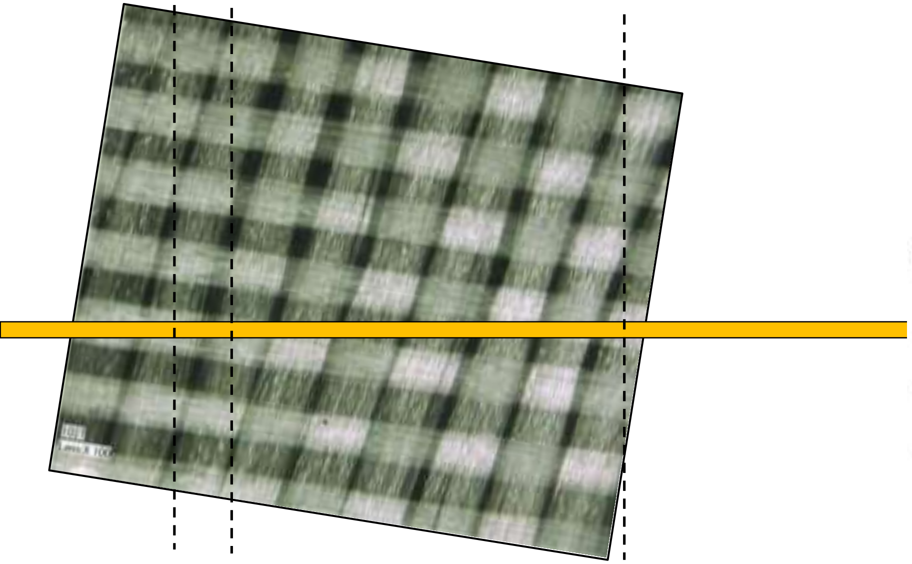




Tips and Tricks: Weave Induced Periodic Loading

Period Fill

Period Grain

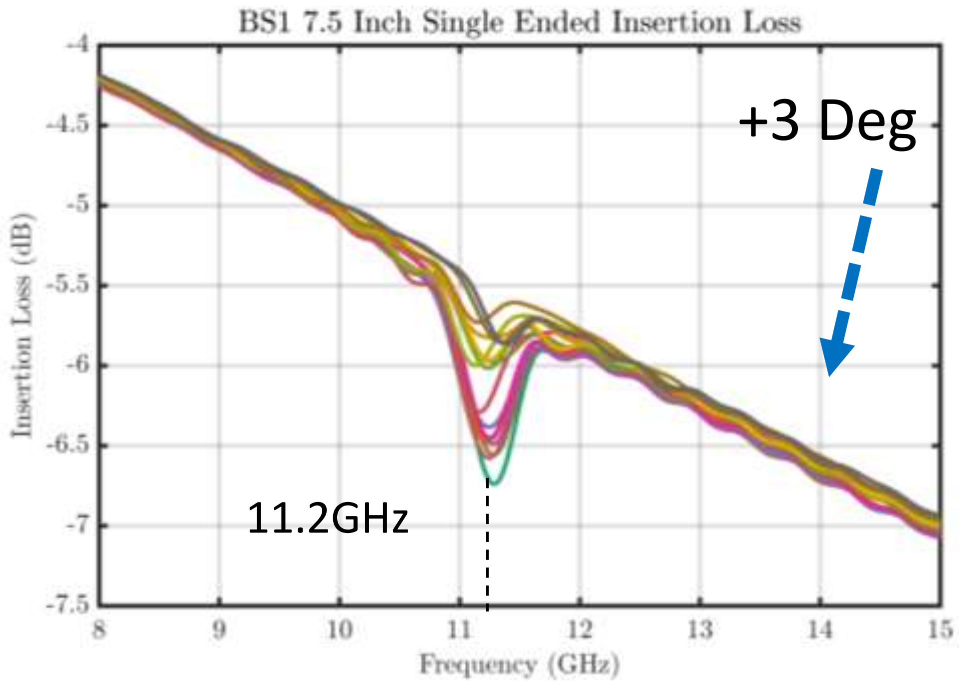


1035 Weave Pitch ~16.1X15.5 mils

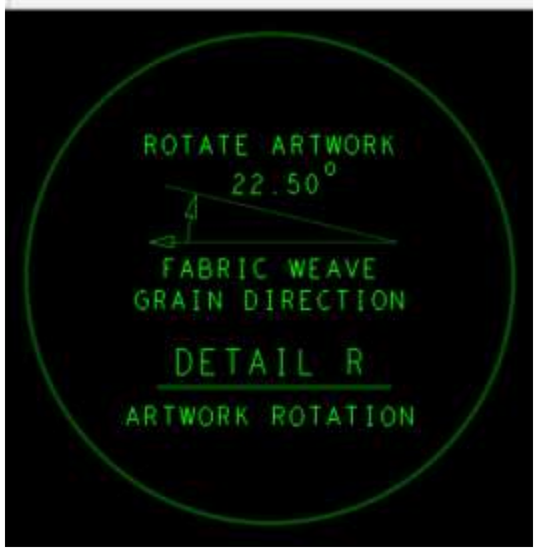
$$Period = \frac{Pitch_{GRAIN}}{\sin(rotation)}$$

$$f_{res} = \frac{c}{2 \times Period \times \sqrt{\varepsilon_r}}$$

Bloch Notch Resonance



Add grain direction screen shot. Symbol.



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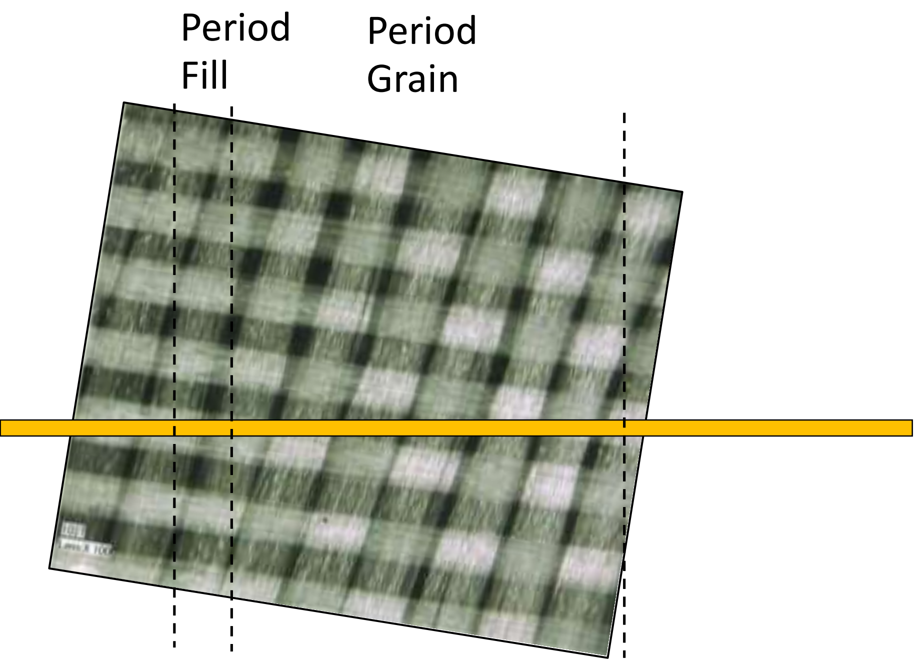

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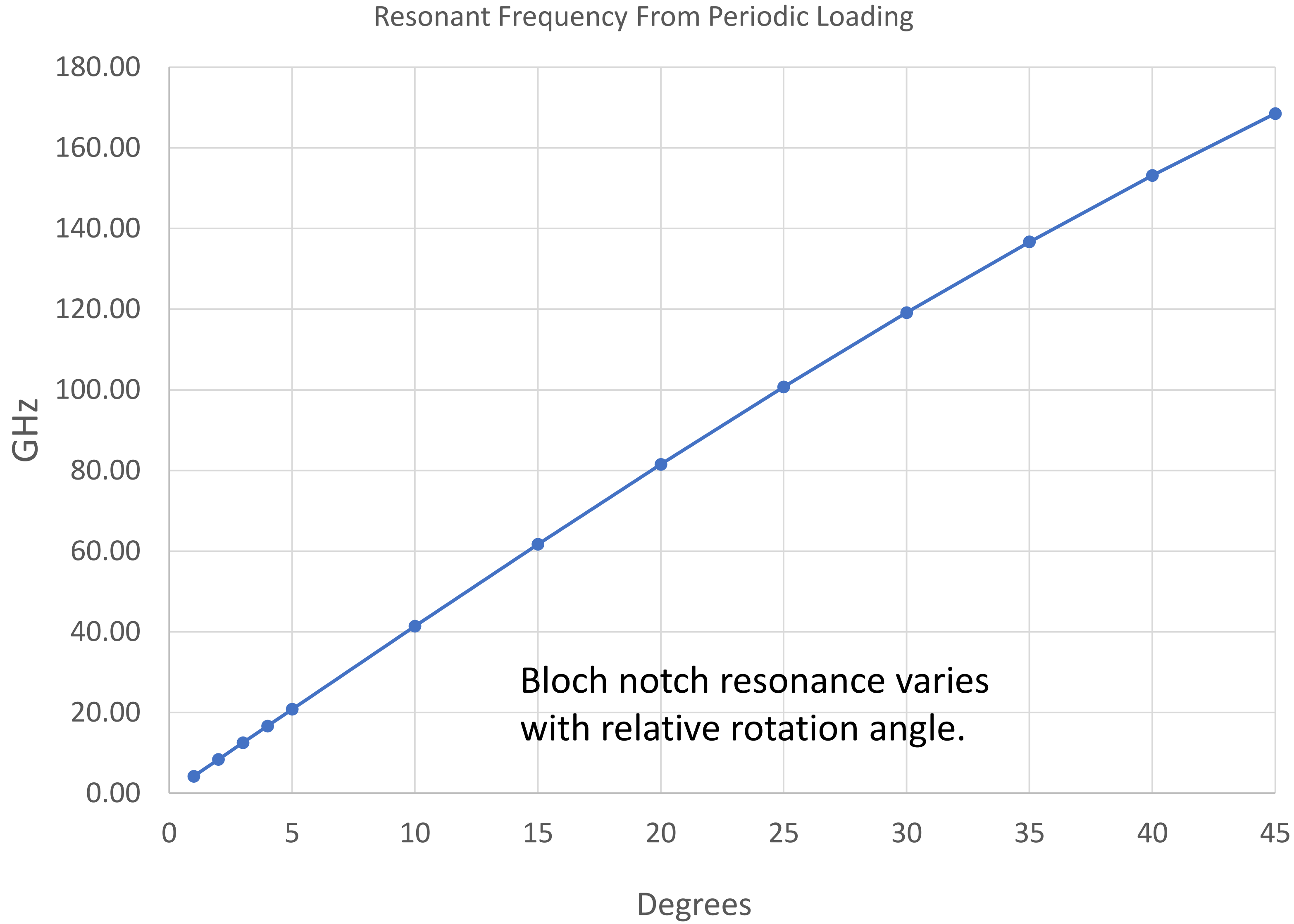
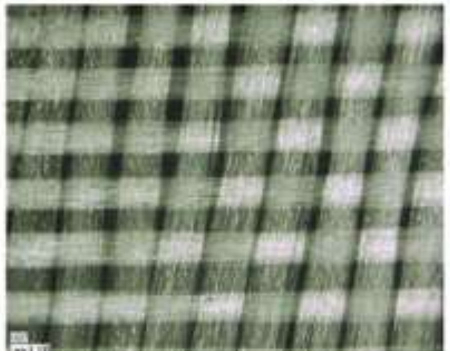
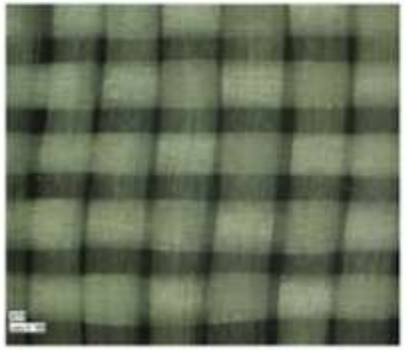


Differential Pairs on Weave ½ Pitch



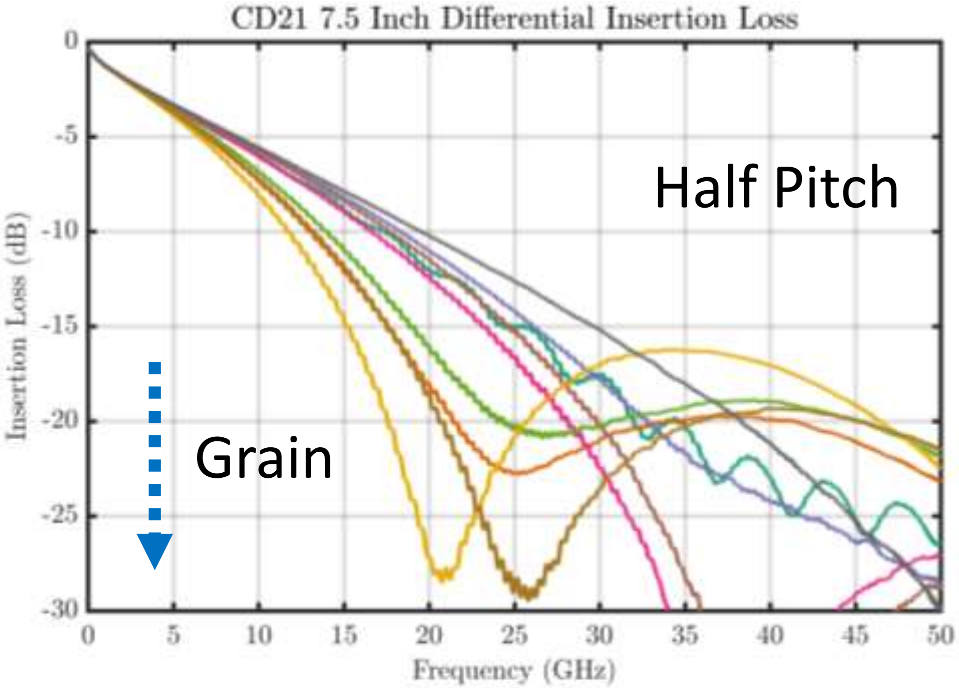
1035
Warp & Fill Count: 66 x 68 (ends/in)
Thickness: 0.0011" / 0.030 mm

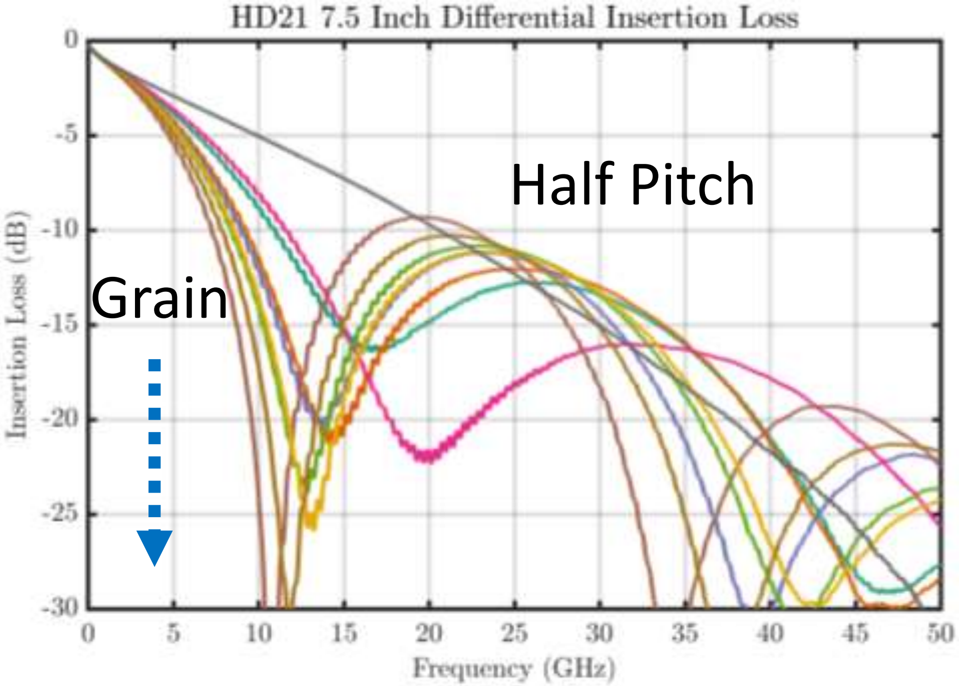
Weave Pitch ~16.1X15.5 mils



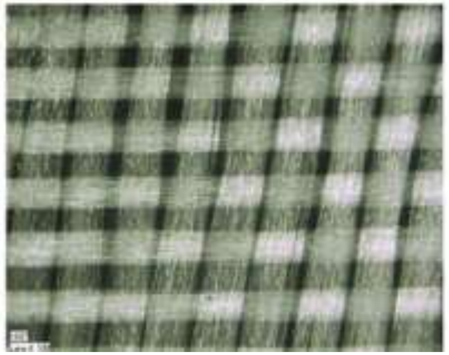
1078
Warp & Fill Count: 54 x 54 (ends/in)
Thickness: 0.0017" / 0.040 mm

Weave Pitch ~16.5X17.8 mils





Differential Pairs on Weave on Pitch



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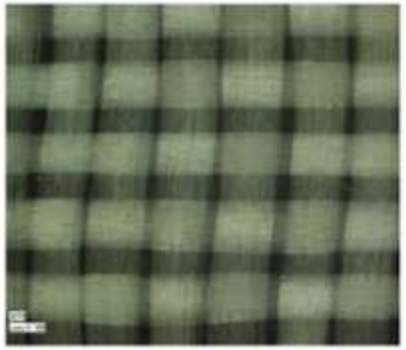

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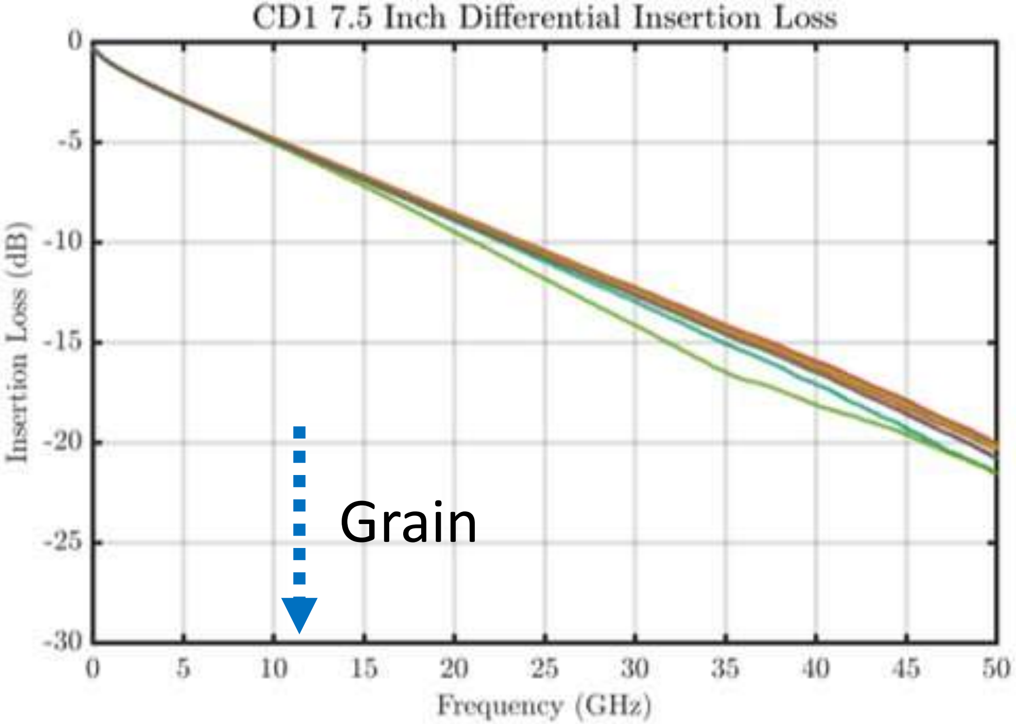

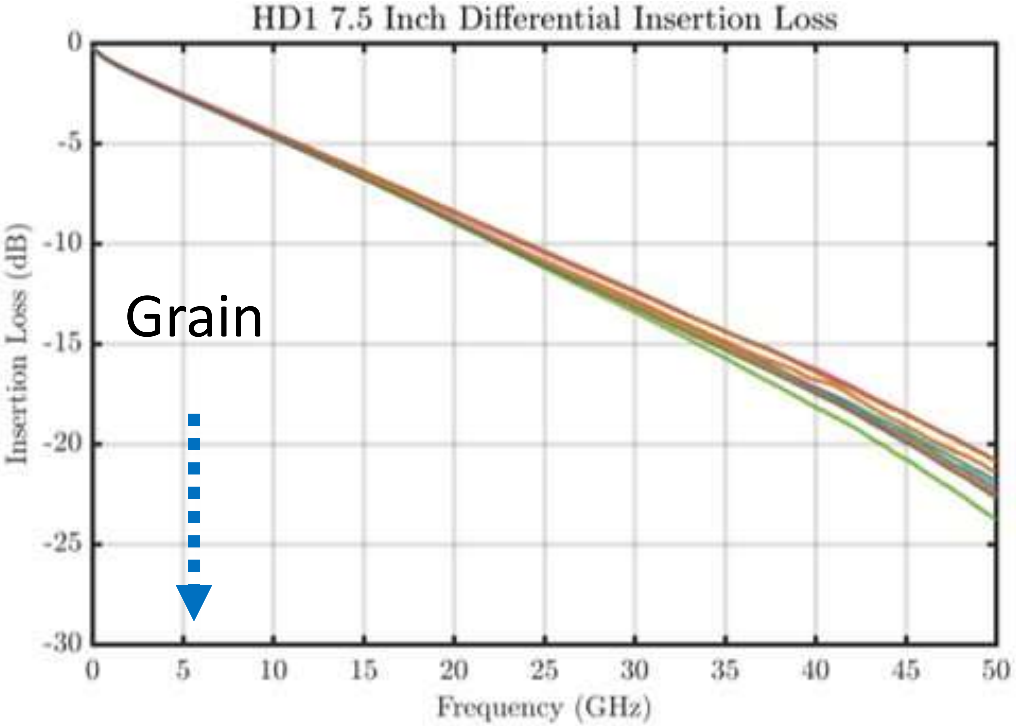

Test Fixture Bert vs. S-parameter Extraction

- Bert Testing
  - Keep losses to a minimum
  - Reduce reflections
  - DC blocks
  - Emphasis on ERL at Nyquist then only up to 1.5*Nyquist
  - Maximizing COM (emphasis on minimal cross talk)
- S-parameter extraction is the underlying premise behind IEEE P370
  - 2X throughs are identical to the test paths
  - Device S-parameters are extracted by moving the reference plane closer to them via the 2X through(s)
  - Insertion Loss vs. Return Loss separation should be >5dB, 10dB provides high confidence de-embedding

Key Elements for Success

- Launches should be perfect and repeatable
- Any transmission line structure change should be carefully designed
- High quality materials are a must
- Artwork rotation WRT weave must be managed
- Registration issues do impair launches and must be considered during the design
- Etch tolerance makes achieving a perfect 50 ohms unlikely…
- Solder mask is not your friend

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SUMMARY

1. Elements of a transparent test fixture
2. A lot can and will go wrong!
    1. Registration Errors
    2. Etching tolerances
    3. Fabricator processing of copper
    4. Be wary of solder mask
3. Trace Losses are becoming dominant contributors as design frequencies push higher

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