Successful PCIe® Interconnect Guidelines at 8, 16, and 32 GT/s

Presenter: Steve Krooswyk
Introduction

• We face an increasing pressure to improve system interconnect at each data rate bump

• Optimizations for loss, reflection and crosstalk are up for consideration

• But we have questions, how much is enough?

• And when should we run channel simulation?

• Let’s answer these questions and review high speed design considerations that apply to PCIe®
Agenda

• High Speed Interconnect Reminders: Transmission Lines & Vias
• PCIe® Connector and Cable Considerations
• Solution Space Discussion: Paper Calculations or Simulation?
• Simulation Examples and Topology Solutions
## PCIe® Generations

<table>
<thead>
<tr>
<th>PCIe® Generation</th>
<th>Data Rate</th>
<th>Total Budget</th>
<th>Add in Card Budget</th>
<th>Reach Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe® 3.0</td>
<td>8 GT/s</td>
<td>23.5 dB</td>
<td>6.5 dB</td>
<td>20-inch and standard PCB</td>
</tr>
<tr>
<td>PCIe® 4.0</td>
<td>16 GT/s</td>
<td>28.0 dB</td>
<td>8.0 dB</td>
<td>16-inch on mid-range PCB material</td>
</tr>
<tr>
<td>PCIe® 5.0</td>
<td>32 GT/s</td>
<td>36.0 dB</td>
<td>9.5 dB</td>
<td>14-inch on low-loss PCB material</td>
</tr>
</tbody>
</table>

*Up to 0.85 dB/inch at 4GHz*
Dissipation factor > 0.018
Standard FR4

*Up to 1.4 dB/inch at 8GHz*
Dissipation factor < 0.015
IT180 370HR etc.

*Up to 1.0 dB/inch at 16GHz*
Dissipation factor < 0.010
Megtron 6 I-Tera MT40
Transmission Lines

Glass Weave Management
- Skew appears on SDD12 at 2 GHz
- Zigzag routes or route @ glass pitch

gEEk® spEEk May 21, 2020 – Quantifying Glass Induced Skew on PCBs

Surface Roughness
- Smoother copper may not be required on shorter, lower speeds
- Significant impact at Gen4+
- Evolving modeling methods (DesignCon papers)

15" Transmission Line on mid-range material: ER=3.3, tanD=0.010

<table>
<thead>
<tr>
<th></th>
<th>PCIe® 3.0 - 4 GHz</th>
<th>PCIe® 4.0 - 8 GHz</th>
<th>PCIe® 5.0 - 16 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Foil (7-14um)</td>
<td>-6.9 dB</td>
<td>-12.3 dB</td>
<td>-21.8 dB</td>
</tr>
<tr>
<td>VLP (1-3um)</td>
<td>-6.4 dB +7%</td>
<td>-11.2 dB +9%</td>
<td>-19.9 dB +9%</td>
</tr>
<tr>
<td>HVLP (&lt;1um)</td>
<td>-6.1 dB +12%</td>
<td>-10.6 dB +14%</td>
<td>-18.8 dB +14%</td>
</tr>
</tbody>
</table>
Transmission Lines: The Bottom Line on 85 Ohms

- 85 ohms required for interoperable systems and cards
- 85 ohms does not apply to packages
- PCB for captive, or custom, systems do not require 85 ohms
- Connectors do not require 85 ohms
- Cables are not bound to 85 ohms

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gEEk® spEEk April 30, 2020 – PCI Express: is 85 Ohms Really Needed?
Transmission Lines

Solder mask: conformal vs. blanket
- 1 ohm impedance
- A brief model review has found impact loss by 2%, crosstalk by 4%

Plating height – microstrip is not all trapezoidal

Vs.
Metal layer fills with resin from prepreg during press
- Expect dk for pockets between 2.8-3.0
- Prepreg properties on metal later is optimistic loss and crosstalk
- TDR: 1-2 ohms difference

Impact scales with ratio of prepreg dk : resin dk
PCle 3 Stack Up (Hk=3.2; Low DK in Metal Layer)
PCle 5 Stack Up (Hk=3.2; Low DK in Metal Layer)
Transmission Lines: Environmental

Temperature and Humidity

- Neglected environment in models or lab may lead to surprises
- Up to 30% in worst case measurement; consider 10-20% in modeling
- Expect localized hot spots
- Microstrip is worst

<table>
<thead>
<tr>
<th>Nominal Loss (dB/inch at 4 GHz)</th>
<th>Microstrip Worst Case 75°C dB/inch (percentage increase)</th>
<th>Stripline Worst Case 75°C dB/inch (percentage increase)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.40</td>
<td>0.50 (25%)</td>
<td>0.48 (19%)</td>
</tr>
<tr>
<td>0.44</td>
<td>0.54 (23%)</td>
<td>0.52 (17%)</td>
</tr>
<tr>
<td>0.5</td>
<td>0.60 (20%)</td>
<td>0.58 (15%)</td>
</tr>
<tr>
<td>0.6</td>
<td>0.70 (17%)</td>
<td>0.68 (13%)</td>
</tr>
<tr>
<td>0.7</td>
<td>0.93 (32%)</td>
<td>0.90 (29%)</td>
</tr>
<tr>
<td>0.8</td>
<td>1.03 (28%)</td>
<td>1.00 (25%)</td>
</tr>
</tbody>
</table>

Note: Decibels per inch (dB/inch) is measured at 4 GHz.

Zhang H, Ou J, Krooswyk S. High Speed Digital Design - Design of High Speed Interconnects and Signaling
Via Design Considerations: Impedance

- **First order optimizations**
  - Closely coupled pair and oval anti-pads
- **Second order**
  - Uniquely tuned anti-pad by-layer
- **Lastly,**
  - Laser\CCD drill, back drill
  - Drill and pad diameter reductions

### First Order Optimizations:
- Radius 20 mil
- Drill diameter 10 mil; Pad diameter 20 mil

### Second Order:
- Unique and larger antipads on planes adjacent to pads
  - And/or backdrills

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**Should we use simulation to optimize the via?**

**If we do not, how much stub is tolerable?** (10/20/30 drill/pad/anti)

<table>
<thead>
<tr>
<th>PCIe®</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe® 3</td>
<td>Not necessary, stubs &lt;=80mils no problems</td>
</tr>
<tr>
<td>PCIe® 4</td>
<td>Optimization may help via stubs 50 mils and larger</td>
</tr>
<tr>
<td>PCIe® 5</td>
<td>Expect optimization simulation for all via designs</td>
</tr>
</tbody>
</table>

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**Return Path Crosstalk**

Don’t forget the grounds.
Via Design Considerations: Stub vs. Xtalk

Two via designs considered – what’s best?
- We often neglect the crosstalk in the shorter via stub
- Consider SNR to make decisions, e.g., ICR

More significant issue in space-constrained BGA fields where back drill may not be possible
- Greater concern for NEXT

Two Breakout Options

- Better Reflection
  - More Crosstalk

- Worse Reflection
  - Less Crosstalk

Long Stub
- ~60 mils

Short stub,
- Greater vertical coupling

Differential IL: Via Stub Length Comparison: Dense BGA Field

Differential FD NEXT PowerSum: Via Stub Length Comparison: Dense BGA Field (2)
Via Design Considerations: Placement

- **Boomerang Via**
  - Addition of small via is negligible compared that large THM\PFT stub on Gen3-4 designs
  - No additional via for capacitor!

- **Keep Surface Transitions Short**
  - Keep lengths to 0.5 inch or less w/o caps
  - Crosstalk + independent Z variable

- **Surface Breakout Advantages:**
  - Mid-channel vias are more easily optimized
  - Easy capacitor placement

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- **Slot**
  - THM/PFT
  - Difficult optimize / cannot drill

- **Boomerang**
  - 0.5" SMT
  - 2-3" SMT
  - 0.1" SMT
Connector Selection: CEM Interface

- Move to Surface Mount at Higher Speeds
  - At Gen4, some TH\PFT may still be possible

- FD Limits for CEM Interface
  - IL, RL, Crosstalk

- New Crosstalk Compliance Approaches at PCIe® 5.0
  - Recognize pin maps in FEXT+ NEXT Power Sums
  - Compliance by integrated crosstalk

Connector Selection: Non-CEM \ Captive

- Specification guidance is validation thru channel compliance (simulated eye height and width)

This feels a lot of burden, why don’t CEM FD limits apply?

- Other form factors are taller – having more loss and lower resonances, with more pins and noise

- Anecdotal recommendations:

  - **Insertion Loss:**
    - Up to 1.5-2.0 dB reasonable, see what PCB budget allows

  - **Return Loss:**
    - Even up to -5 dB at Nyquist may be only moderate degradations

  - **Impedance:**
    - Component does not need to be 85
    - More than +/-10% is easily okay

Examples: Don’t Judge a Bit Just by its Fourier – 112 Gbps PAM4 Component Optimization and Selection, DesignCon 2019, S. Krooswyk, M. Rengarajan

For PCIe® 5, use ccICN to compare

gEEk® spEEk April 30, 2020 – PCI Express®: is 85 Ohms Really Needed?
Cable Considerations

• Cable Loss Advantage for Longer Reach
  – Relatively temp & humidity insensitive
  – High value for all generations

Table: Raw 34 Gauge Cable Conversion at Nyquist

<table>
<thead>
<tr>
<th>Standard</th>
<th>PCB Length</th>
<th>Cable Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe® 3.0 Standard Loss PCB</td>
<td>10&quot; PCB</td>
<td>85&quot; Cable 34 Gauge</td>
</tr>
<tr>
<td>PCIe® 4.0 Mid-Loss PCB</td>
<td>10&quot; PCB</td>
<td>94&quot; Cable 34 Gauge*</td>
</tr>
<tr>
<td>PCIe® 5.0 Low-Loss PCB</td>
<td>10&quot; PCB</td>
<td>55&quot; Cable 34 Gauge</td>
</tr>
</tbody>
</table>

*Smaller increment from Standard to Mid Loss PCB, than Mid to Low 1-inch of 34-Gauge Twinax is 0.20 dB at 16GHz.

• Positions for side bands – know your features 2-8 pins per port
• Optimal impedance?
  – the mating connector is the greatest factor
  – lower losses in 100 ohm twinax
  – EH\EW simulations better @ 100 ohm
  – see... gEEk® spEEk April 30, 2020 – PCI Express®: is 85 Ohms Really Needed?

• Greater Interest for PCIe® 4.0/5.0 where PCB Solution Space is Reduced
• Avoid PCBs for Better Return Loss
Cable Reach Example: PCIe® 5.0

13" PCB Channel
18" Total Channel
66" Total Channel

13" PCB 1-conn:
31.1mV/0.48UI

0.25m Cable, 3-conn:
32.9mV/0.5UI

1.5m Cable, 2-conn:
32.4mV/0.6UI

Spec Min: 15mV/0.3UI

Stripline 3x separation crosstalk models; PCIe® 5 via not included.
Channel Analysis Steps: Top-Down Approach

- At the top – easiest analysis first
- Step down the pyramid to mitigate risk
- Increasing effort towards bottom

First Principles: Loss Budget
Simulation: Nominal
Simulation: Corners
Simulation: Statistical

Resources
First Principles: Loss Budget

- Initial pass at channel compliance
- No simulation needed
- Spreadsheet based calculations
- Stop gap to identify channels with too much insertion loss
- Specification is not normative about loss – common to see PCIe® 3.0/4.0 channel simulation complaint slightly beyond loss target
First Principles: Loss Budget Example

- Reasonable budget calculations for all three generations
  - Validated with simulation
- Package losses per spec
- Card losses are informative
- At PCIe® 4.0 and above, a remainder must exist for reflection and crosstalk noise missed on paper

<table>
<thead>
<tr>
<th></th>
<th>PCIe® 3.0</th>
<th>PCIe® 4.0</th>
<th>PCIe® 5.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Target</strong></td>
<td>23.5 dB</td>
<td>28 dB</td>
<td>36 dB</td>
</tr>
<tr>
<td><strong>PCB</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Main Board</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8 db\inch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.35 db\inch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.1 db\inch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12.8 @ 4 GHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13.5 @ 8 GHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 @ 16 GHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>RC Package</strong></td>
<td>3.5</td>
<td>5</td>
<td>8.5</td>
</tr>
<tr>
<td><strong>Vias, Caps</strong></td>
<td>0.5</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td><strong>Connector (Spec)</strong></td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
</tr>
<tr>
<td><strong>4&quot; Card Budget</strong></td>
<td>6.5</td>
<td>8.5</td>
<td>9.5</td>
</tr>
<tr>
<td><strong>Reflection &amp;</strong></td>
<td>negligible</td>
<td>&lt; 1</td>
<td>4</td>
</tr>
<tr>
<td><strong>Crosstalk Penalty</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>23.8 dB</td>
<td>28.5 dB</td>
<td>36 dB</td>
</tr>
</tbody>
</table>
Channel Compliance Simulations

- Defined by PCI Express® Base Specification
  - Any simulation tool that adheres to requirements is acceptable
  - Phyton tool is provided to PCI-SIG members
- A compliant channel passes eye diagram in all impedance and environment corner conditions
- Reference packages are minimally compliant to loss and return loss
  - Package model crosstalk is a reference, and not a requirement
- Refine solution with device vendor models
- Channel compliance is not actually measurable, except for CEM slots
  - Captive channels may use vendor determined validation limits for on-die eye or BER
Interpreting Channel Simulation Results

Equalized channel response

Power sum is total of FEXT and NEXT

Time domain responses (same colors)

This plot, FD conversion created from time domain, may show small discrepancy from s-parameters.

Data Rate

Total: Victim + Aggressors

Adaptive EQ Results

Total Eye Opening, peak to peak, Compare to spec

EH Offset: location of maximum eye height reported value

Loss

Power sum is total of FEXT and NEXT

This plot, FD conversion created from time domain, may show small discrepancy from s-parameters.
Channel Simulation Results: Example Length Sweep, PCIe® 4.0

- Some dithering occurs in simulation results
  - Example: near +/- 1mv and 0.5 ps deviation from a smooth curve

- Sources:
  - Discrete steps in adaptive equalization
  - Reflection alignment with CDR

- Caution simulating a single-point for a small effect: could the conclusion be in the noise?

- From simulation, we can determine:

  **PCIe® 4.0 Rule of Thumb**
  
  5 mV \ 2.4 ps = 1 inch = 1.4 dB at 8 GHz
Channel Simulation Results: 
Eye Closure Slope \ Rule of Thumb

- What to do with this information?
- Apply to simulation result comparisons when asking “What is the impact”
- Translate confusing “mV impact” into meaningful loss or PCB terms
- Clarity will be given to negligible effects

PCIe® 3.0 Rule of Thumb
4mV \ 1ps = 1 inch = 0.8 dB at 4 GHz

PCIe® 4.0 Rule of Thumb
5mV \ 2.4 ps = 1 inch = 1.4 dB at 8 GHz

PCIe® 5.0 Rule of Thumb
5mV \ 0.5 ps = 1 inch = 1.1 dB at 16 GHz

Simplify Decisions:
e.g. “The cost is X mV / X ps, which is a X-inch reduction”
Sensitivity to Neck Down Regions

- Tight regions are inevitable
- If regions are FEXT (and most are), there is no location sensitivity ✓
  - Occurrence near Tx, or near Rx, is no different
- Short regions of tight spacing are acceptable for shorter durations
- Let’s review two excursions:
  - Stripline at 2x dielectric thickness
  - Microstrip at 5x dielectric thickness

Dielectric thickness is taken for nearest reference plane.
Sensitivity to Neck Down Regions: Stripline, by PCIe® Version

2.5mV impact? Rule of thumbs:
That's 0.5-inch solution reduction

Duration of 2x neck down routing: 0, 0.2, 0.5, 1, 2, 5"
Total length constant

TAKE AWAY
PCIe® 3 is agnostic to significant 2x neck down length
PCIe® 4 is insensitive up to 1-inch of 2x neck down
Sensitivity to Neck Down Regions: Microstrip, by Generation

**Variability Gauge**

**Variability Chart for EH(mV)**

Duration of 5-7x neck down routing: 0, 0.2, 0.5, 1, 2, 5"

**Variability Gauge**

**Variability Chart for EW(UI)**

Total length constant

**TAKE AWAY**

PCle® 3: 5x negligible up to 1"
PCle® 4: 5x negligible up to 0.5"
PCle® 5: 5x negligible up to 0.2"
**Overall Topology Guidelines**

**Option 1 (Stripline)**
- **PCle® 3.0**: 16" .8db\ in
  - Stubs: <= 80 mil
  - PFT Conn Stub: <= 80
  - 3x Stripline Space
- **PCle® 4.0**: 10-12" 1.4db\ in
  - Stubs: <= 60 mil
  - SMT Conn
  - 3x Stripline Space
- **PCle® 5.0**: 10" 1.0db\ in
  - Stubs: managed
  - 3x Stripline Space

**Option 2 (Mixed)**
- **PCle® 3.0**: 16" .85db\ in
  - Stubs: <= 80 mil
  - 9x Microstrip
  - Space
- **PCle® 4.0**: 9-10" 1.4db\ in
  - Stubs: <= 60 mil
  - 11x Microstrip
- **PCle® 5.0**: 8-9" 1.0db\ in
  - Stubs: managed
  - 11x Microstrip
Repeater Considerations: Two Types

**Re-Timers**
- A2D, D2A Conversion
- Re-Clocked
- Up to 2x channel reach
- Full channel capability available before AND after
- Specification supporting 2 re-timers for PCIe® 4.0
- Reference pinmap

**Re-Drivers**
- Analog equalizer configs validated in lab
- ~30% channel reach increase
- Ideal for captive channels
- May not support open interchangeable slots
- Adaptive TXEQ phases disabled

Summary

• As expected, greater efforts are needed with higher speed, however the challenges are not insurmountable
  – With hope, this tutorial better equips designers
• Some reminders...
• Critical considerations for transmission lines include roughness and the environment
• PCB, cable, and connector impedance need not always be 85 ohms
• PCB: cable physical displacement is significant for all generations
• Repeaters include re-timers and re-drivers, for which there are many differences
• Non-CEM connectors have no guideline – so we’ve offered one
• Channel simulation EH\EW is not always intuitive – decisions are best communicated as PCB-reach or loss
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