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**ERL Part 2 – Practical Use of ERL to Optimize
Interconnect/BOR Design**

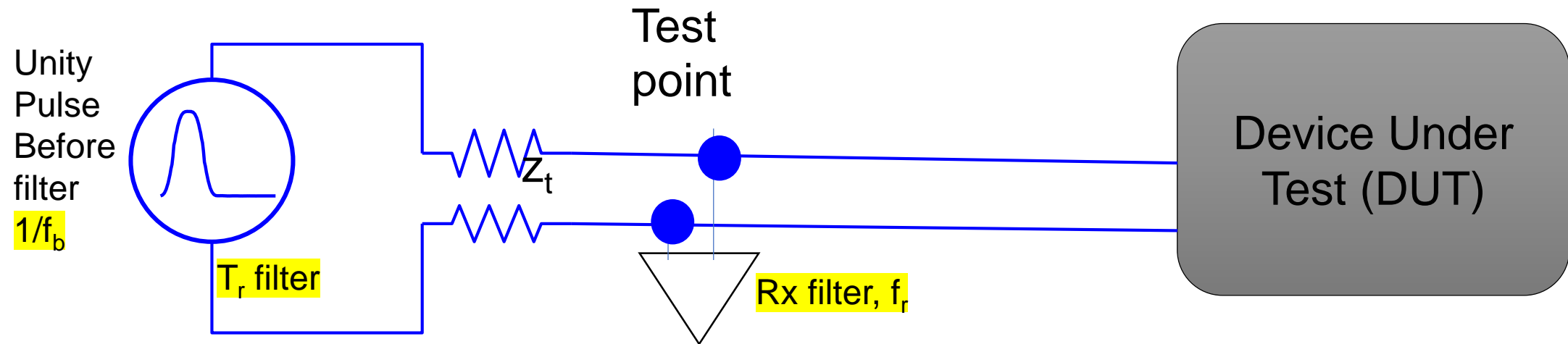
Presenter: Scott McMorrow

ERL Summary

- ERL is single number representing the return loss for
 - A particular data rate, required BER, and signaling (NRZ, PAM4, PAM6 ...)
- ERL is computed from a pulse TDR.
- PTDR sort looks like a derivative of TDR
- ERL is specification for many standard with data rates above 50 Gb/s
- ERL may be used to evaluate BOR and connector designs

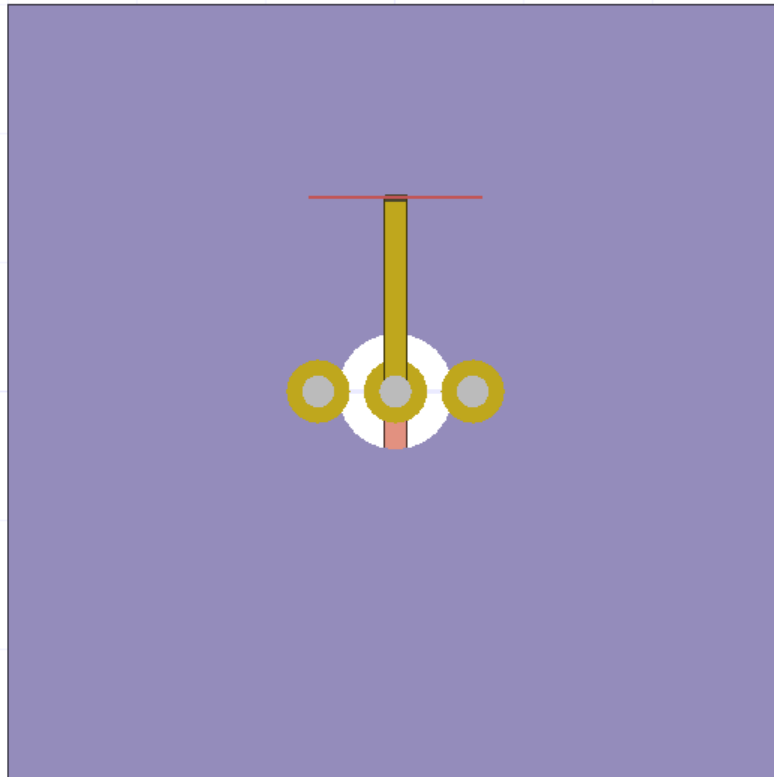
- One number rules them all.

Pulse Response Parameters applied to determine PTDR

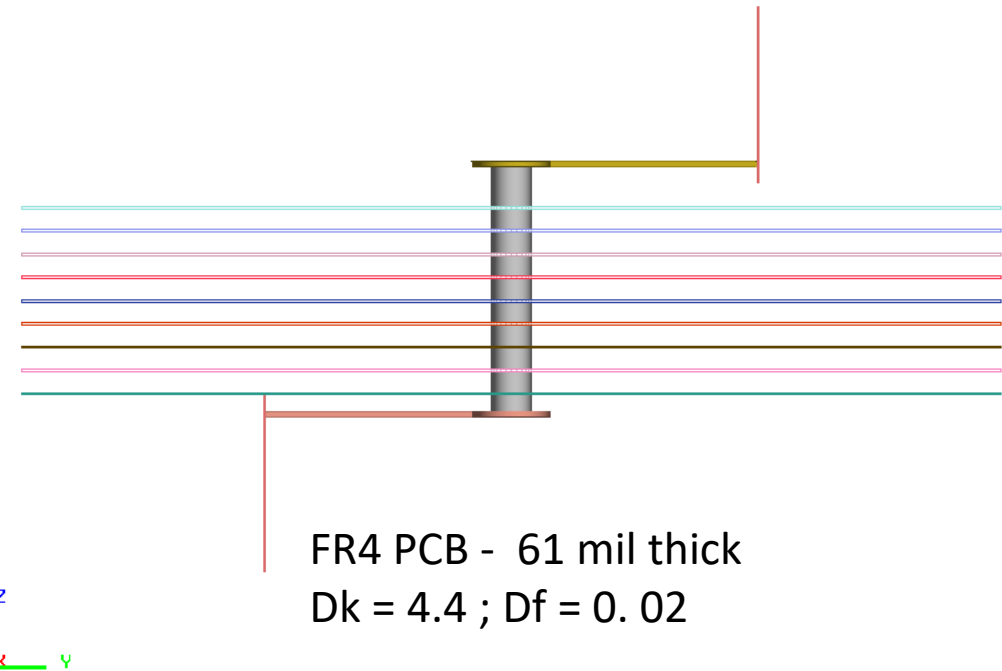


Parameter	Symbol	Units	COM Code Keyword
Signaling rate	f_b	GBd	f_b
Transition time associated with a pulse	T_r	ns	TR_TDR
Receiver 3 dB bandwidth	f_r	GHz	f_r

Simple Single Ended Via Transition Design

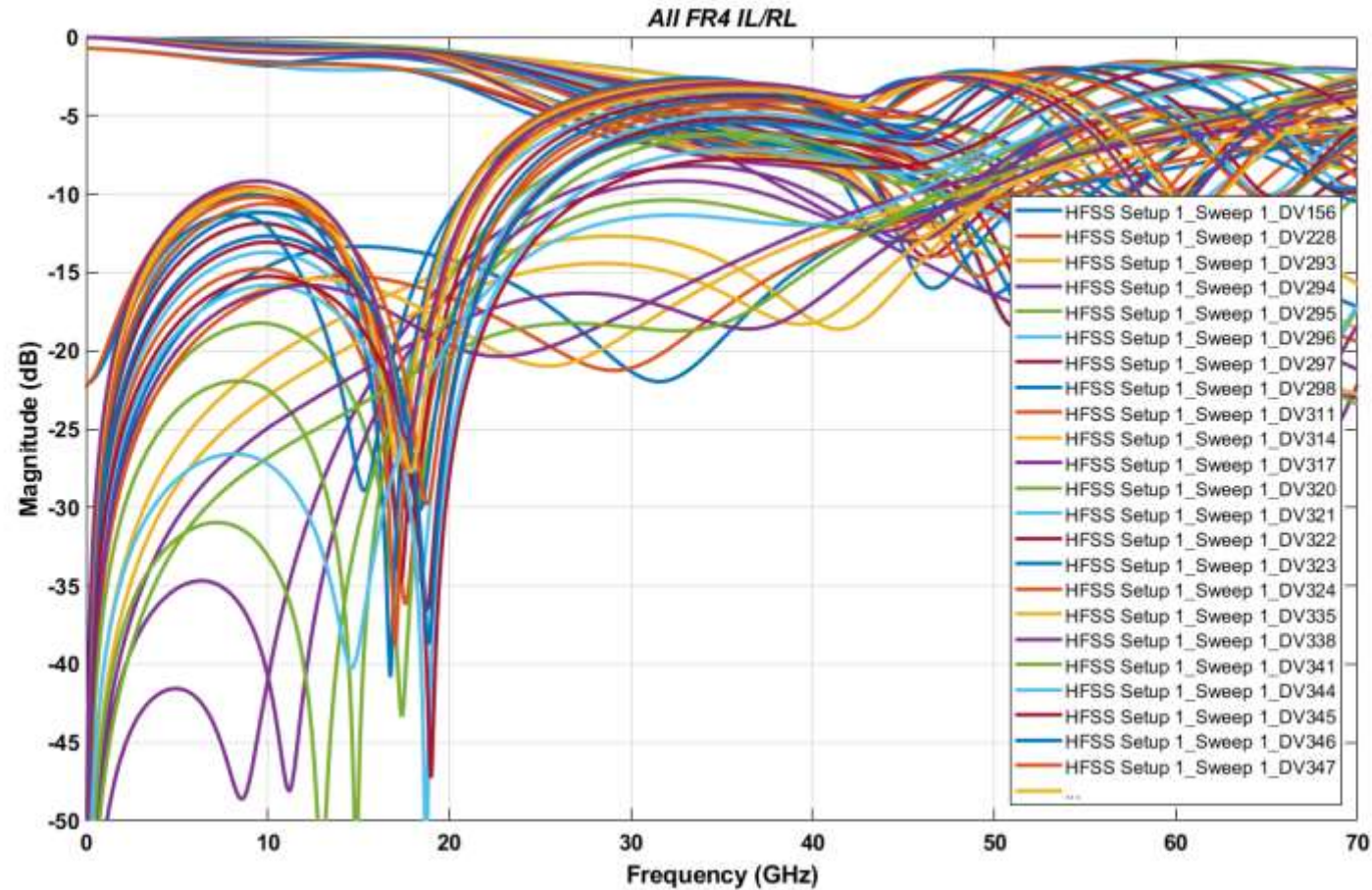


Vary Ground via pitch – 0.6 to 1 mm
Vary Antipad Diameter – 0.7 to 1.5 mm



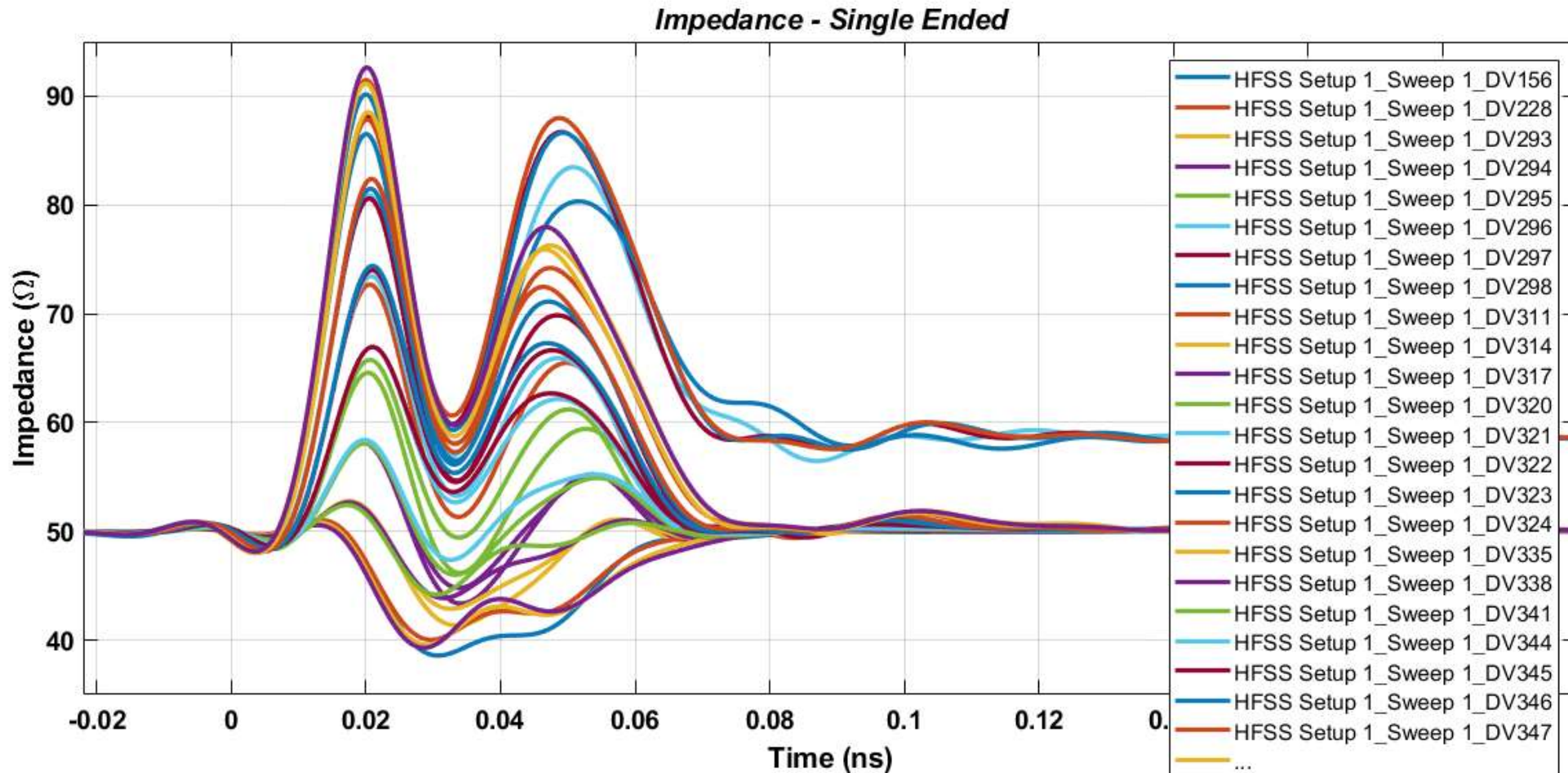
FR4 PCB - 61 mil thick
 $D_k = 4.4$; $D_f = 0.02$

IL/RL For Parametric Sweep



Which of these responses is best?
At what data rate?

TDR for Parametric Sweep



Which of these responses is best?
At what data rate?

ERL Settings for 224G PAM6

Stimulus = scott_ERL_224G	
Butter	0.75
driver	norm
levels	6
N	100
ndfe	0
rho_x	0.3
risetime	5.385e-12
risetime_level	10_90
specBER	0.0001
t_step	2.5e-13
term	
tfx	0
UI	1.1538e-11

← No DFE

← 65 GHz Risetime Bandwidth

← 86.7 Gbaud UI

ERL Settings for 112G PAM4

Stimulus = scott_ERL_112G	
Butter	0.75
driver	norm
levels	4
N	100
ndfe	0
rho_x	0.3
rifetime	8.333e-12
rifetime_level	10_90
specBER	0.0001
t_step	2.5e-13
term	
tfx	0
UI	1.7857e-11

← No DFE

← 42 GHz Risetime Bandwidth

← 56 Gbaud UI

ERL Settings for 56G PAM4

Stimulus = scott_ERL_56G	
Butter	0.75
driver	norm
levels	4
N	100
ndfe	0
rho_x	0.618
rifetime	1.6666e-11
rifetime_level	10_90
specBER	0.0001
t_step	2.5e-13
term	
tfx	0
UI	3.5714e-11

← No DFE

← 21 GHz Risetime Bandwidth

← 28 Gbaud UI

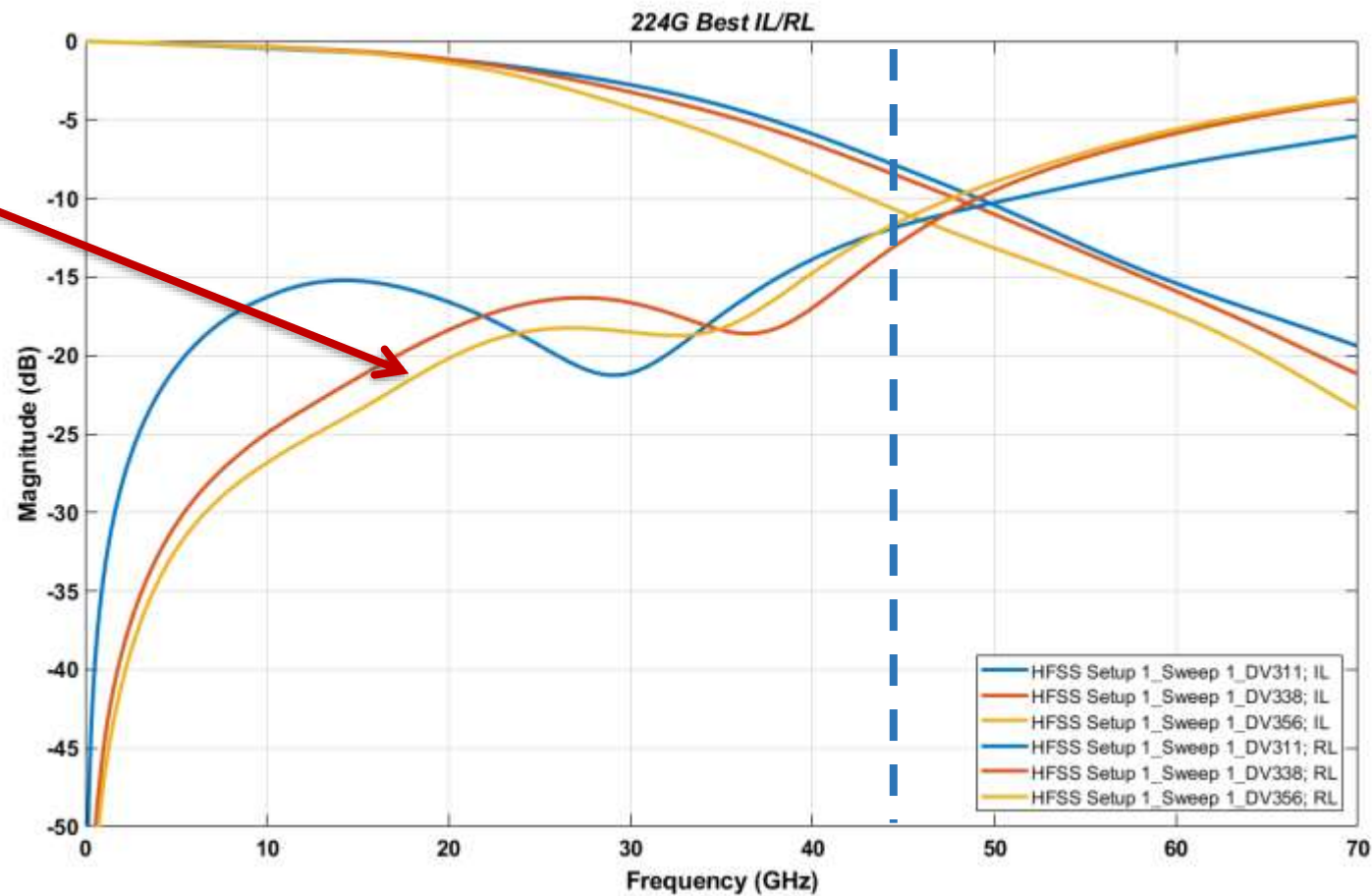
ERL for 56G PAM4, 112G PAM4, 224G PAM6

Case	ERL (dB) 224G PAM6	ERL (dB) 112G PAM4	ERL (dB) 56G PAM4	\$antipadDiameter	\$gndPitch
HFSS Setup 1_Sweep 1_DV356	10.48657623	17.64794617	23.75510606	1.9mm	0.9mm
HFSS Setup 1_Sweep 1_DV311	10.345386	12.95634964	14.66596066	1.9mm	0.7mm
HFSS Setup 1_Sweep 1_DV338	10.03654679	16.18216566	21.81958292	1.1mm	0.9mm
HFSS Setup 1_Sweep 1_DV335	9.754318734	12.58603815	14.74149061	0.9mm	0.9mm
HFSS Setup 1_Sweep 1_DV156	9.548507346	11.62403419	12.83749429	0.7mm	0.7mm
HFSS Setup 1_Sweep 1_DV314	9.18840567	13.92744047	19.80248733	1.7mm	0.7mm
HFSS Setup 1_Sweep 1_DV355	8.787527509	12.35245393	15.03072565	1.3mm	0.9mm
HFSS Setup 1_Sweep 1_DV293	8.022002259	12.21667831	17.66784512	0.9mm	0.7mm
HFSS Setup 1_Sweep 1_DV357	6.079865696	11.38560224	24.05464918	2mm	0.9mm
HFSS Setup 1_Sweep 1_DV341	5.738593483	10.50111329	25.53088656	2mm	0.8mm
HFSS Setup 1_Sweep 1_DV317	5.151782388	9.426807095	25.76385542	1.1mm	0.8mm
HFSS Setup 1_Sweep 1_DV294	4.557968614	8.671250156	26.14306161	0.9mm	0.8mm

Best Cases

224G PAM6 Best Designs

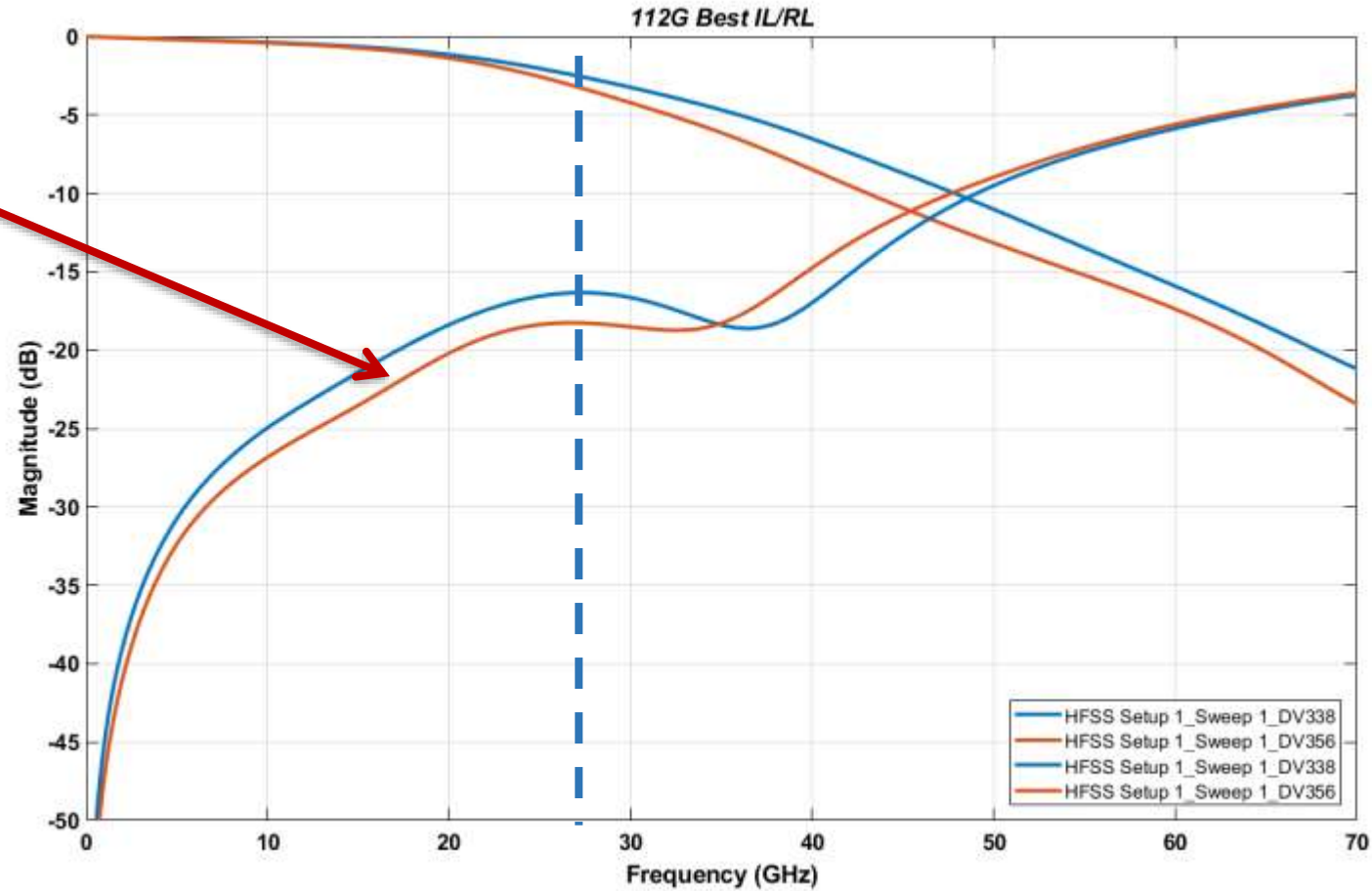
Best 224G ERL



43.33 GHz Nyquist

112G PAM4 Best Designs

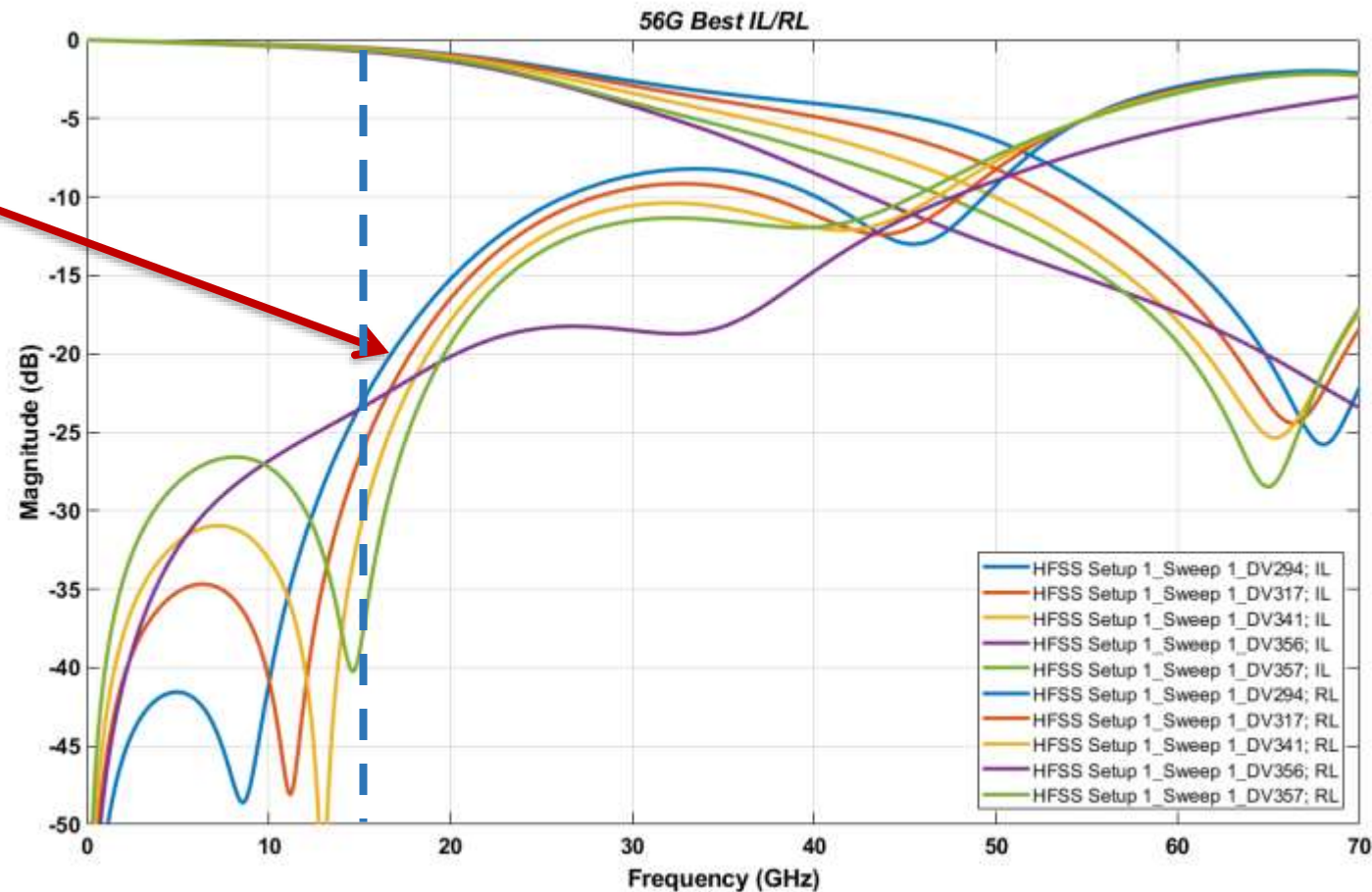
Best 112G ERL



28 GHz Nyquist

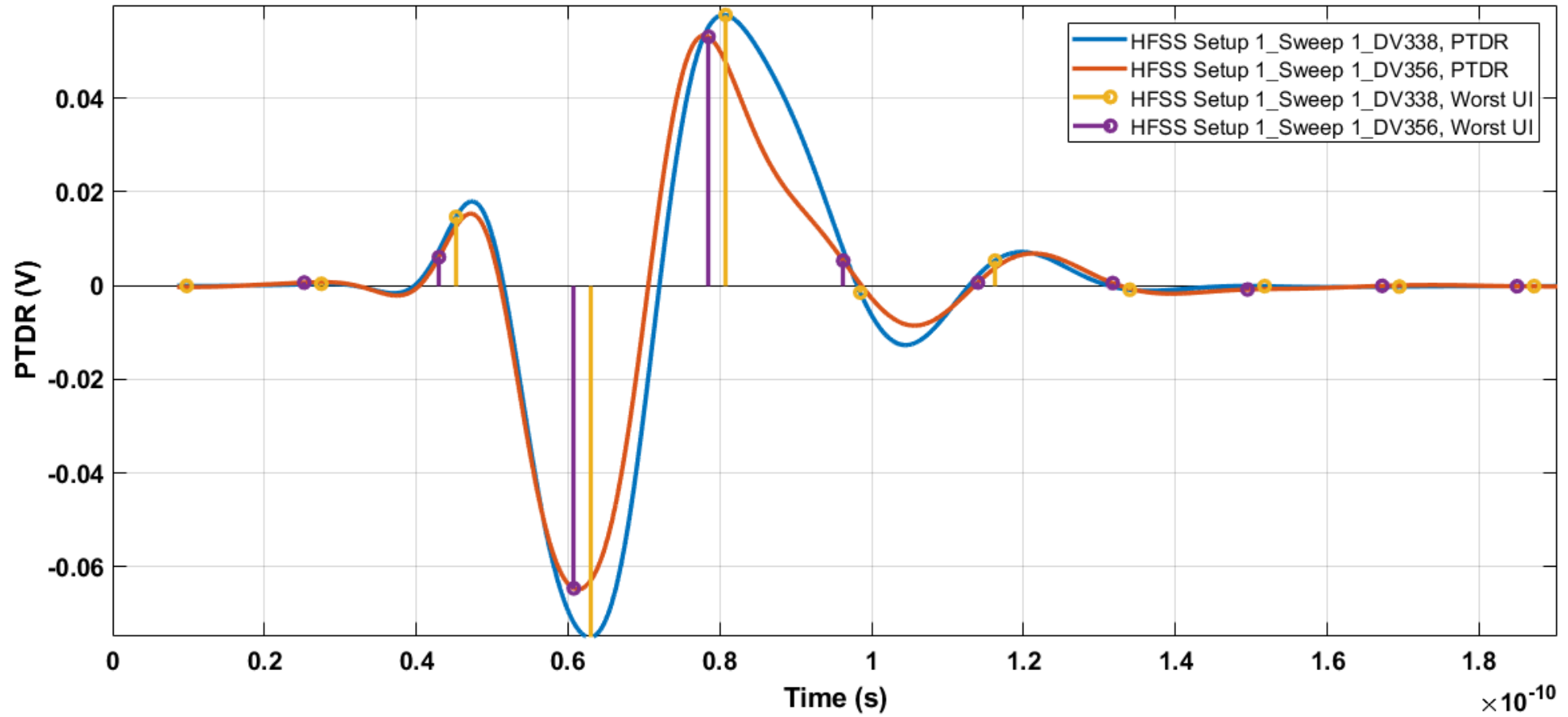
56G PAM4 Best Designs

Best 56G ERL

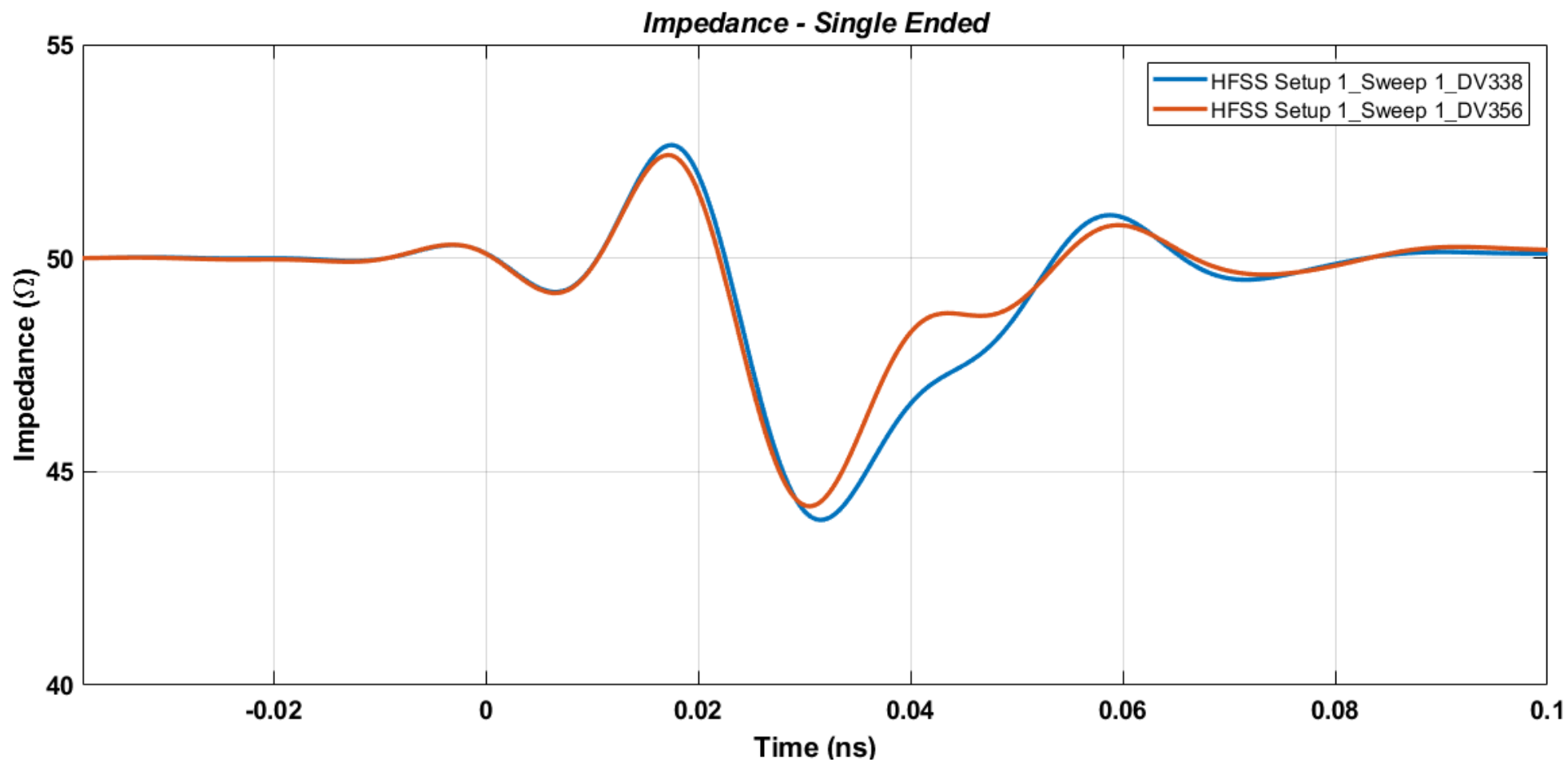


14 GHz Nyquist

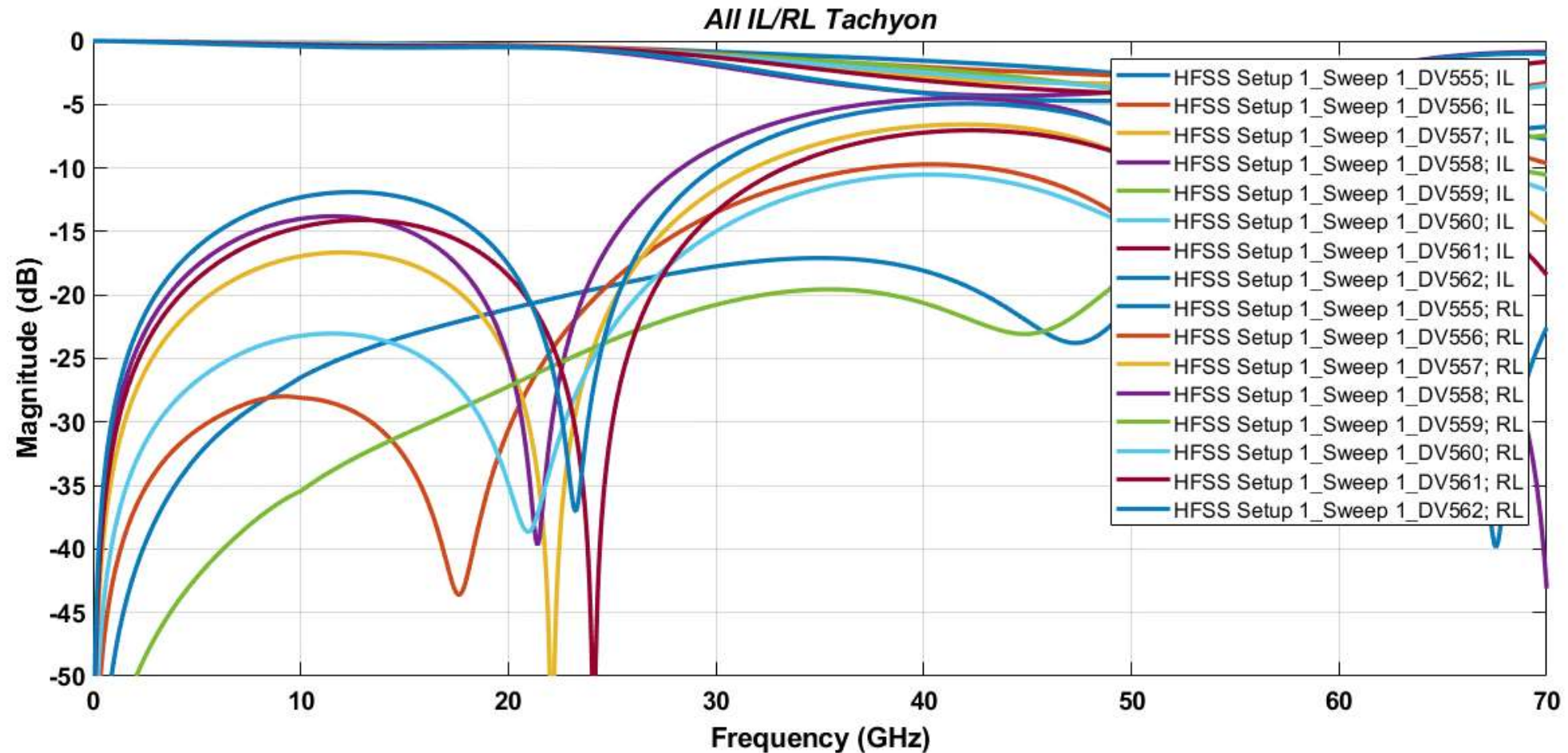
112G ERL PTDR



112G TDR

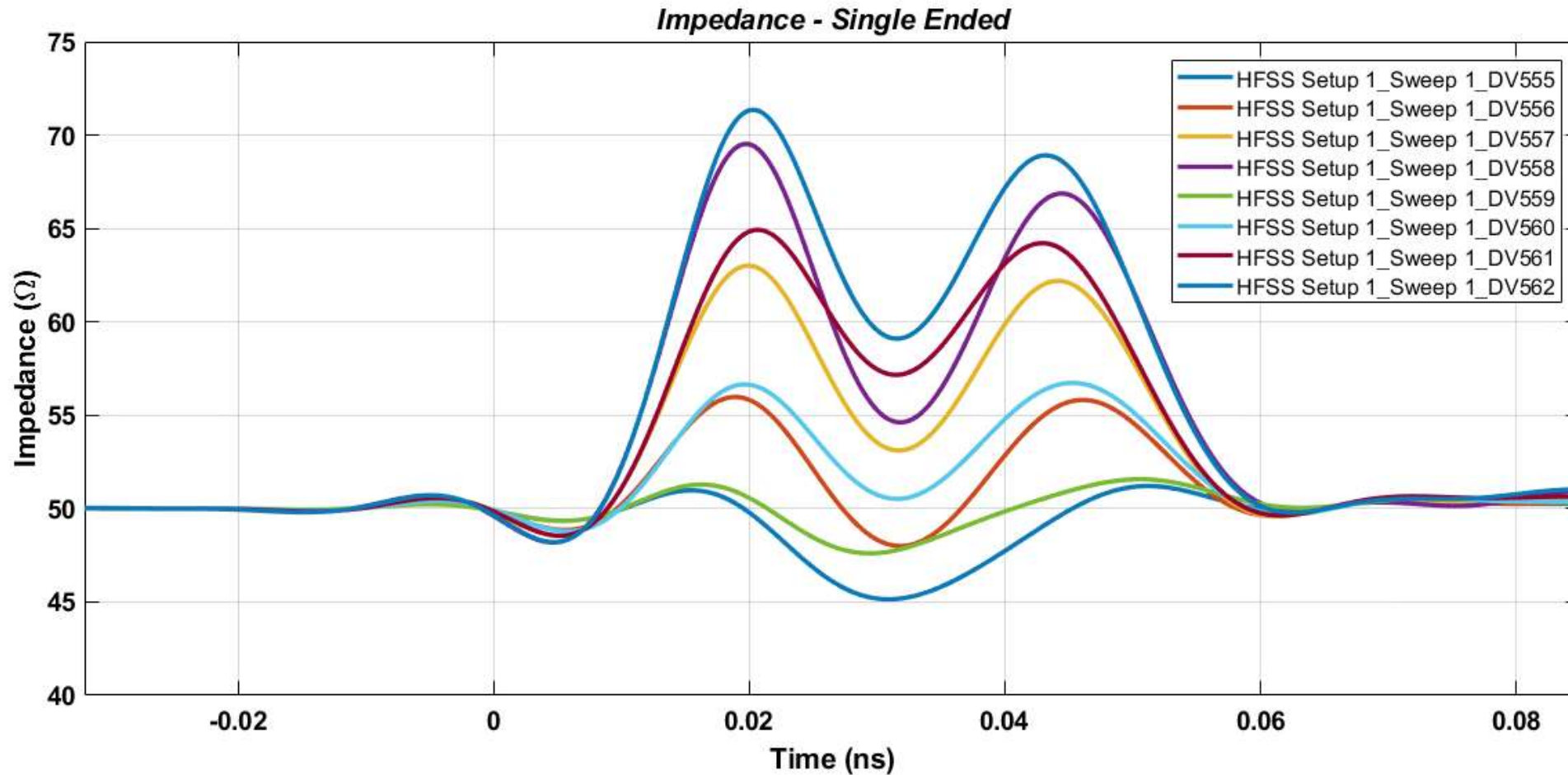


IL/RL For Parametric Sweep with Tachyon



Which of these responses is best?
At what data rate?

TDR for Parametric Sweep with Tachyon



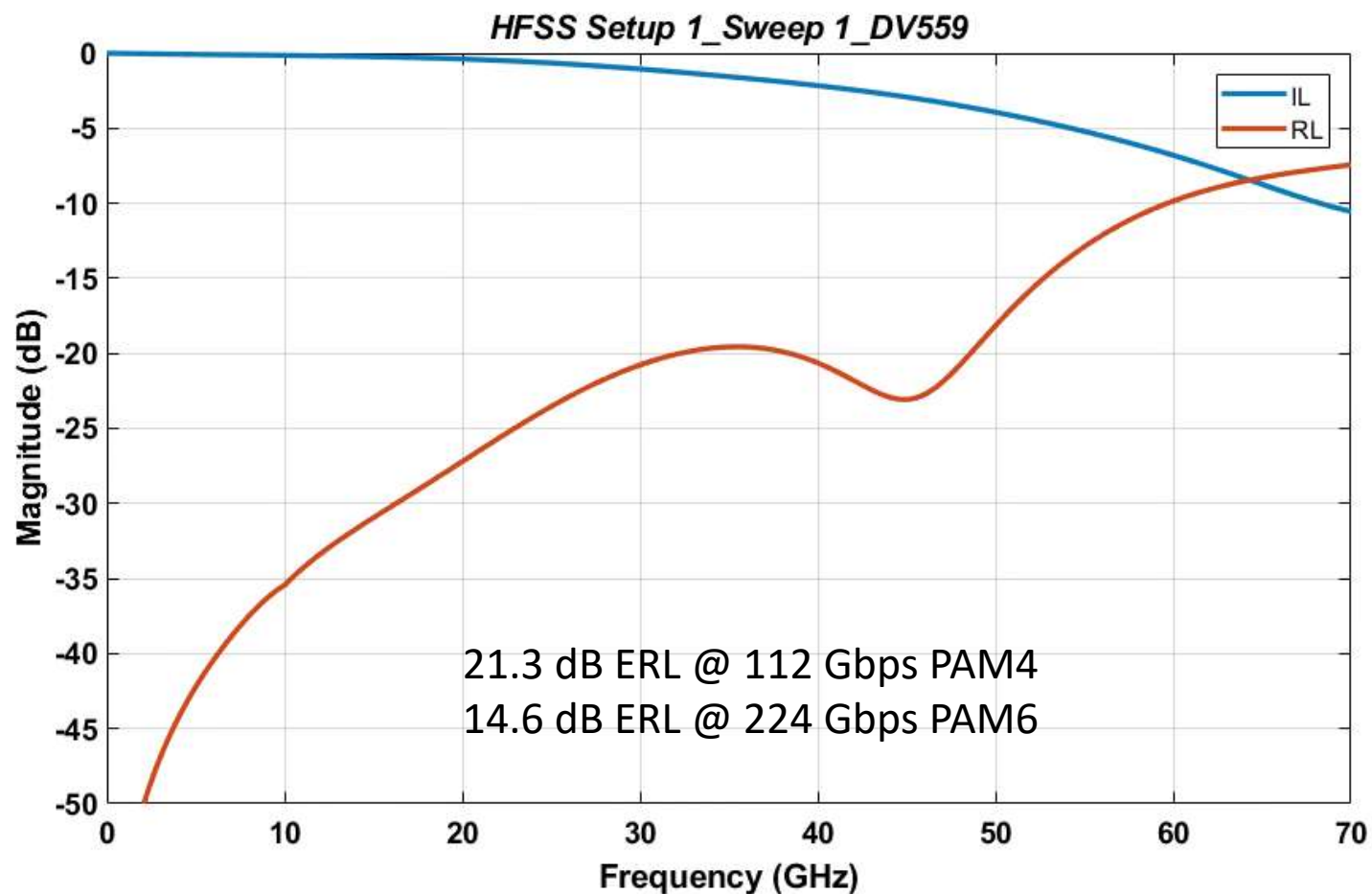
Which of these responses is best?
At what data rate?

112G ERL with Tachyon

ERL - Single Ended	
	ERL (dB)
HFSS Setup 1_Sweep 1_DV555	17.8152
HFSS Setup 1_Sweep 1_DV556	14.7652
HFSS Setup 1_Sweep 1_DV557	13.2828
HFSS Setup 1_Sweep 1_DV558	9.85098
HFSS Setup 1_Sweep 1_DV559	21.3201
HFSS Setup 1_Sweep 1_DV560	17.291
HFSS Setup 1_Sweep 1_DV561	11.6307
HFSS Setup 1_Sweep 1_DV562	9.53288

Best Case

112G Tachyon Best Case IL/RL



Conclusion

- ERL methodology provides one number that can be used to evaluate devices
 - Connectors
 - BORs
 - Packages
 - Etc
- Because it is one number, ERL can be used to quickly evaluate various design iterations.
- ERL is extremely valuable in the optimizing BOR and Connector designs.



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