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Effective Return Loss (ERL): What is ERL and How is it Computed? | Presenter: Richard Mellitz

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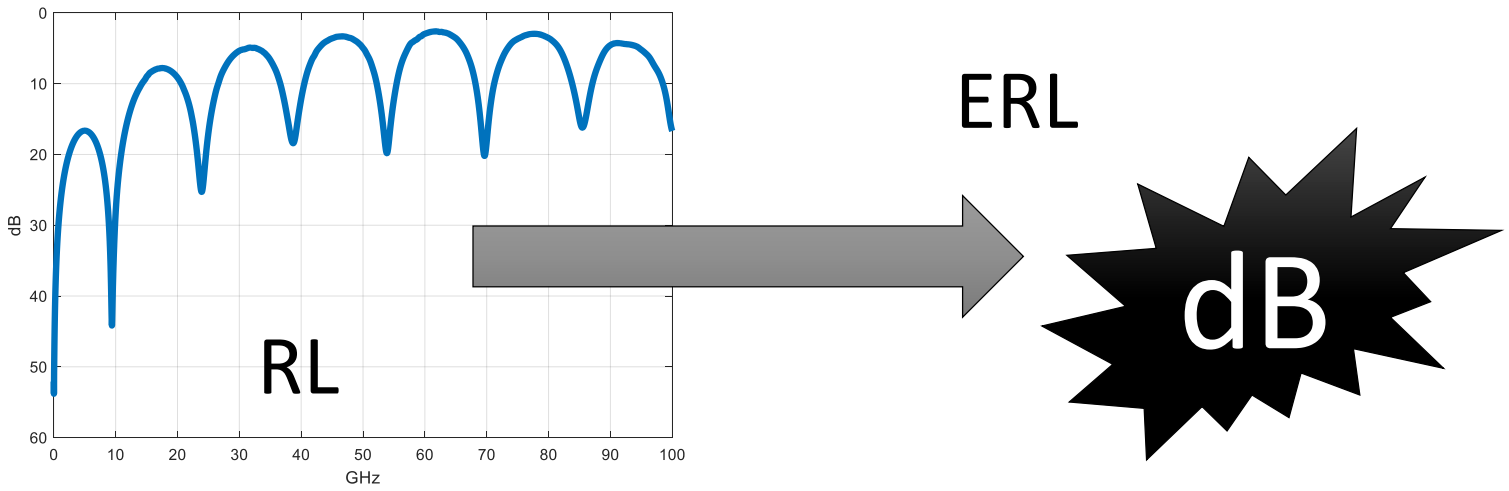
EFFECTIVE RETURN LOSS (ERL)

- ERL is a figure of merit representing measured return loss (RL)
  - ERL is a scalar
  - ERL is the amount of digital signal returned which is statistically reduced to an effective value at the test point.
  - ERL may address both compensable and un-compensable ISI.
- Return loss (RL) is the self-port s-parameter (s_{ii}) versus frequency represented as loss.
  - RL is vector



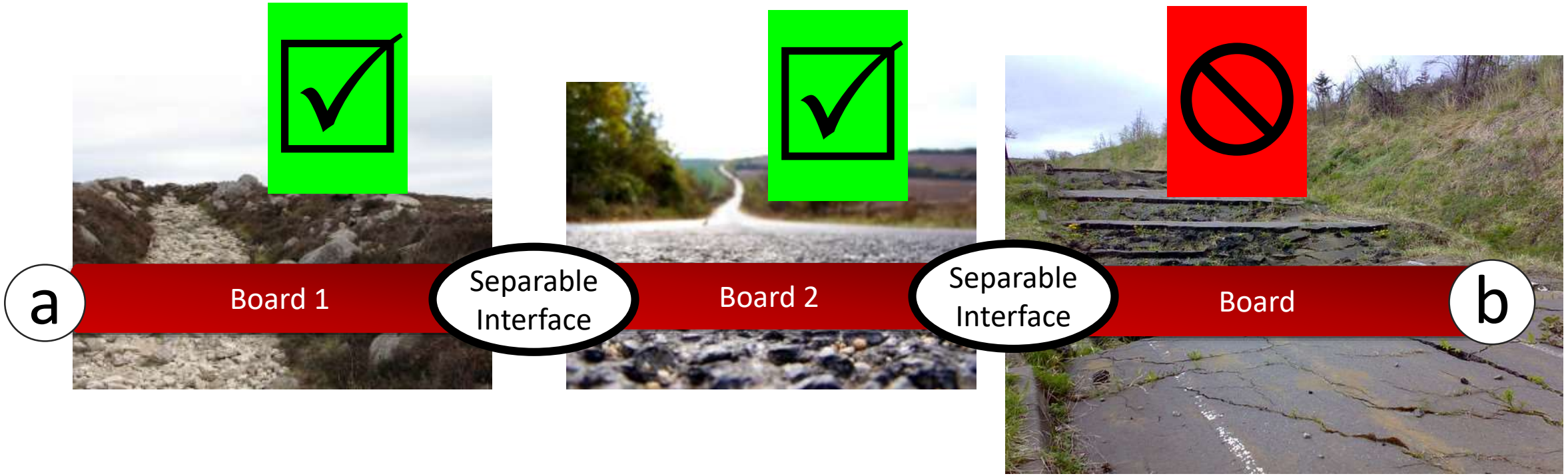
RL AND ERL PROPERTIES FOR DIGITAL SIGNALING

- Return loss is a measurement of reflections
- Bumps on road can be a simple analogy for reflections on a transmission path

SOME REFLECTIONS ARE ALREADY INCLUDED

- Use 3 Boards with separable interfaces as an example
- Reflections are included for transmission performance between “a” and “b”
- Next look at Board 3 as an interchangeable part

HOW MUCH MORE REFLECTION IS TOLERABLE?



- **Question:** How much more reflection can Board 3 have and still have acceptable signal transmission between “a” and “b”?
- The challenge is to quantify the reflection in a meaningful way

REMINDER

- ERL and RL are only a small part of the story

- A Hummer is different from a Ferrari
- Context matters
- How the interface behaves to a data stream is context for ERL
- However, reducing reflections is most always desirable

HISTORICALLY, RL vs. FREQUENCY WAS THE METRIC

- Limit lines RL vs frequency were used to indicate pass fail
  - Called masks
- Setting these limit lines can be a challenge
  - There does not appear to be a clear way to relate limits lines to successful signal transmission.
  - Except we know that if there are no reflection, that is good.
- An example is used to illustrate

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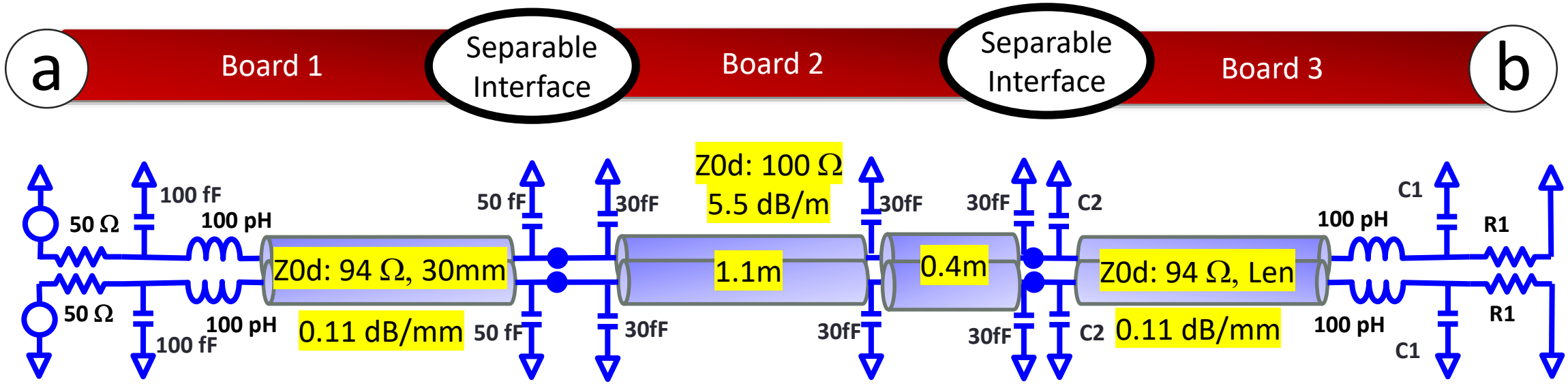
THE SIMPLIFIED CHANNEL USED IN THE EXPERIMENT HAS ABOUT 12. 5 DB LOSS AT 26.6



- 3 separable Boards (1, 2, 3)
- Board 1 and Board 3 are respectively a transmitter (Tx) board and receiver (Rx) board with circuitry
- Board 2 is similar to low loss cabling
- This channel is somewhat reflection dominated
  - It will serve to illustrate the impact of reflection metrics

CONSIDER 100 GBPS (53.126 GBAUD) PAM-4 SIGNALING

Evaluation includes three PCB variations for Board 3

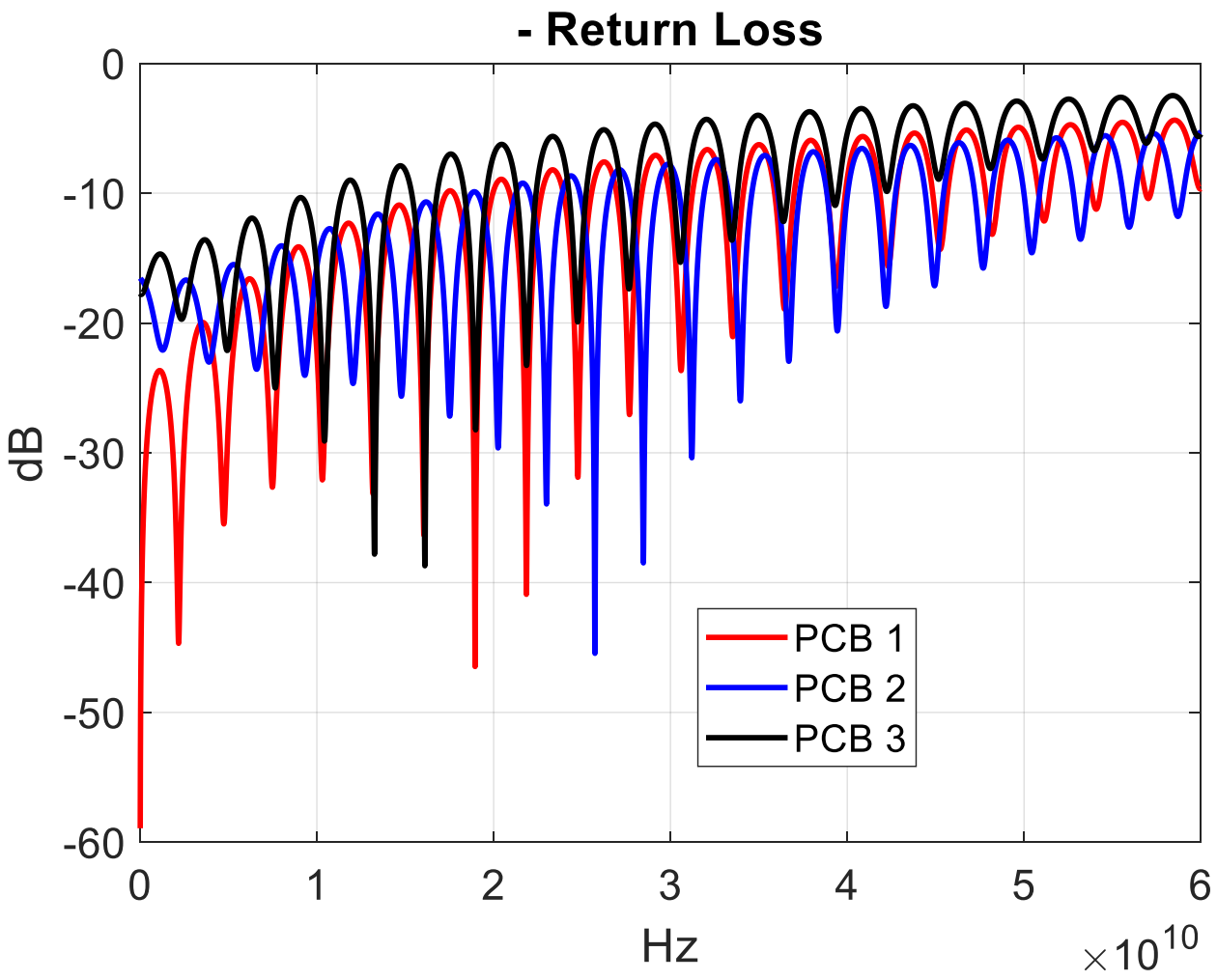
PCB 1, PCB 2, & PCB 3

The end-to-end insertion loss for all 3 PCB variations for Board 3 are about the same

~ 12.5 dB total loss at 26.6 GHz

- No Jitter or noise
- The transmitter has 1 precursor FFE tap
  - 0 to -0.1, 0.02 steps
  - Tx edge rate at source 6 ps
- The receiver has a CTLE
  - 0 dB to -15 dB, 1 dB steps

WHICH HAS BETTER PERFORMANCE?



- Channel operating margin (COM) and minimum detector error ratio (DER) used to compare the three designs

CHANNEL OPERATING MARGIN (COM) WAS USED TO COMPARE THE THREE DESIGNS

	PCB 1	PCB 2	PCB 3
C1	110 fF	130 fF	120 fF
C2	60 fF	50 fF	95 fF
R1	50 Ω	37 Ω	65 Ω
Len	28 mm	30 mm	28 mm

COM
4.4 dB
DER= 2e-6

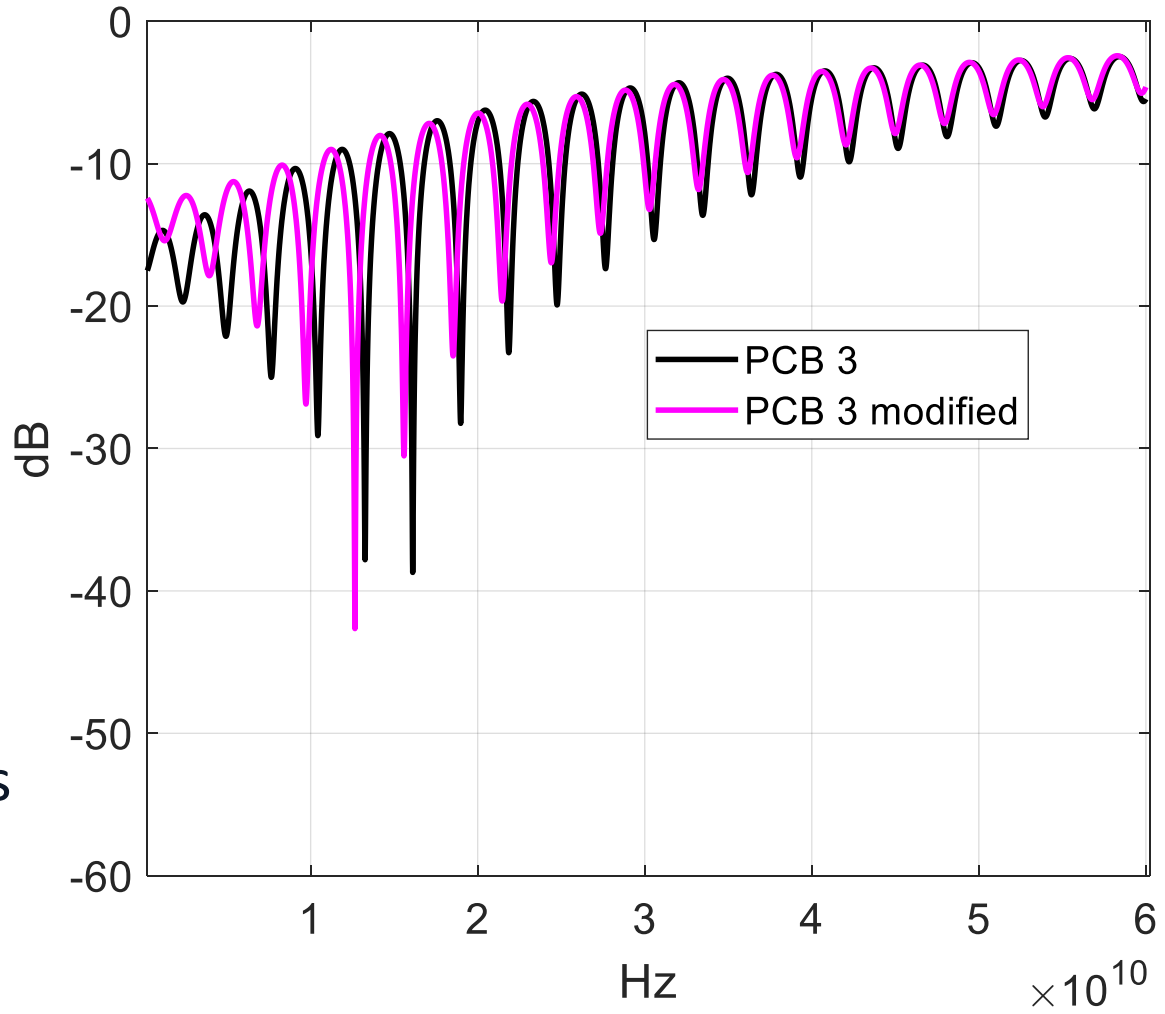
COM
4.43 dB
DER= 2.1e-6

COM
2.3 dB
DER= 3.8e-4

No Big Surprise

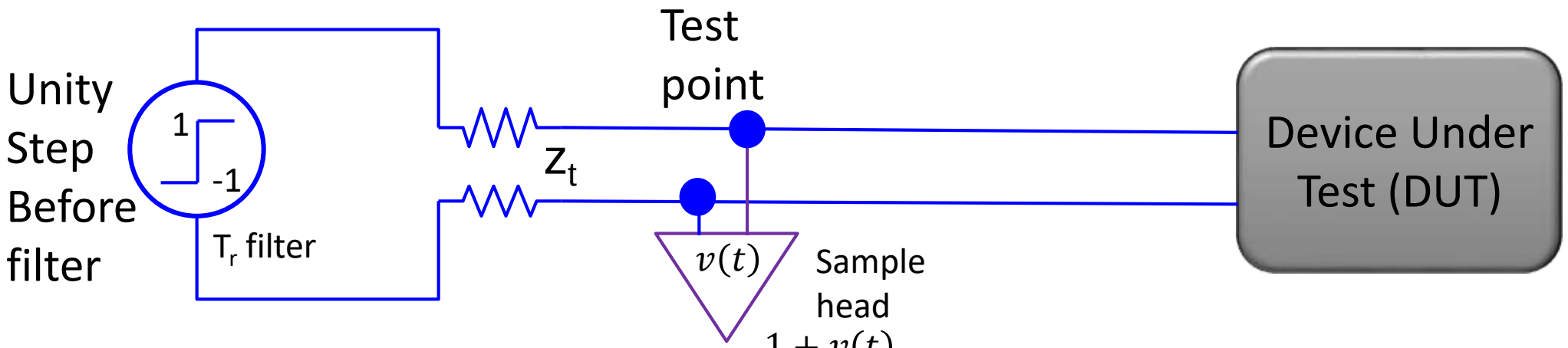
JUST WHEN YOU THINK YOU HAVE IT FIGURED OUT…

- Modify PCB 3 a little
  - Change C1 from 130 fF to 140 fF
  - Change C2 for 95 fF to 100 fF
  - Change R1 from 65 Ω to 35 Ω
- PCB 3 Performance improves
- Old PCB 3 COM was 2.3 dB
- Modified PCB 3 COM is 3.3 dB
- More on latter ERL later, but ERL improves
  - Old PCB 3ERL was 5.6 dB
  - New PCB 3 ERL is 6.6 dB
- It's harder to gain insight from these RL plots
- TDR may hint how to account for reflections



REVIEW OF TIME DOMAIN REFLECTOMETRY (TDR)

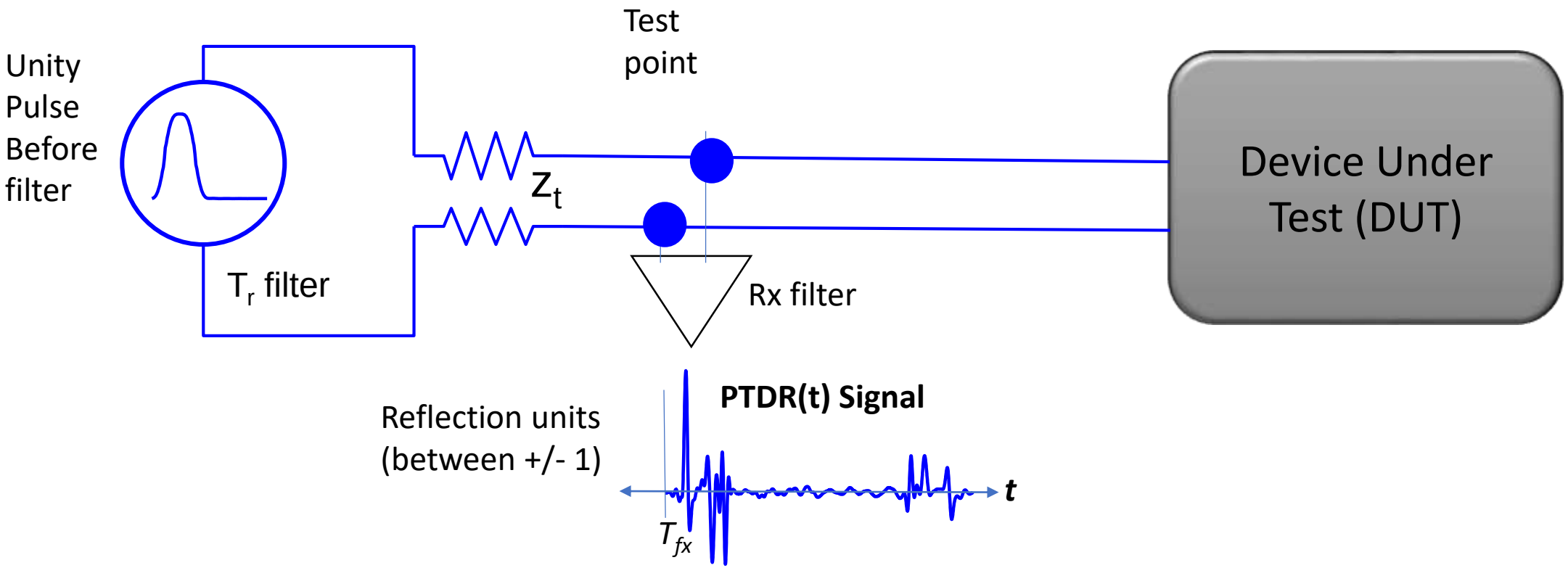
- TDR is time domain reflectometry, using a step as a source
- The voltage measured at the sample head, v(t), is converted to a waveform of impedance verse time
- We normally look for impedance discontinuities
- Why not quantify the discontinuities as a data signal would encounter
  - That is basis of using pulse instead of a step



$$Z(t) = 2Z_t \frac{1 + v(t)}{1 - v(t)}$$

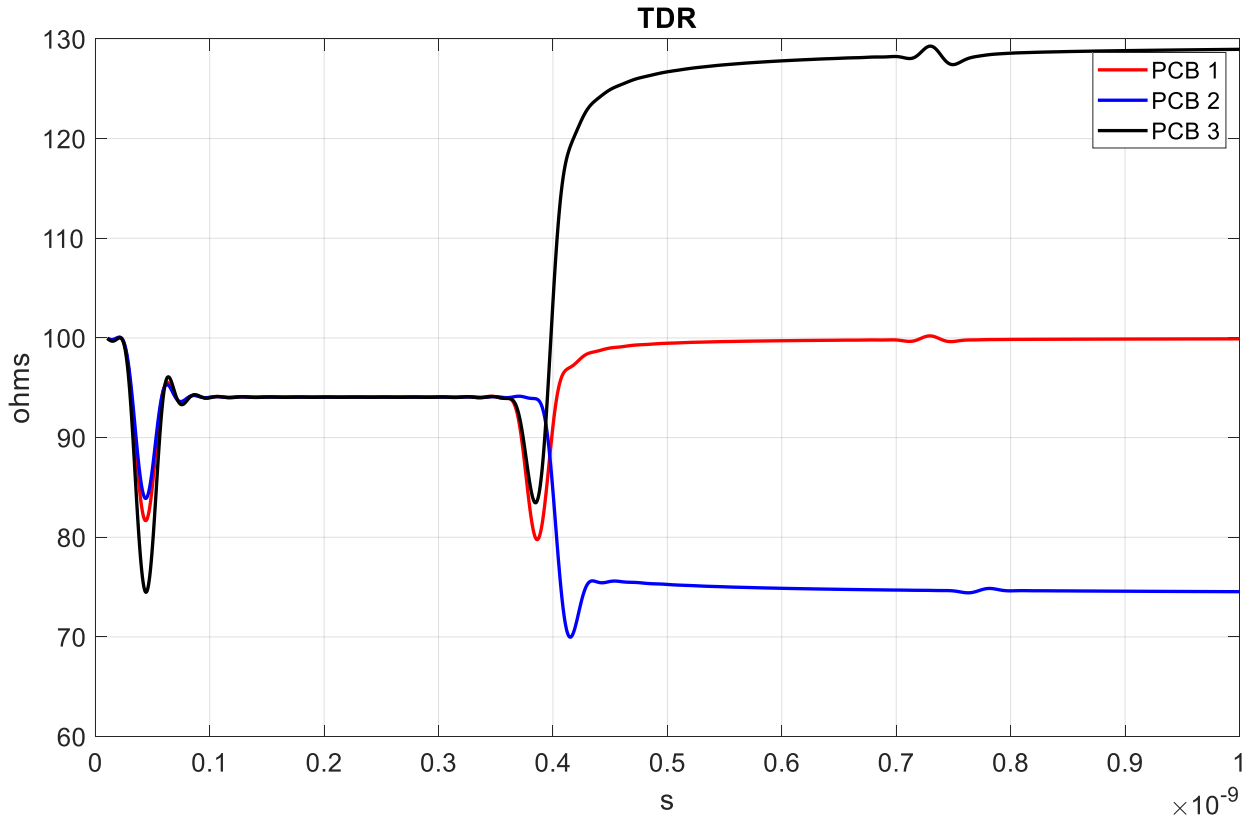
INTRODUCTION TO PULSE TIME DOMAIN REFLECTOMETRY (PTDR)

- PTDR is time domain reflectometry using a pulse as a source
- PTDR units are the amount of reflection at a point in time
- The PTDR waveform is observed at the test point after a filter



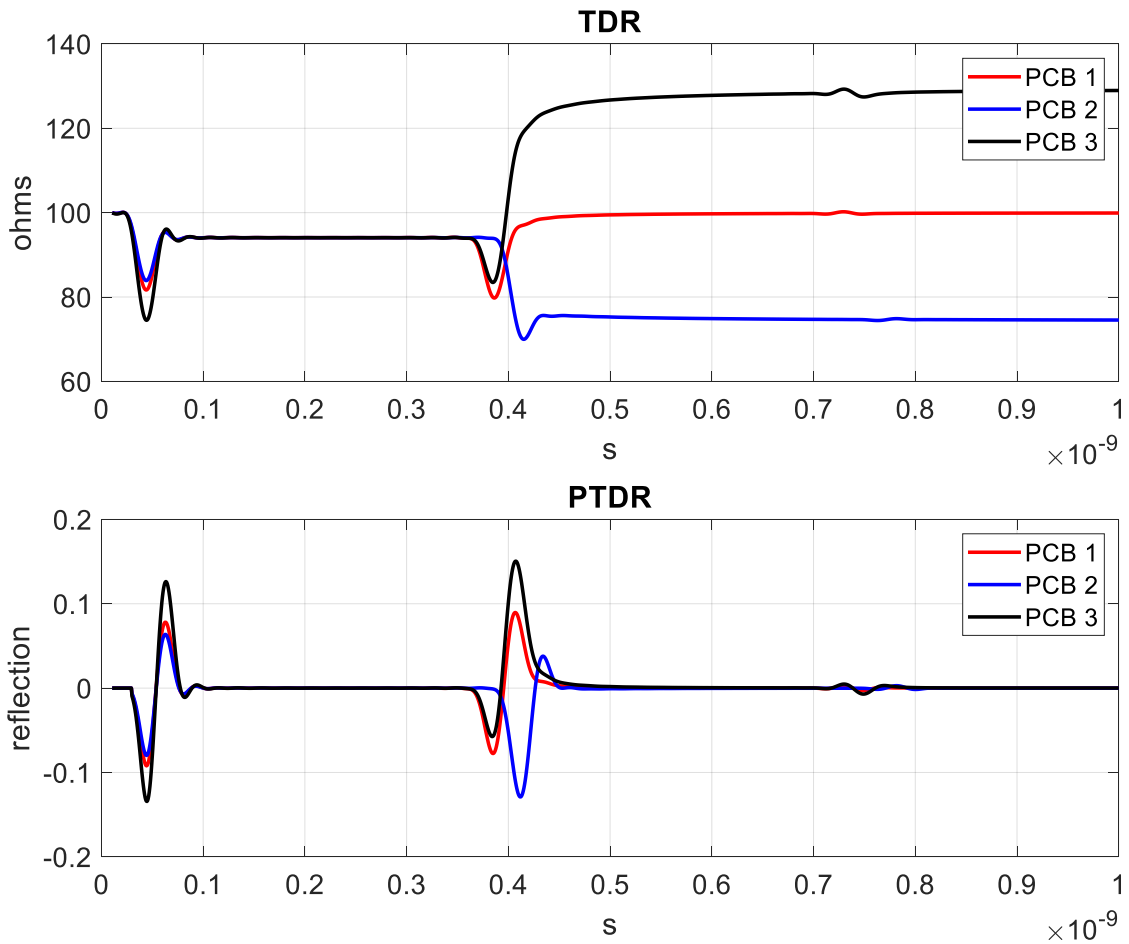
FIRST LOOK: TIME DOMAIN REFLECTOMETRY (TDR)

- Traditionally, TDR has been used to diagnose discontinuities
- We could rationalize that PCB 3 is worse
- How can we turn this inspection of TDR into a meaningful number?
- Let's start with the context
- In prior presentations we showed how for a given data rate the received signal can be decomposed into a collections of pulses



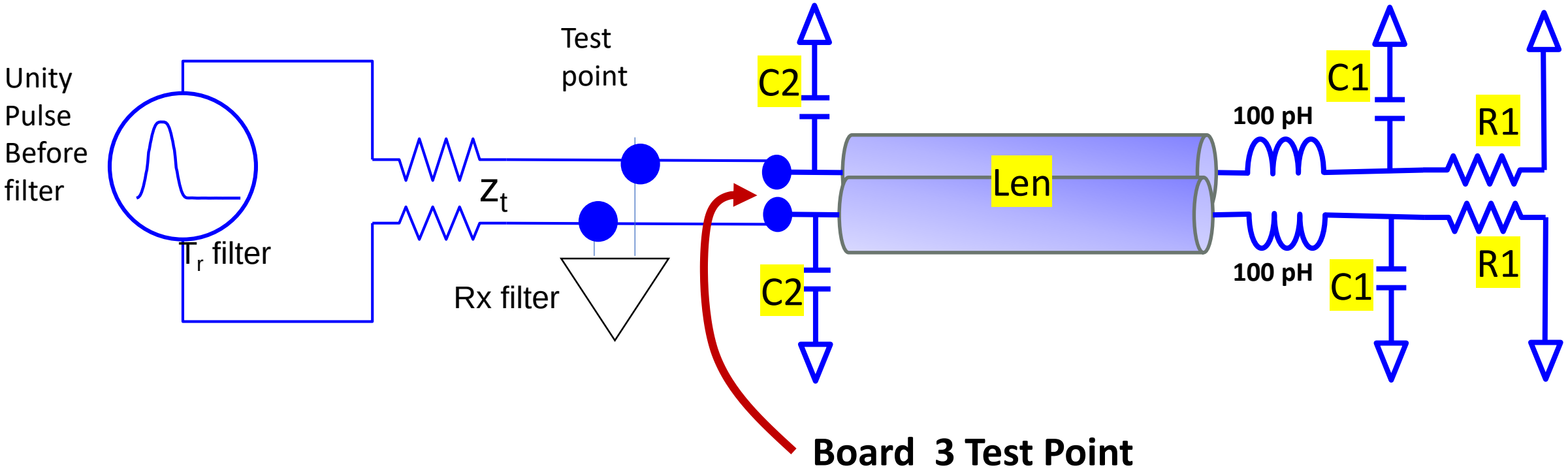
PULSE TIME DOMAIN REFLECTOMETRY (PTDR)

- For TDR we convert reflected voltage to impedance
- For PTDR we report the amount of pulse that is reflected
- PTDR provides more insight into the amount of signal reflected at each point in time
- PTDR captures changes in impedance
  - Sort of like a derivative
- One thing to note is not all of the reflected signal makes it back to the receiver.
  - It needs to be re-reflected by the other board
  - So the board reflections at each interface are tied together



SET UP FOR MEASURING PTDR IN THE EXAMPLE

PDTR is used to determine a single value, ERL representing reflections looking into the Board 3 test point



PTDR IS OBTAINED FROM A MEASURED RL S-PARAMETER … DETAILS …

PTDR may be computed using an iFFT of the filtered return loss

$$PTDR(t) = \int_{-\infty}^{\infty} X(f) H_t(f) S_{ii}(f) Hr(f) e^{j2\pi f t} dt$$

- $H_t(f)$ is the edge rate filter
- $H_r(f)$ is a receiver filter
- $S_{ii}(f)$ is the measured return loss
- X(f) is a function representing a pulse

ADDING UP ALL THE REFLECTION IN PTDR?

That seems pessimistic

Look at context again

- Pulses only occur, depending on data, at well-defined intervals which is the inverse of the baud rate ($1/f_b$)
  - Commonly called the unit interval (UI)
- This results in a set of reflection corresponding to samples in the PTDR
  - At UI sample intervals.

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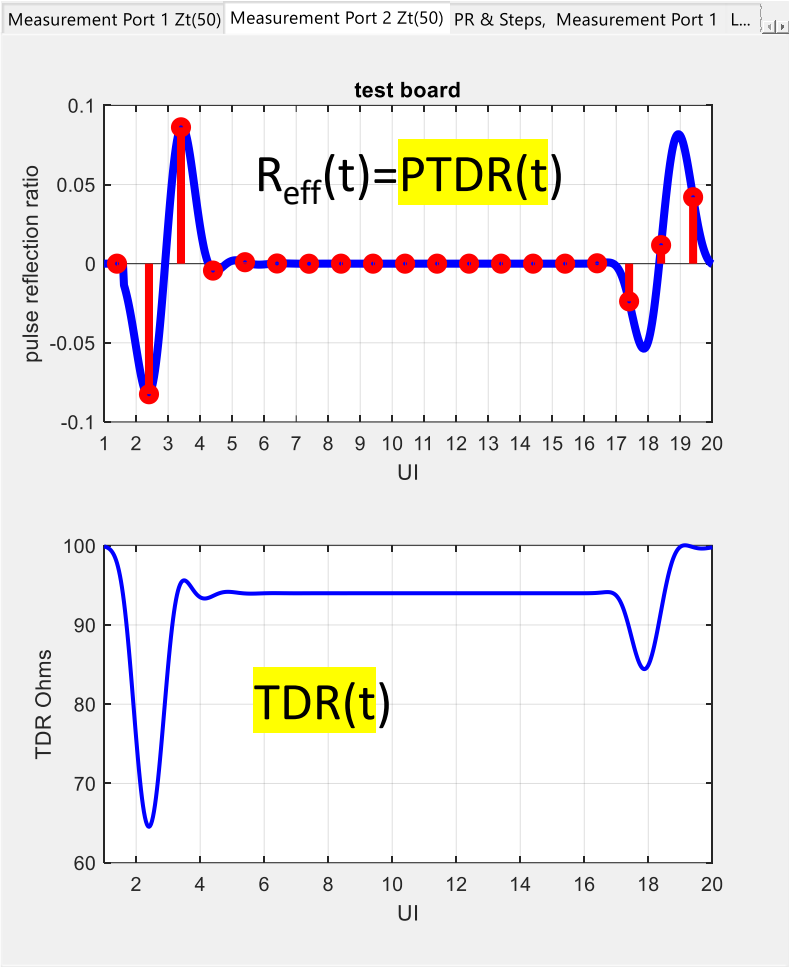
COMPUTING ERL FROM PTDR

- ERL is a statistical compilation of
  - The red dots at the right
  - They are a selection of “n” reflections sampled 1 UI apart
- ERL really uses $R_{eff}(t)$

$$R_{eff}(t) = G_{loss}(t)\, G_{rr}(t)\, PTDR(t)$$

  - For this example $G_{loss}(t) = G_{rr}(t) = 1$
  - We will do more with this later when we talk about gating

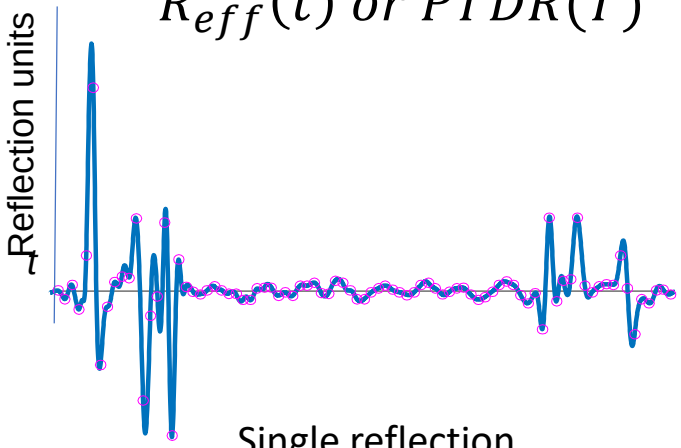


A STATISTICAL COMPILATION OF REFLECTIONS IS USED TO DETERMINE ERL

For the assumption of random data based on coded [1]symbols:

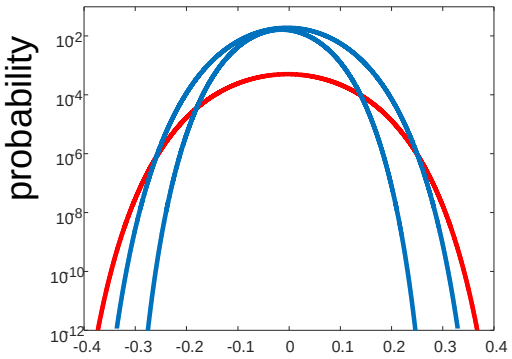
- The goal is to determine the reflection sample set with the largest variance distribution
- Using that sample set we determine the cumulative reflection value with a probability associated with the specified BER

$R_{eff}(t)$ or $PTDR(T)$



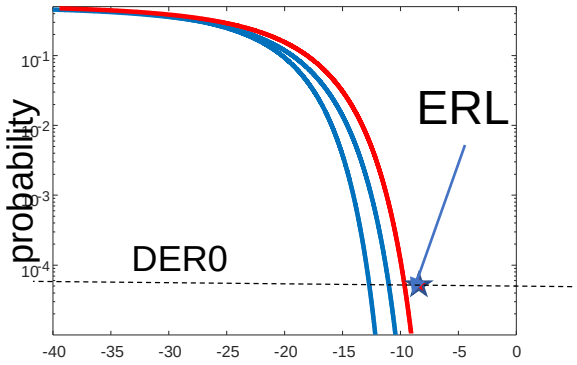
Single reflection symbol/ bit

Convolve with random data to create a PDF for each n sample set



Reflection units

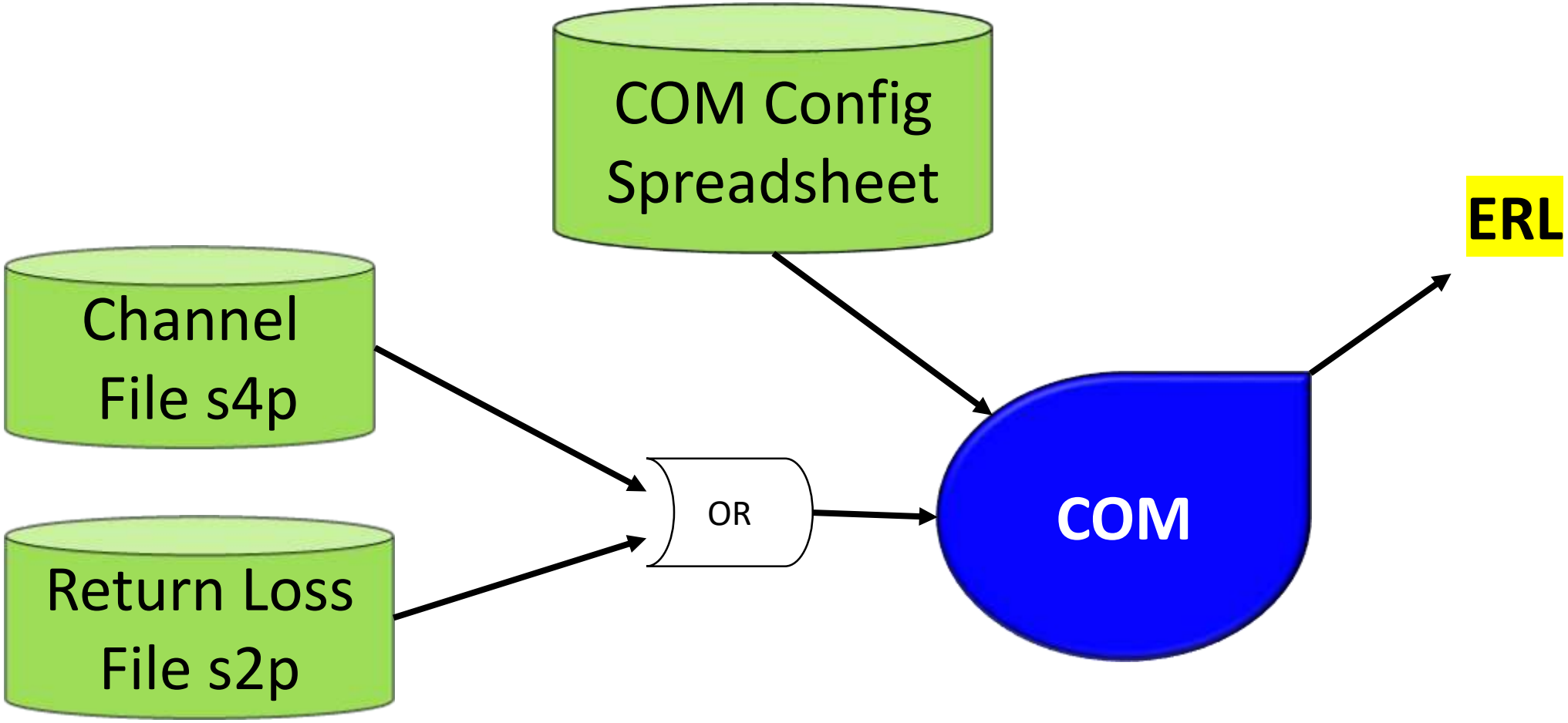
CDF for each sample "n" sample set



dB of reflection

[1]*Symbols for PAM-4 = [-1 -1/3 1/3 1]*

COM MATLAB® CODE MAY BE USED TO COMMUTE ERL

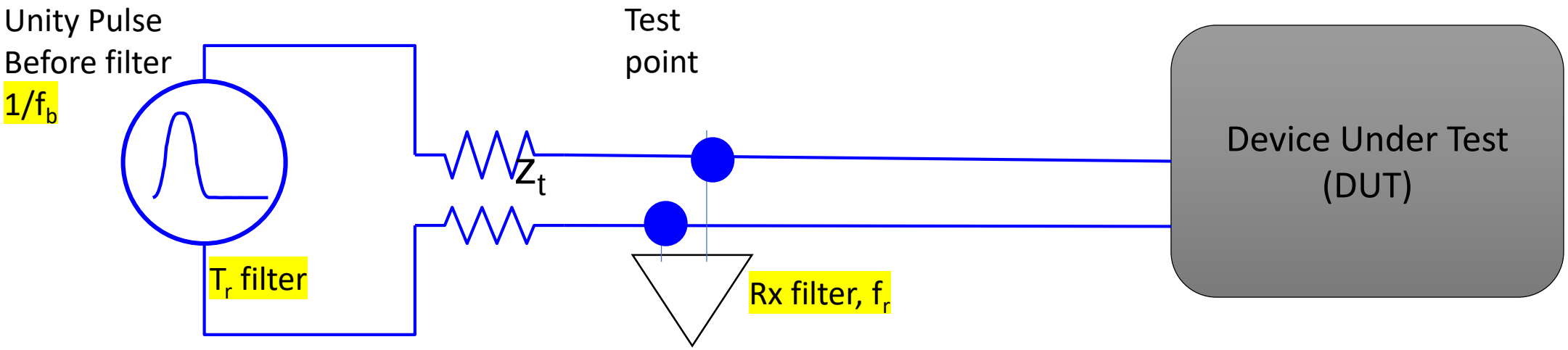


★PARAMETERS USE TO COMPUTE ERL (More Details Later On)

Parameter	Symbol	Units	Default	COM Code Keyword
Signaling rate	f_b	GBd	-	f_b
20%/80% Gaussian transition time associated with a pulse	T_r	ns	0.01 ns	TR_TDR
Receiver bandwidth for 4th order Butterworth Filter	f_r	f_b	0.75	f_r
Number of signal levels	L	—	-	L
Length of the reflection signal	N	UI	-	N
Number of samples per unit interval	M	—	32	M
Equalizer length associated with reflection signal	N_{bx}	UI	-	N_bx
Incremental available signal loss factor	β_x	GHz	0	beta_x
Permitted reflection for an external connection at the test point	ρ_x	—	0.618	rho_x
Target detector error ratio	DER_0	—	-	DER_0
Fixture gating delay time	T_{fx}	sec.	0	fixture delay time

★ IEEE Std 802.3cd™-2018 Annex 93A.5
(Amendment to IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018 and IEEE Std 802.3bt™-2018)

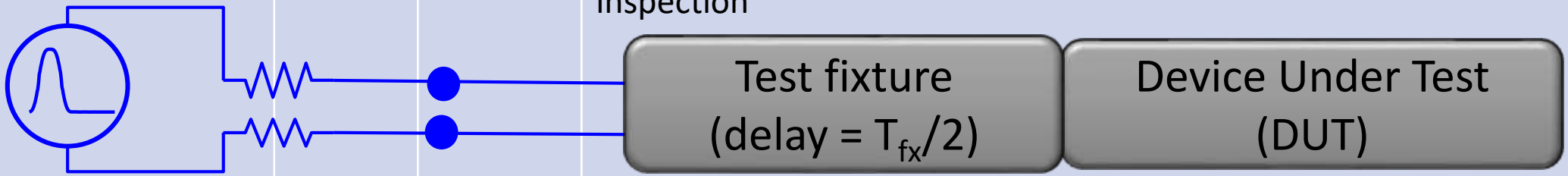
PULSE RESPONSE PARAMETERS APPLIED TO ACQUIRE A PTDR

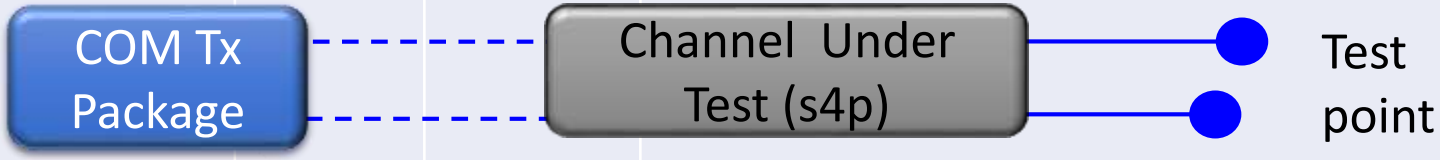


Parameter	Symbol	Units	COM Code Keyword
Signaling rate	f_b	GBd	f_b
20% to 80% Gaussian transition time associated with a pulse	T_r	Ns	TR_TDR
Receiver bandwidth for 4th order Butterworth Filter	f_r	f_b	f_r

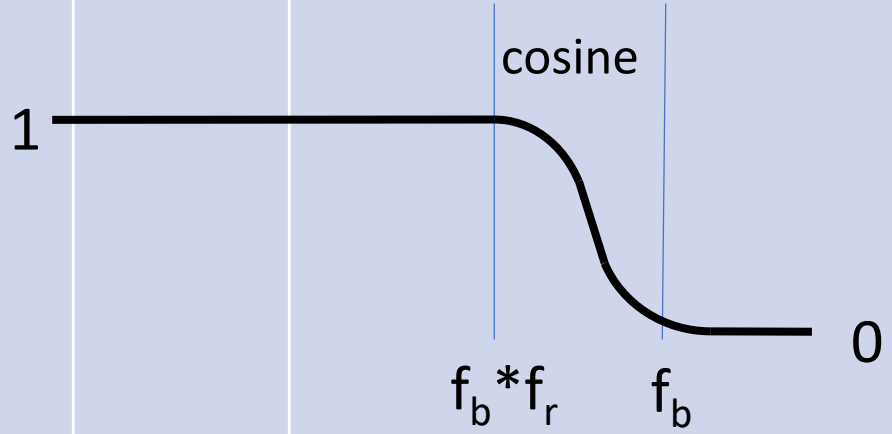
ADDITIONAL ERL COM CONTROL PARAMETERS

COM Code Keyword	Units	Symbol	Description
Fixture delay time	**s**	T_{fx}	Fixture gating delay time is twice the propagation delay in ns associated with the test fixture, obtained by measurement or inspection
TDR_W_TXPKG	**Logical**	**-**	1 cascades one selected package in the COM configuration file to the transmit end of the specified channel 0 no cascade action (default)





WINDOW FOR iFFT OF RL

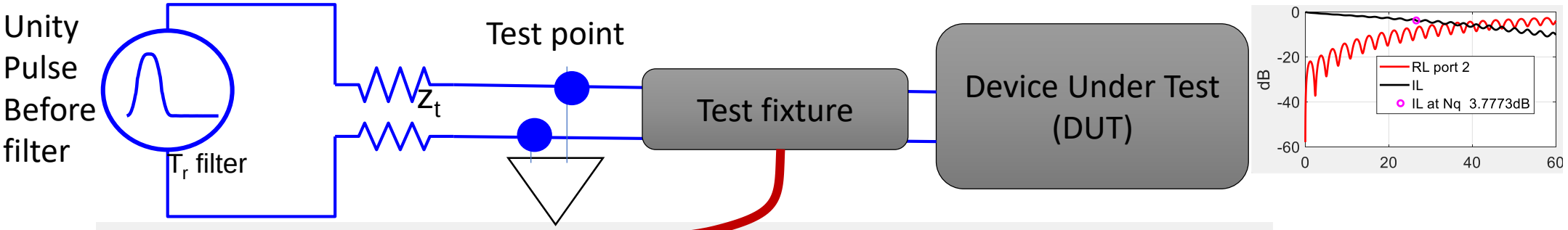
COM Code Keyword	Units	Symbol	Description
Tukey_Window	**Logical**	**-**	1 applies a Tukey filter to the PTRD increasing computational stability A Tukey window is also known as a cosine-tapered window 0 no filter is apply (default) 

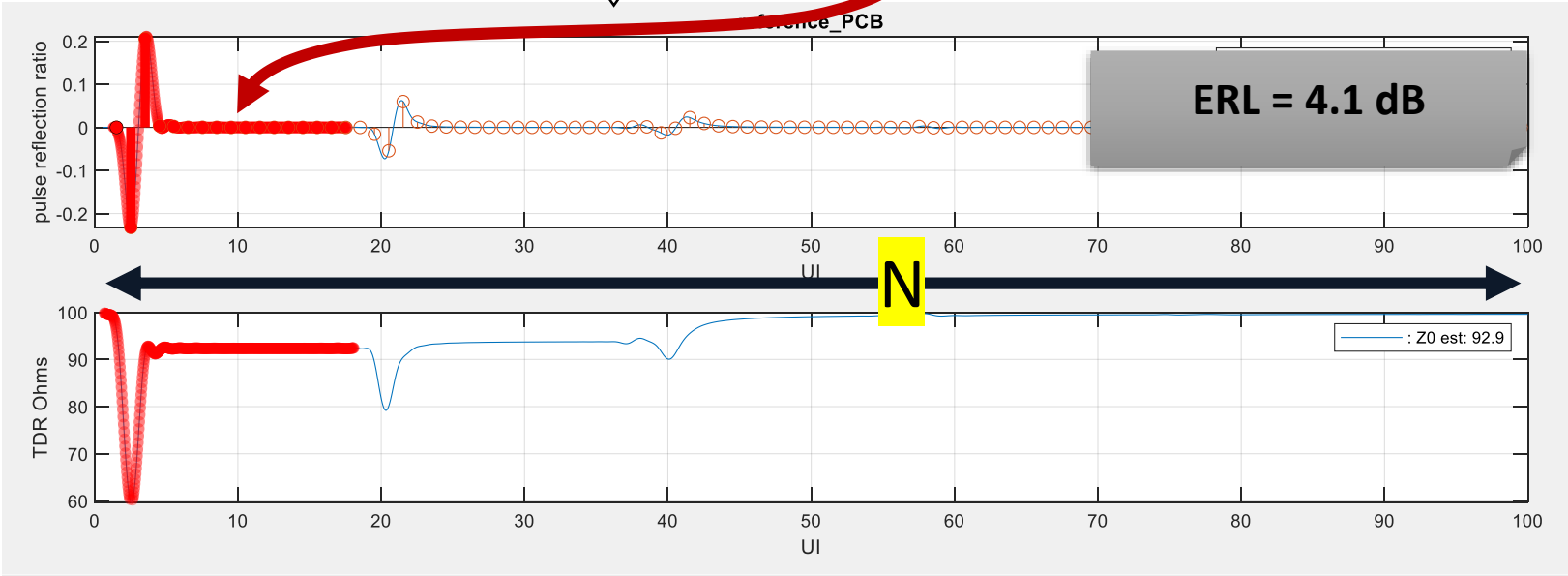
ADDITIONAL ERL COM CONTROL PARAMETERS

COM Code Keyword	Units	Symbol	Description
TDR	**logical**	**-**	0 Disables TDR 1 Enables TDR (required for ERL)
ERL	**logical**	**-**	0 Disables ERL computation 1 Enables ERL computation, requires TDR enabled
ERL_ONLY	**logical**	**-**	0 Enables COM computation (default) 1 Disables COM computation for faster runs

N IS NUMBER OF UI GATING TDR AND PTDR

Parameter	Symbol	Units	Default	COM Code Keyword
Length of the reflection signal	**N**	**UI**	**-**	**N**
Fixture gating delay time	T_{fx}	sec.	0	fixture delay time

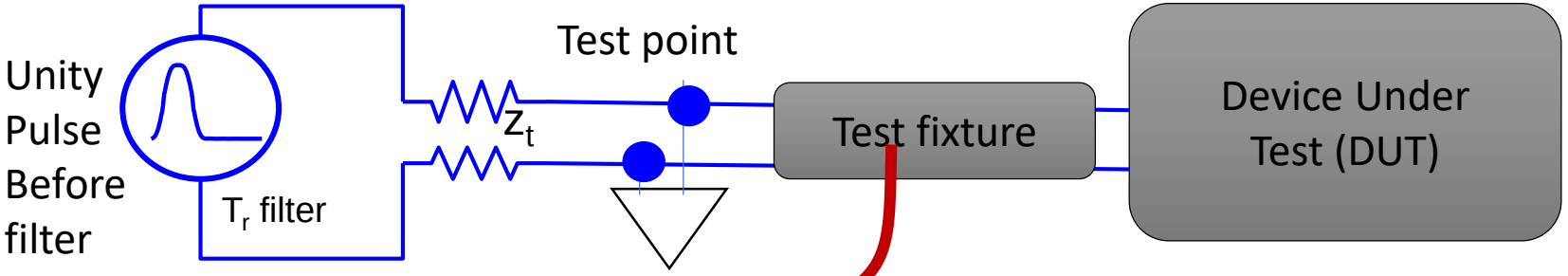


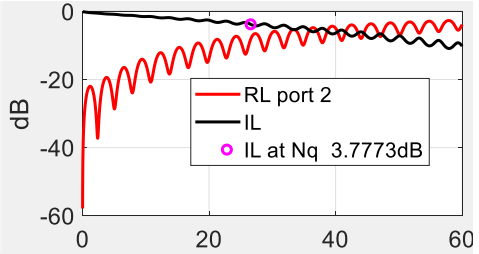


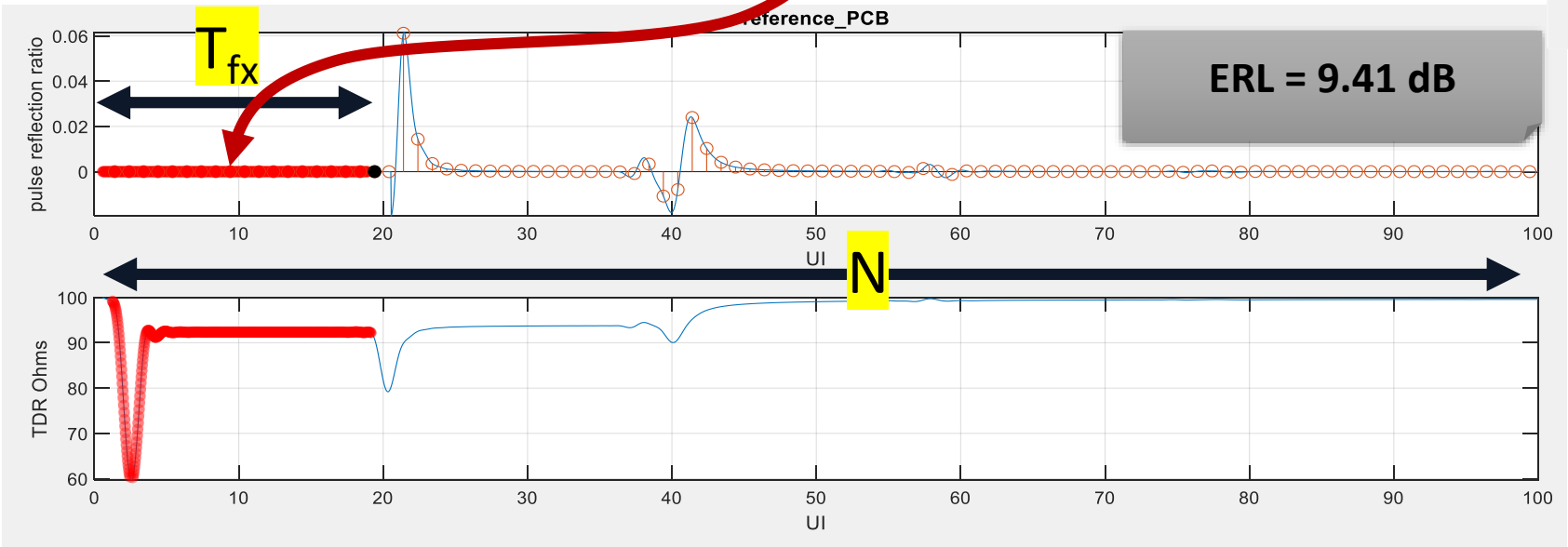
O We don't want the red dots in the ERL computation

T_{fx} IS NUMBER OF SECONDS WHICH GATES TDR AND PTDR FOR FIXTURE ADJUSTMENTS

Parameter	Symbol	Units	Default	COM Code Keyword
Length of the reflection signal	N	UI	-	N
Fixture gating delay time	T_{fx}	**sec.**	**0**	**fixture delay time**



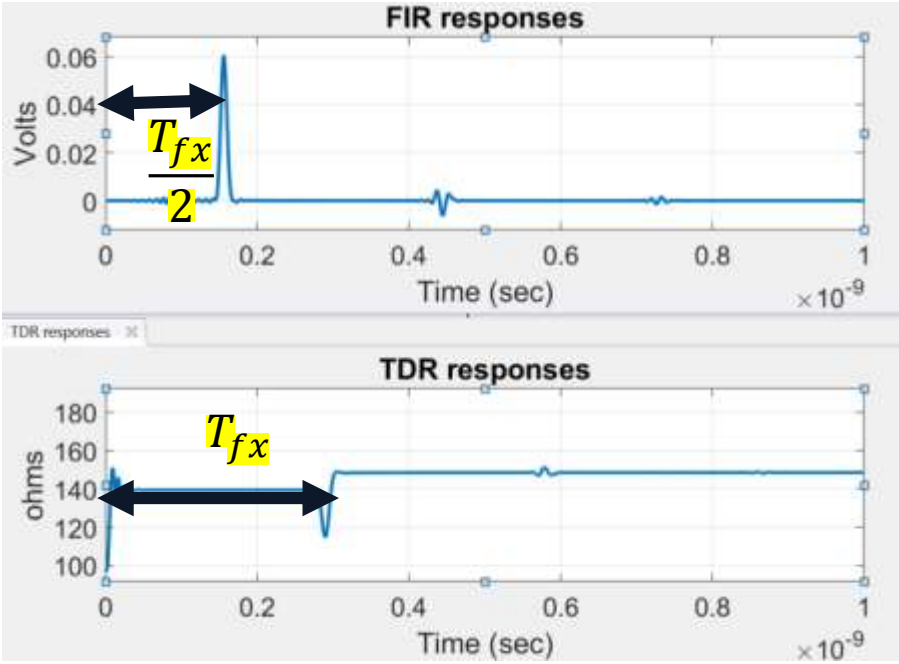




O Removing the red dots increases ERL from 4.1 to 9.4 dB

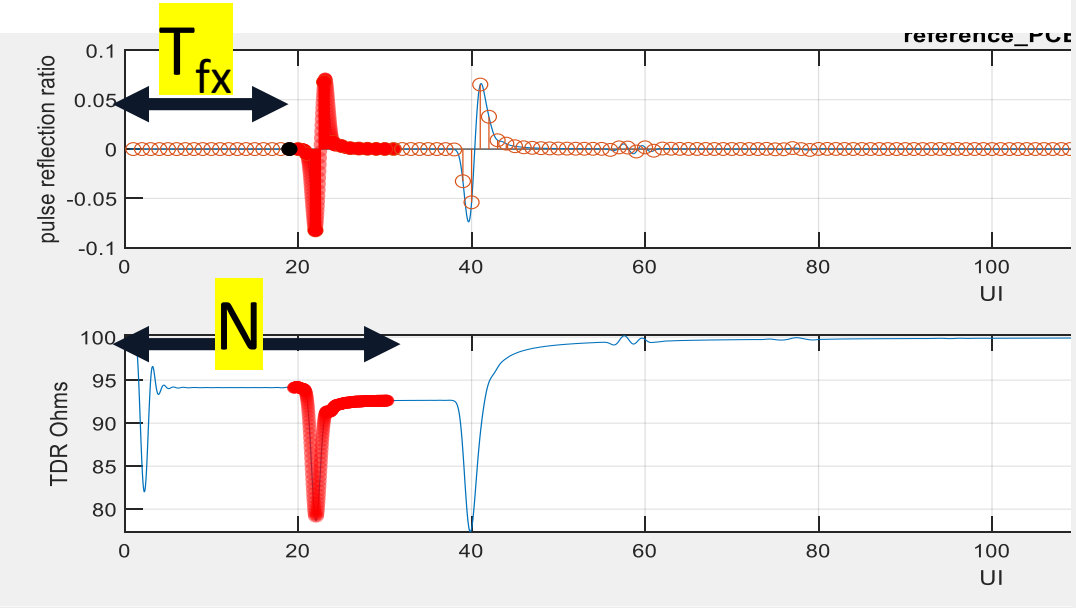
DETERMINING T_{fx}

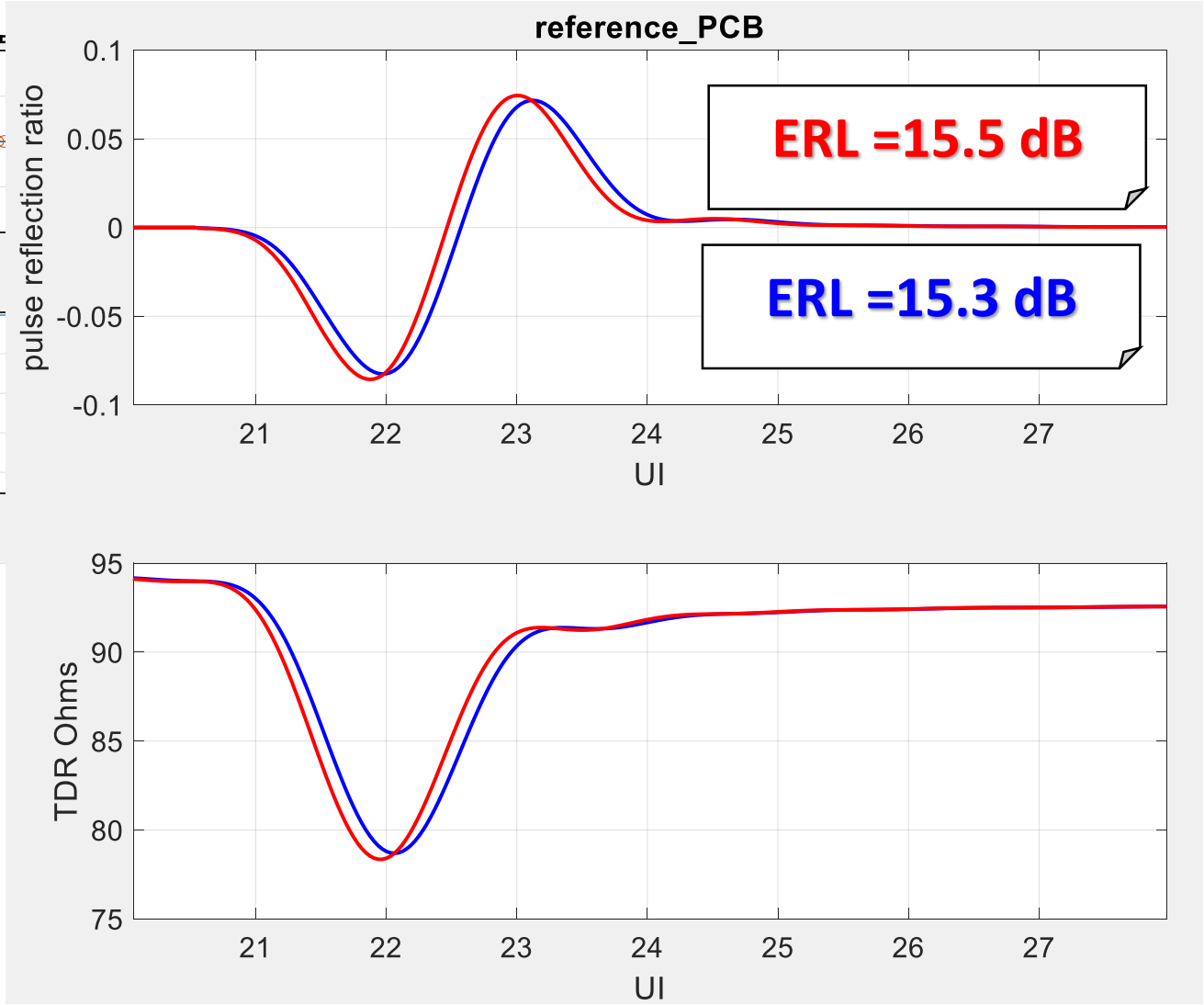
Test fixture → [s] →



- T_{fx} may be found by:
  - Acquiring a FIR (finite impulse response) from the fixture s-parameter
  - Double the time at which the peak of the FIR occurs

ERL FINE TUNING ACHIEVED BY ADJUSTING N AND T_{fx}





- The red curves at the right are with a reference via which may be modeled as a shunt 120 fF
- The blue curves at the right are the same via with 20 fF of reduce capacitance
  - I.e. modeled as 100 fF
- A 20 fF change in via impedance is quantifiable

ERL ADVANCED TOPICS

- Package Loss Compensation
- DFE adjustments (compensable ISI)
- Both use the parameter N_{bx} which is set equal to the total number of DFE taps, N_b
- The thinking is N_{bx} is linked to the highest expected package loss

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REVIEW OF ADVANCED FEATURE PARAMETERS

Parameter	Symbol	Units	Default	COM Code Keyword
Equalizer length associated with reflection signal	N_{bx}	UI	DFE n	N_bx
Incremental available signal loss factor	β_x	GHz	0	beta_x
Permitted reflection for an external connection at the test point	ρ_x	—	0.618	rho_x

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PACKAGE LOSS COMPENSATION

- Short packages have more reflection but less loss
- For systems with maximum die to die loss, the package loss tends to be much greater than package reflections
  - Remember that package reflections are also already included end to end loss
- Goal: Adjust the effective return loss to compensate
- Originally G_{loss} , fitted time gating/weighting function, was applied to PTDR

$$G_{loss} = 10^{\frac{\beta_x\left(t-T_{fx}-T_b(N_b+1)\right)}{20}}$$

- However since G_{rr} and G_{loss} have similar gating properties and it was decided to only use G_{rr} for this purpose
  - i.e. set β_x is zero which sets G_{loss} to 1

DFE ADJUSTMENTS (COMPENSABLE ISI)

- All reflections are not equal
- Goal: Adjust the effective return loss to accommodate a DFE which may remove the effects of some reflections at the receiver
- Solution: Apply fitted time gating/weighting function G_{ff} to the PTDR waveform

$$G_{rr} = \rho_x(1+\rho_x)e^{-\frac{\left(\frac{t-T_{fx}}{UI}-(N_b+1)\right)^2}{(N_b+1)^2}}$$

- The amount of allowable re-reflection is captured by ρ_x
- As mentioned earlier this can be used to account for loss too

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G_{rr} CAVEATS

- Some reflections nullified at the receiver but
  - The actual reflection waves are not removed from the channel and are free to reverberation with other discontinuities
- The parameter N_{bx} is used to adjust the PTDR waveform
  - It is usually the same as the number of DFE taps
- N_{bx} is not appropriate for all topologies and test point
- The latest standards sets the value of ρ_x to 0.618
- Locking down ρ_x and β_x simplified setting of ERL pass fail limits
  - Reduces the number of moving parts

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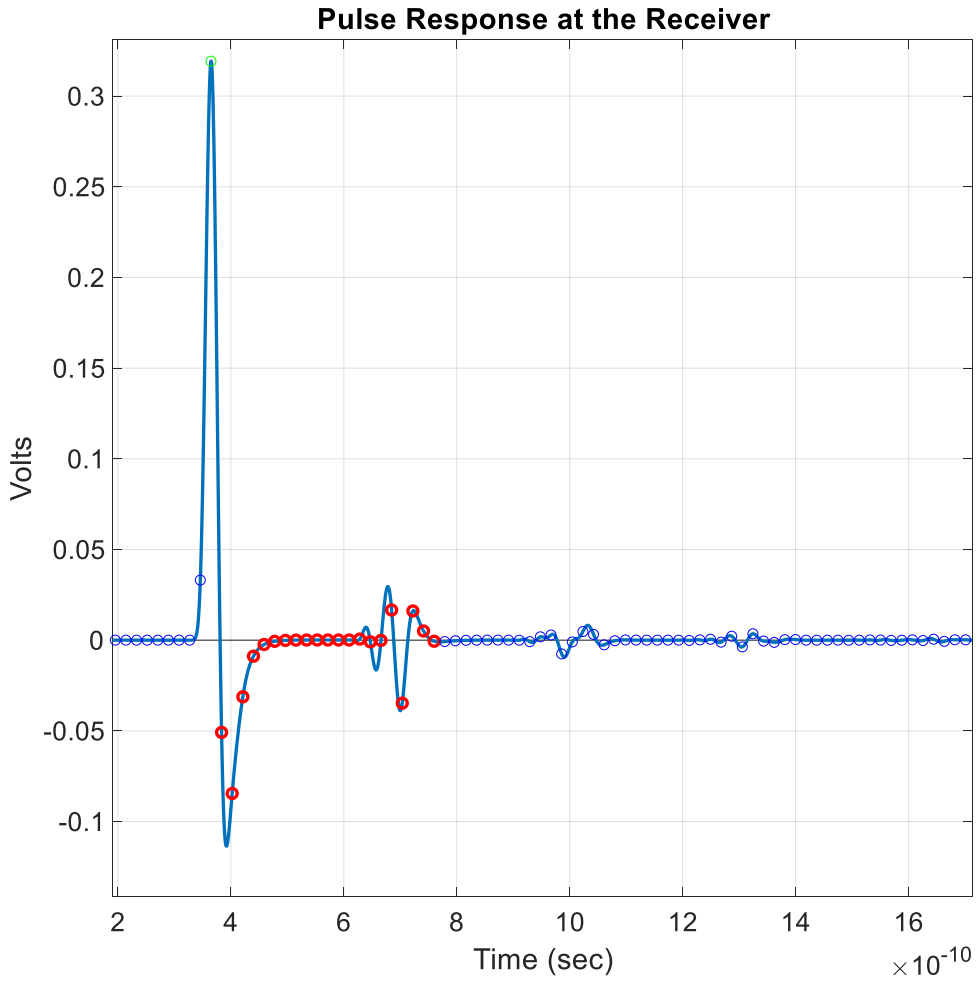
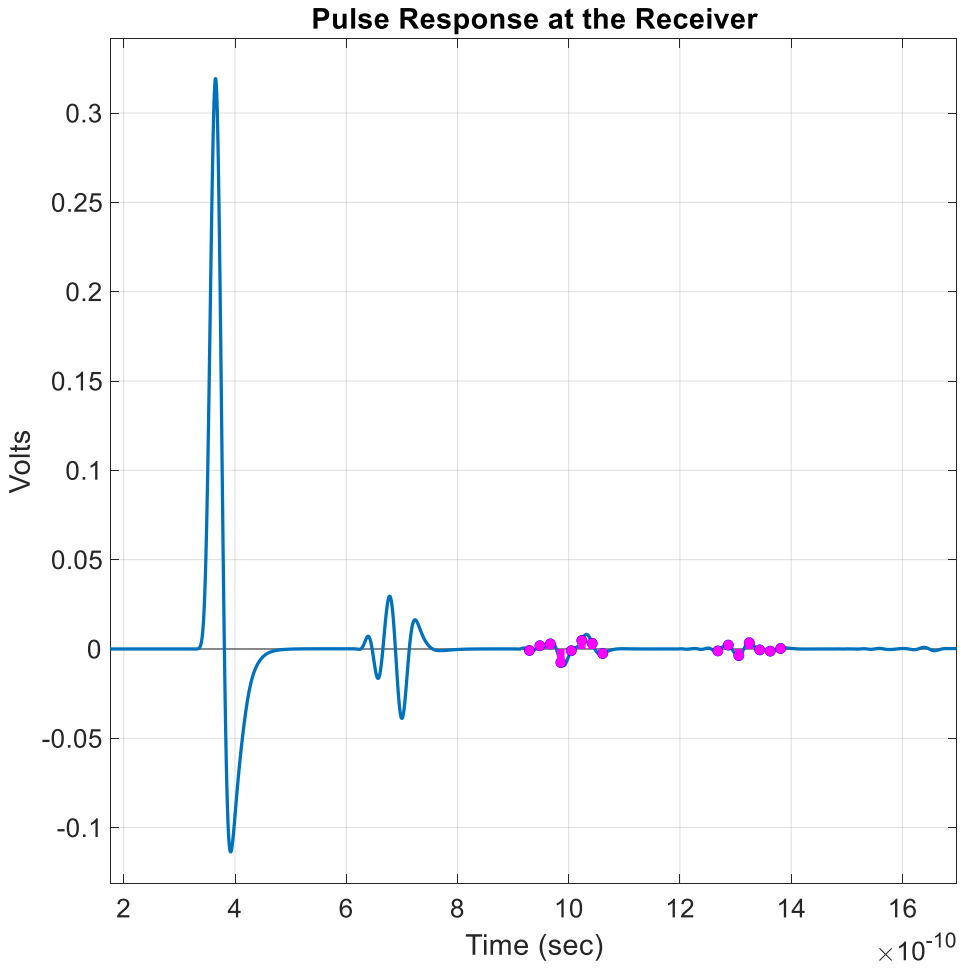
DFE OPERATIONS ON AN Rx PULSE RESPONSE

- A DFE might interpret the response in red dots at the right as zero volts
- 21 DFE taps
- The DFE offers some protection against discontinuities in a package and BGA break out reflections
- Time gating and weighting accommodates this



ALL IS NOT GONE

- The magenta signal is a direct result of the signal highlighted in red in the previous slide
- There are still interactions the DFE will not remove
- So we only remove a portion of these reflections in the PTDR



REFLECTION GATING AND WEIGHING

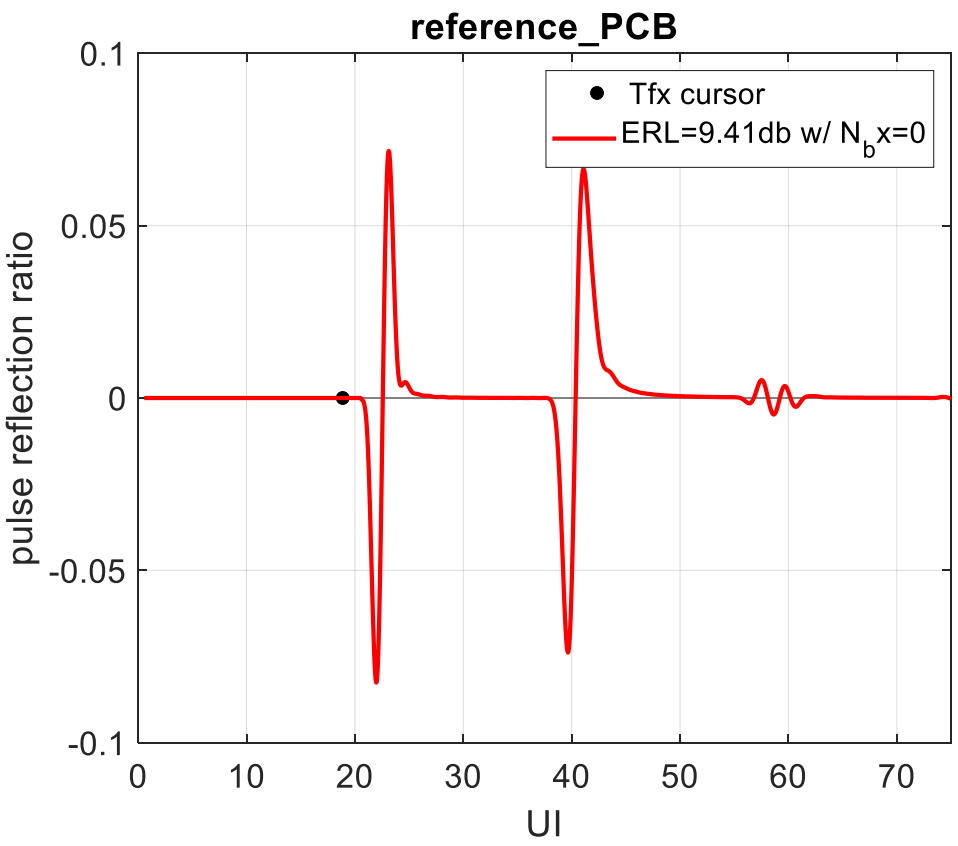
From a previous slide

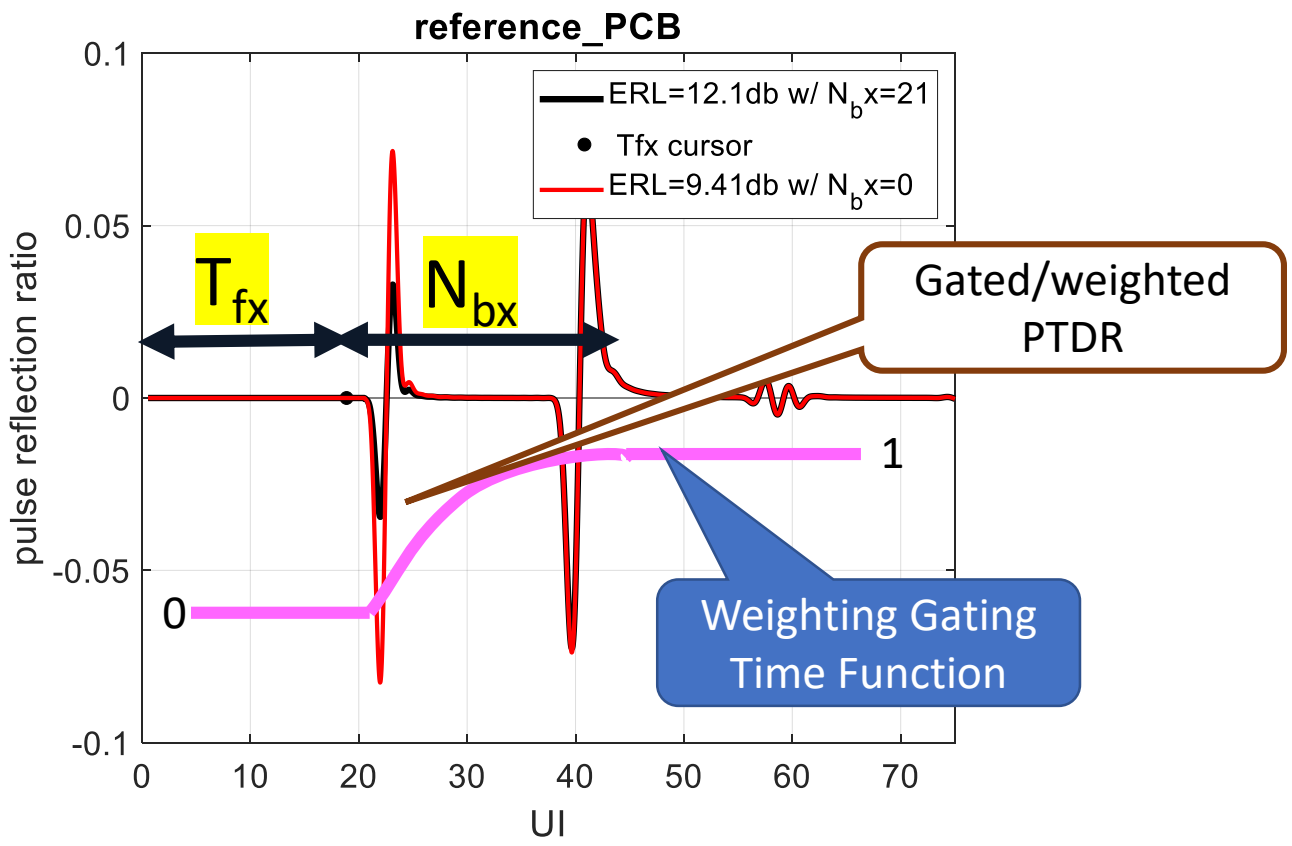
- ERL really uses $R_{eff}(t)$

$$R_{eff}(t) = G_{loss}(t)\, G_{rr}(t)\, PTDR(t)$$

- $G_{loss}(t)\, G_{rr}(t)$ is a weighting gating function
- Now let's looks at a simple example

USAGE MODEL: GRAPHIC VIEW OF WEIGHTING GATING TIME FUNCTION





The Weighting Gating Time Function has 0 value before T_{fx} and 1 after $N_{bx}+T_{fx}$

SUMMARY

- ERL is scalar number representing return loss for
  - For a particular data rate, required BER, and signaling (NRZ, PAM4, PAM6 …)
- ERL may account for package loss and a DFE
- ERL is computed from a pulse TDR (PTDR)
- PTDR looks like a derivative of TDR
- ERL is normatively specified for many standard with data rates above 50 Gb/s
- ERL may be used to tune design features
  - By adjusting timing parameters

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Backup Data

COM References

- COM Matlab download

http://www.ieee802.org/3/ck/public/tools/tools/mellitz_3ck_adhoc_01a_090920_COM2p95.zip

- Early paper on COM

https://pdfs.semanticscholar.org/7e9c/b8b162fe93a131d37fa1408fb56d9e5b05f8.pdf

ERL References

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- “Effective Return Loss for 112G and 56G PAM 4”; R. Mellitz, Dr. E. P. Sayre DesignCon 2018; Santa Clara, Ca, USA
- “Practical Implementation of Testing 50-Gbps per Lane Effective Return Loss (ERL)”, C. DiMinico, C. Donahue O.J. Danzy, R Mellitz, M Resso, M. Sapozhnikov, M. Klempa; DesignCon 2019, Santa Clara, Ca, USA

Example COM Configuration

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	[0.3 0.2*ones(1,10)]		
b_min(1)	0.3		
b_min(2..N_b)	[0.05 -0.03*ones(1,10)]		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	8	dB
DER_0	0.0001	
T_r	0.0075	ns
FORCE_TR	1	logical
Local Search	2	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MAT	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3500	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	21	UI
Tukey_Window	1	logical
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*110.3*	mm
z_bp (NEXT)	*110.3*	mm
z_bp (FEXT)	*110.3*	mm
z_bp (RX)	*110.3*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.594	*Fb
f_f	0.594	*Fb
f_n	0.594	*Fb
f_2	40.000	GHz
A_ft	0.600	V
A_nt	**0.600**	V
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

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