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XTLK Mitigation Strategies in 12G-SDI Systems

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INTRODUCTION

The purpose of today's discussion is to demonstrate techniques to reduce crosstalk in 12G SDI systems.

Some key points:

- Crosstalk in a typical implementation can be bad.
- How to assign pins effectively in edge card connectors for improved crosstalk.
- Eliminating the legacy floating pin whilst meeting Return Loss requirements.
- How simple changes can lead to a >40dB crosstalk improvement.

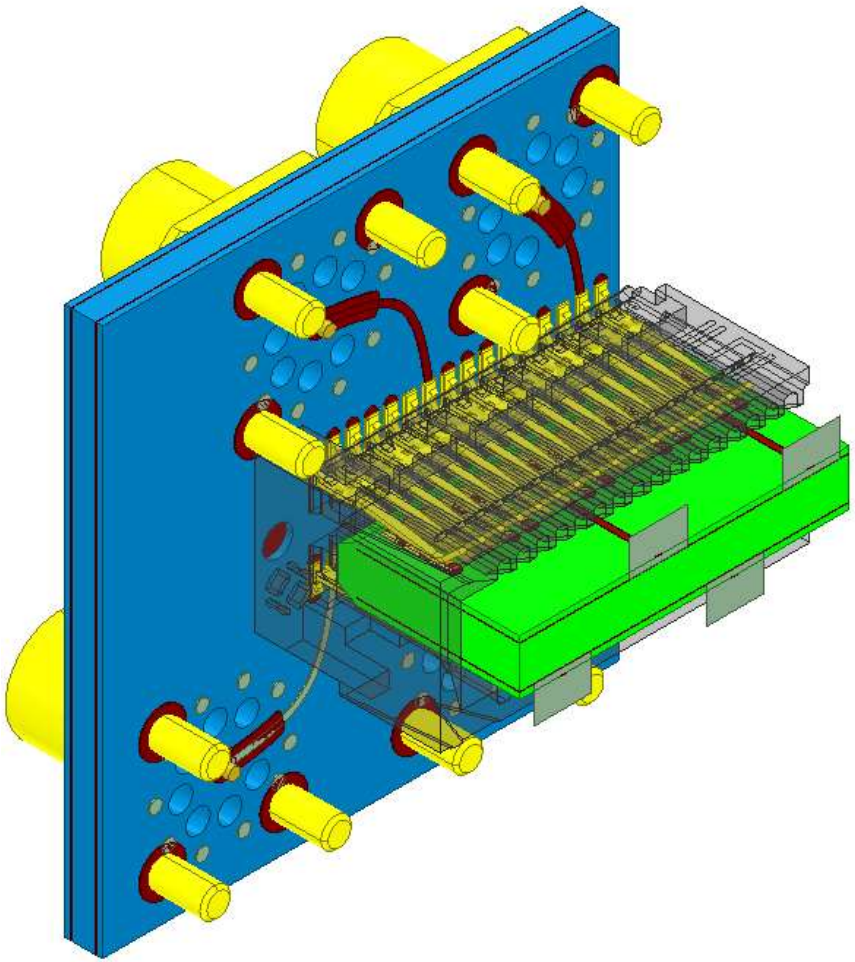
SDI Data Rates "Reference"

Standard	Name	Introduced	Bitrates	Example video formats
SMPTE 259M	SD-SDI	1989[2]	270 Mbit/s, 360 Mbit/s, 143 Mbit/s, and 177 Mbit/s	480i, 576i
SMPTE 344M	ED-SDI	2000[8]	540 Mbit/s	480p, 576p
SMPTE 292M	HD-SDI	1998[2]	1.485 Gbit/s, and 1.485/1.001 Gbit/s	720p, 1080i
SMPTE 372M	Dual Link HD-SDI	2002[2]	2.970 Gbit/s, and 2.970/1.001 Gbit/s	1080p60
SMPTE 424M	3G-SDI	2006[2]	2.970 Gbit/s, and 2.970/1.001 Gbit/s	1080p60
SMPTE ST 2081	6G-SDI	2015[4]	6 Gbit/s	1080p120, 2160p30
SMPTE ST 2082	12G-SDI	2015[5]	12 Gbit/s	2160p60
SMPTE ST 2083	24G-SDI	In development[9][10]	24 Gbit/s	2160p120, 4320p30

Agenda

- An example system with an HDBNC front panel plugged into an edge card.
- A typical design and the performance.
  - Illustrating how 3G SDI design practices break down wrt XTLK
- How to successfully use 50 ohm edge card connectors for 75 ohm applications.
- Orders of magnitude improvement in crosstalk are possible with proper floor planning in the early design stages.
  - Backed up with simulation

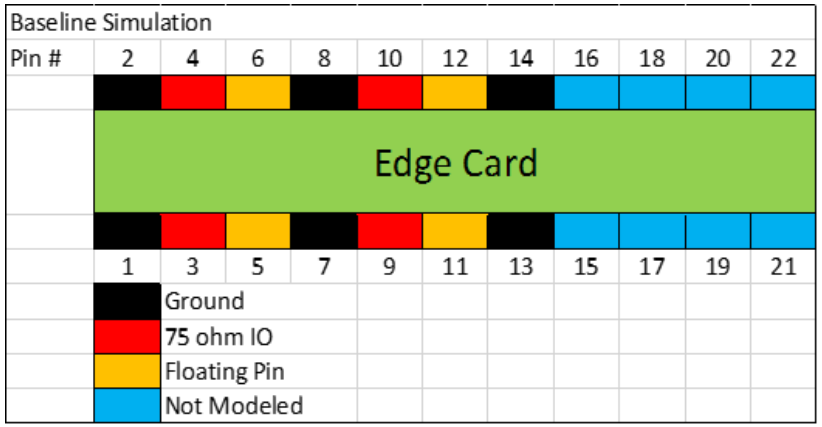
Model Overview



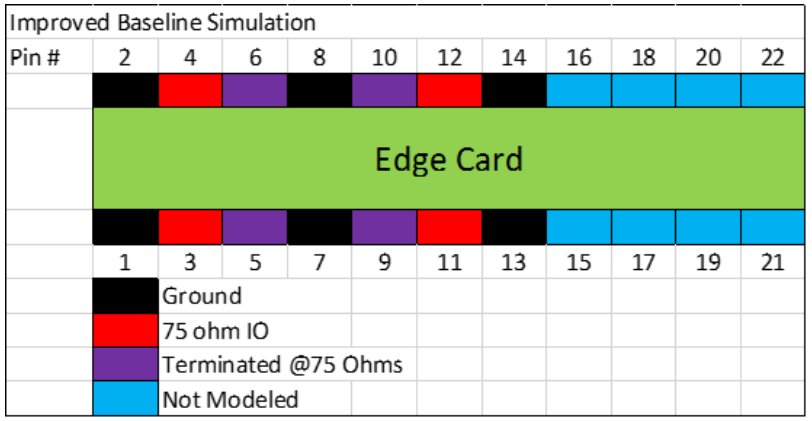
- For this exercise, a four-channel model was created.
- Several typical impairments were included in the baseline simulation.
- The improvements in performance were achieved by:
  - Breakout optimization
  - Terminating pins in the pin field strategically to dampen crosstalk.
  - Adding additional space between signals
  - "Staggering when appropriate."

Cases "Pin Assignments"

Case 1

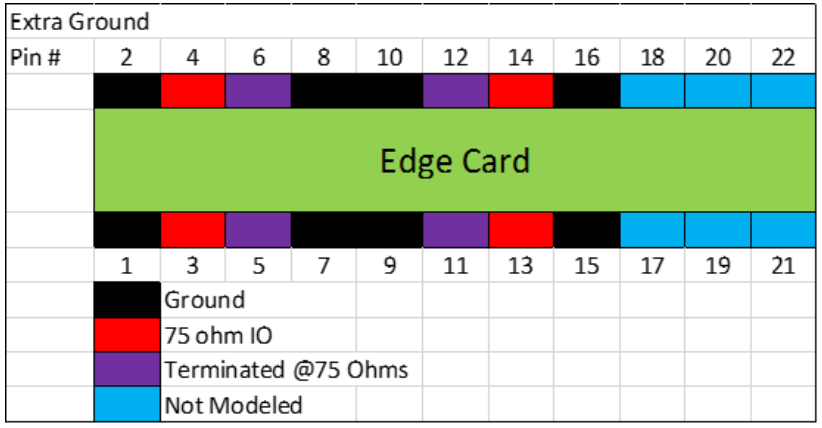


Case 2**

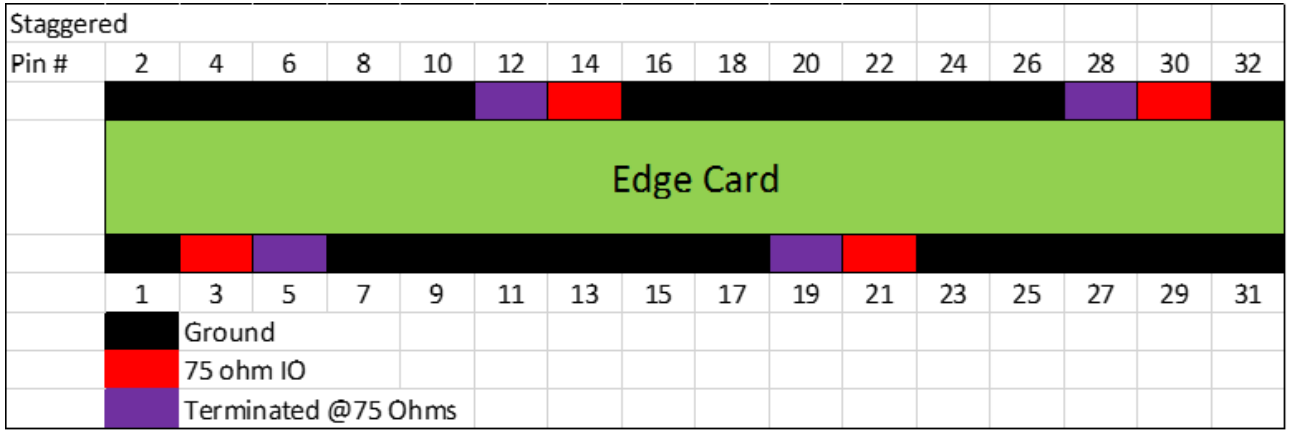


Note** Case 2 ran with terminated and floating pins

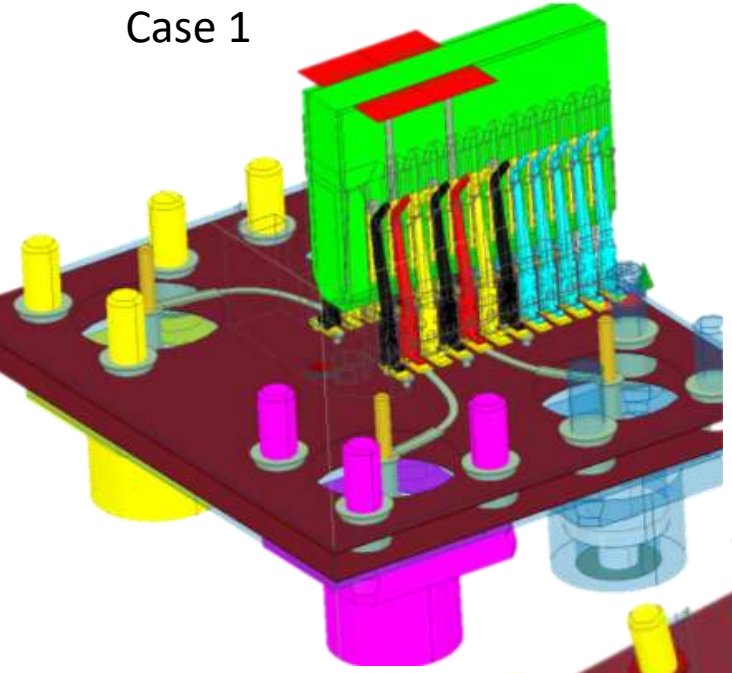
Case 3

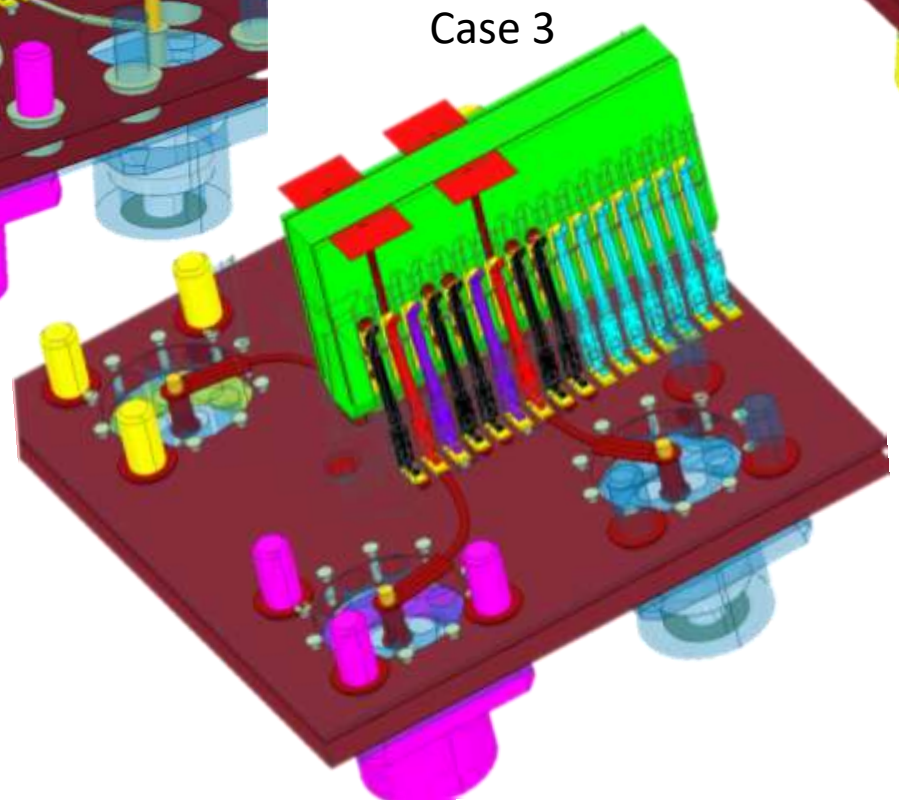


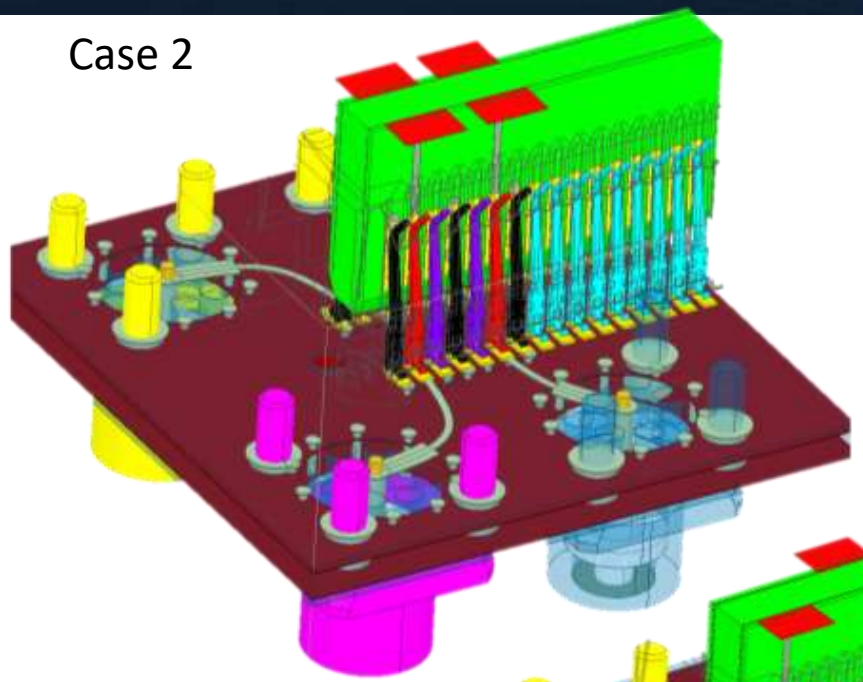
Case 4

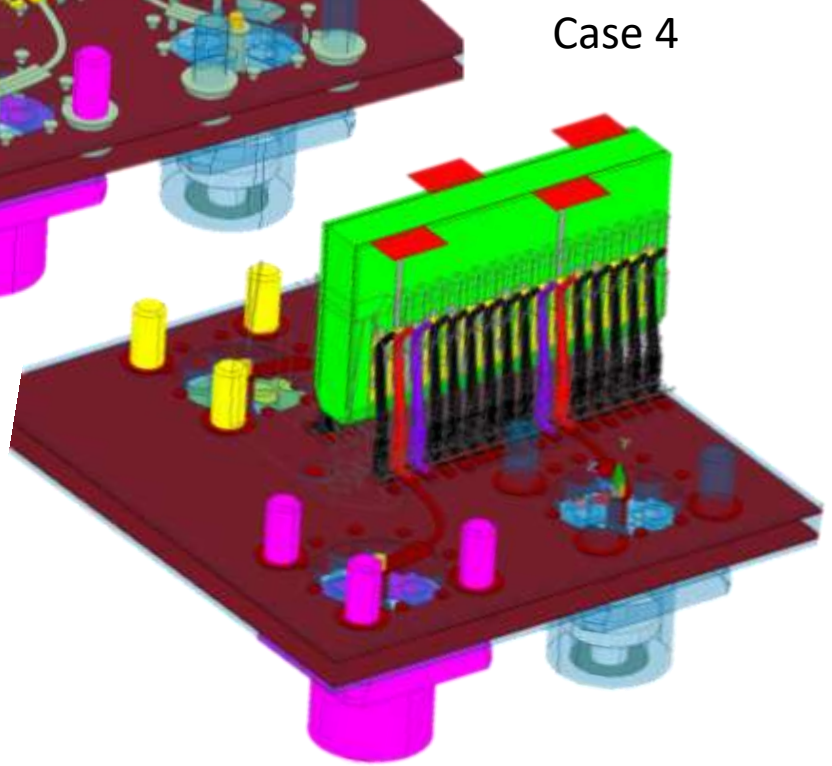


Cases "Model Snap Shots"

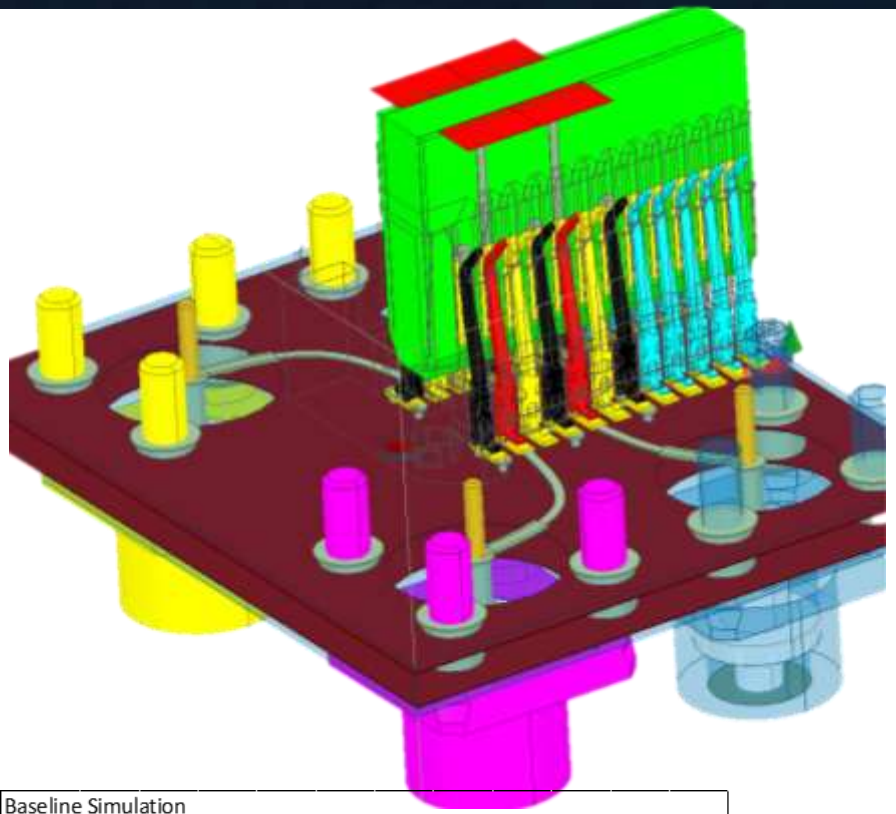








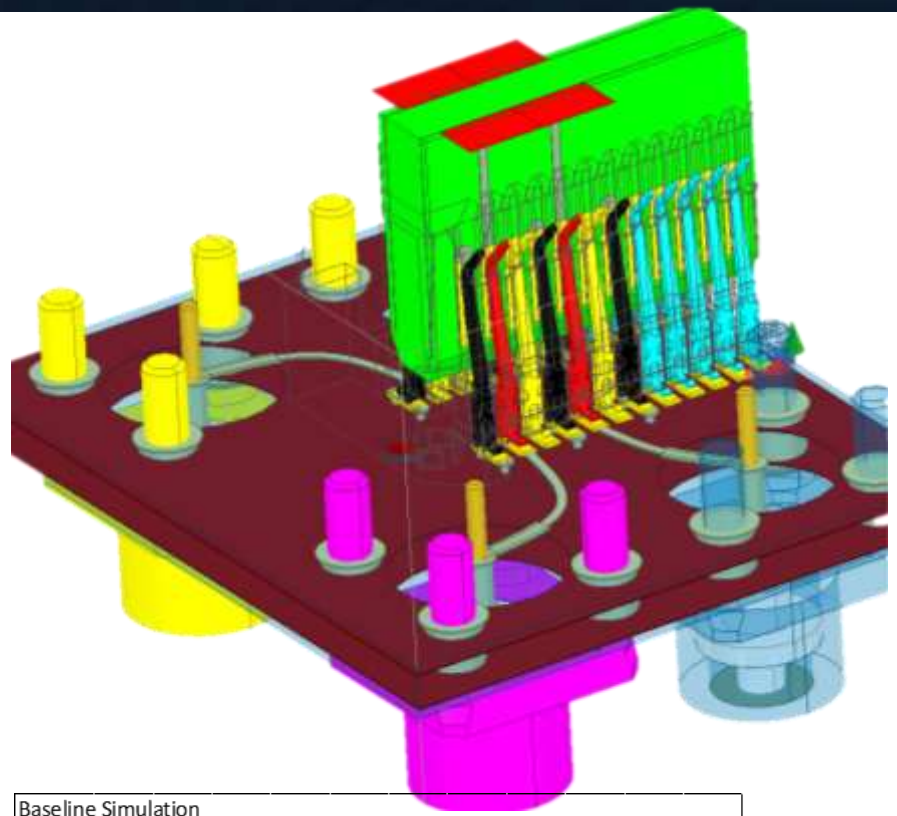
Case 1: Performance

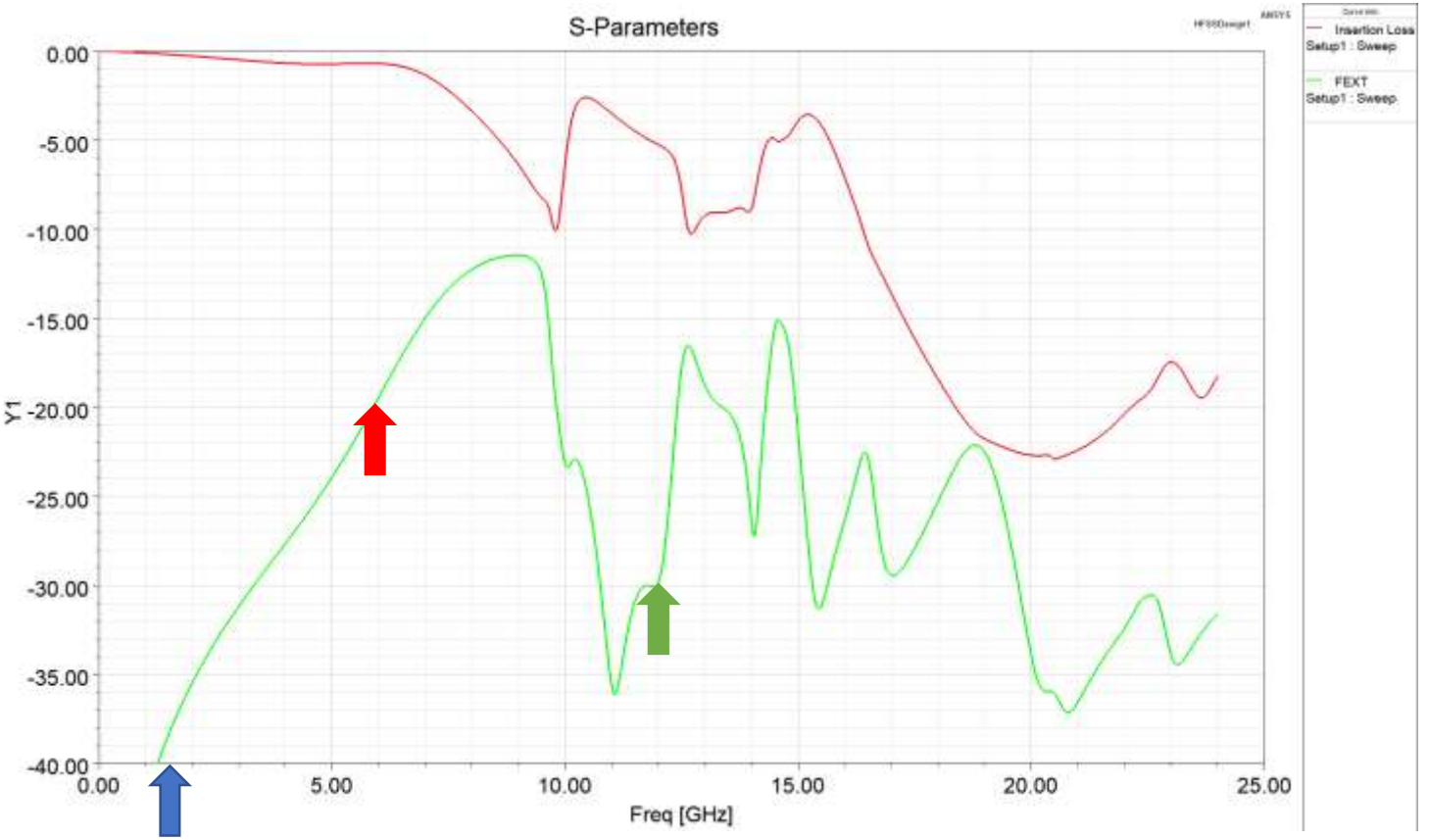


Baseline Simulation											
Pin #	2	4	6	8	10	12	14	16	18	20	22
	Edge Card										
	1	3	5	7	9	11	13	15	17	19	21
	Ground										
	75 ohm IO										
	Floating Pin										
	Not Modeled										

- Typical 3G SDI implementation that meets 12G SDI RL Mask…
- However it lacks key optimization features which leads to poor insertion loss and crosstalk performance.

Case 1: Performance Issues





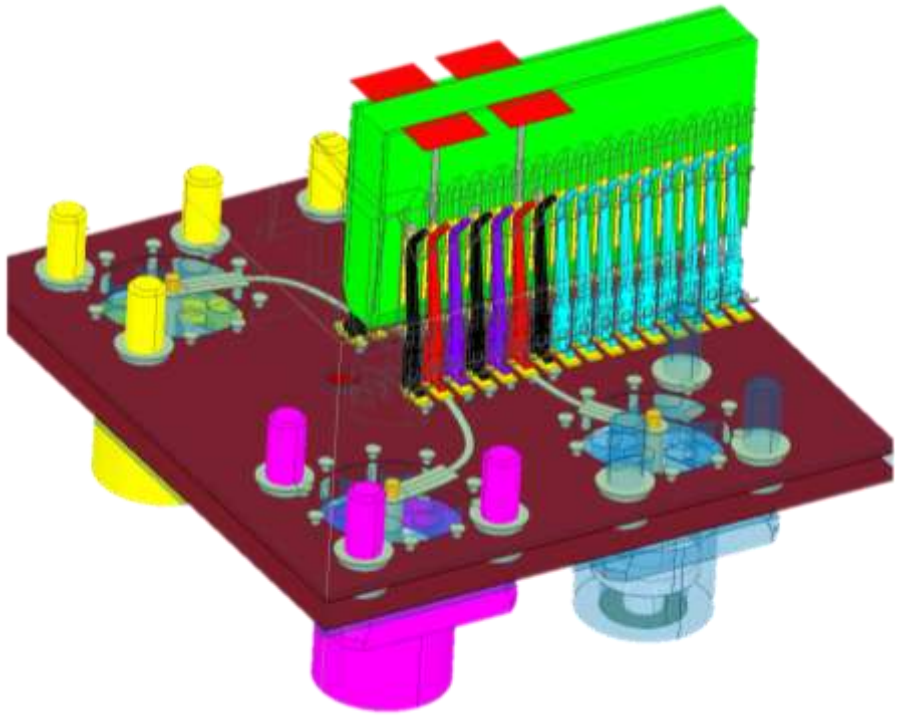
Baseline Simulation

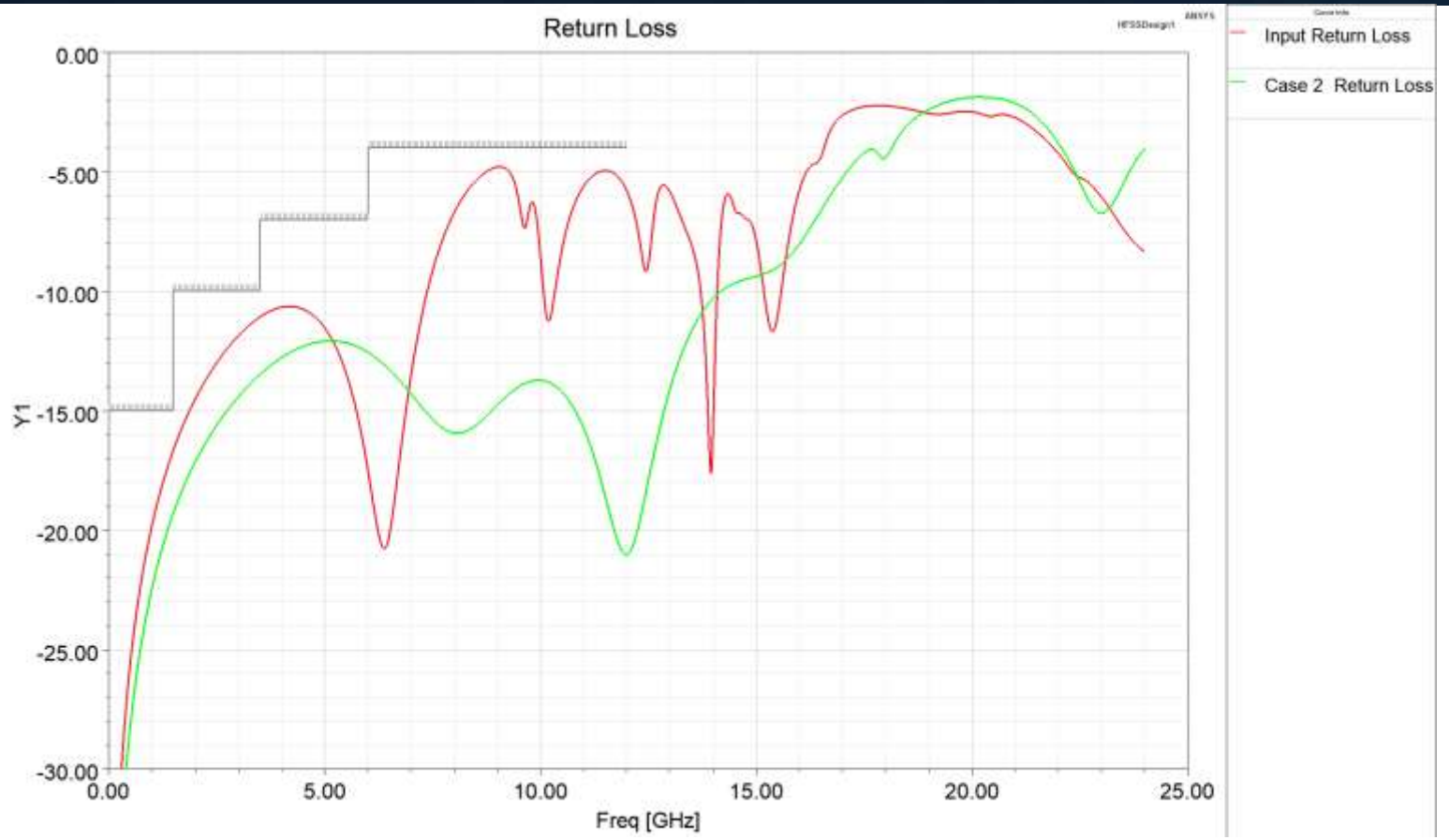
Pin #	2	4	6	8	10	12	14	16	18	20	22
	Edge Card										
	1	3	5	7	9	11	13	15	17	19	21

Ground
75 ohm IO
Floating Pin
Not Modeled

- Design details necessary for improving this design.
  - Radial ground stitching around HDBNC anti-pad
  - 75 ohm terminations on both sides of HSEC8 pins that were floating.
  - Extra anti-pad tuning on HSEC8 Edge card
  - Pin out changes to increase physical spacing where necessary for improved isolation

Case 2: Performance Vs. Case 1

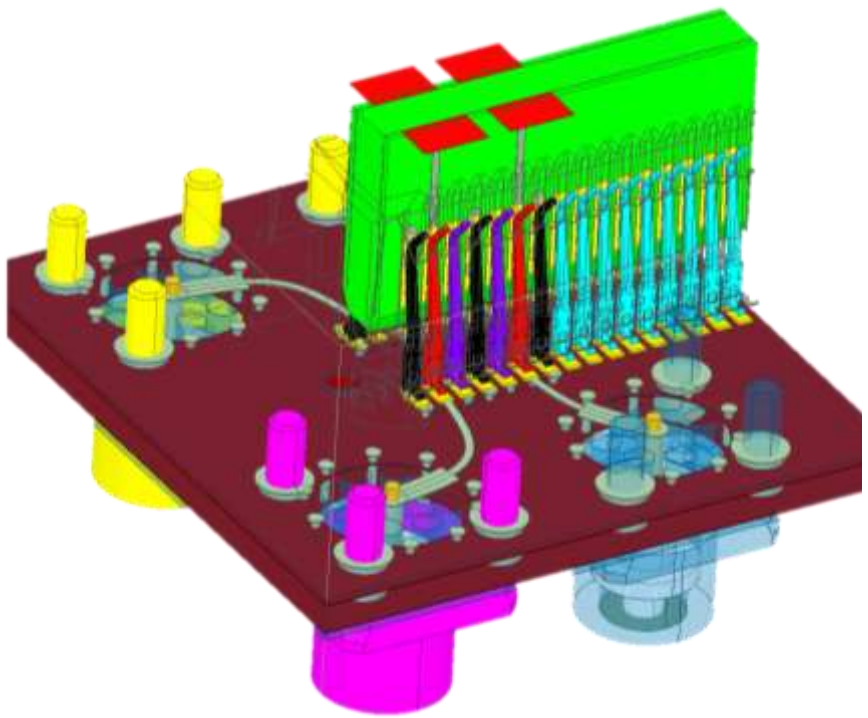


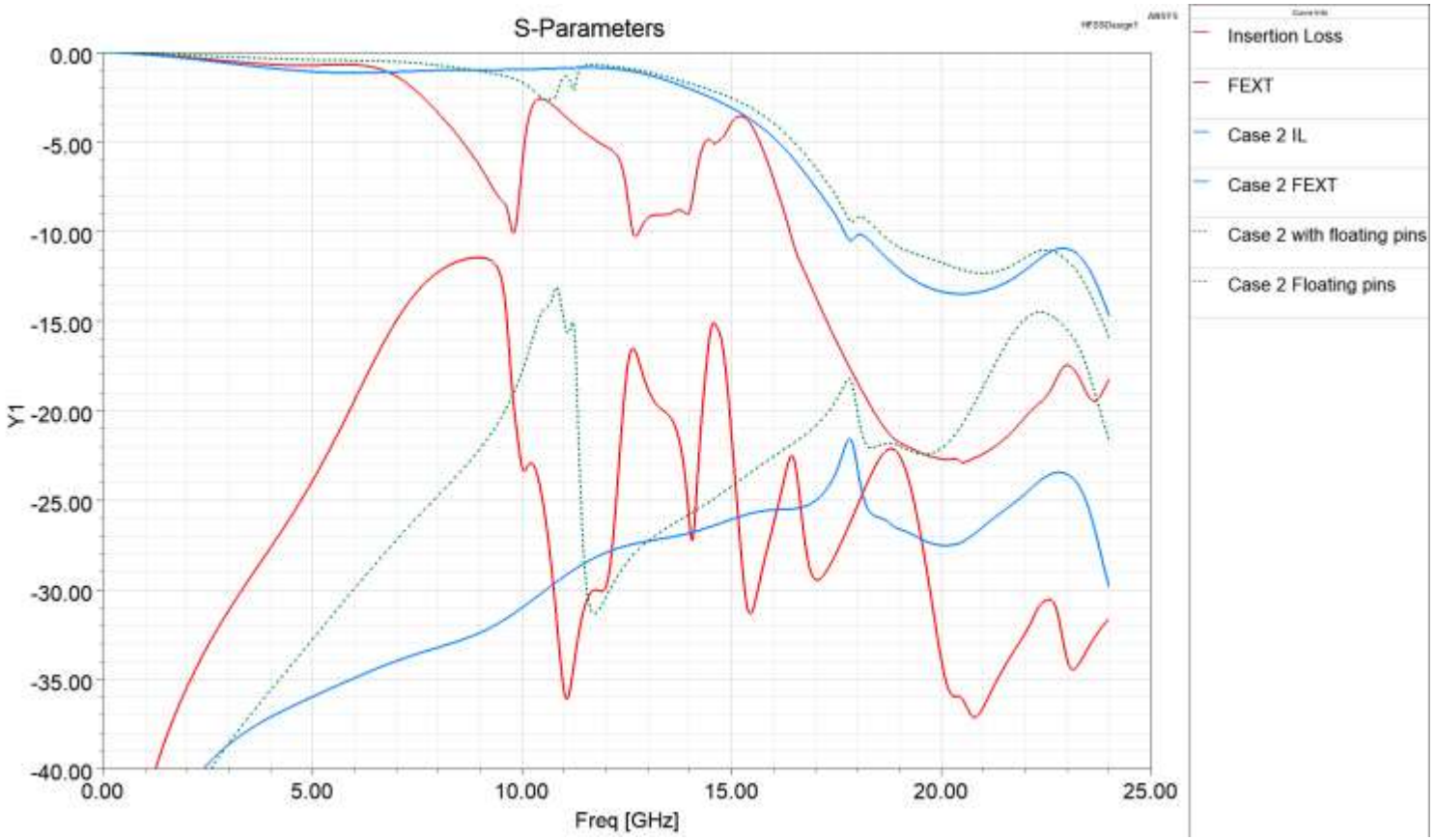


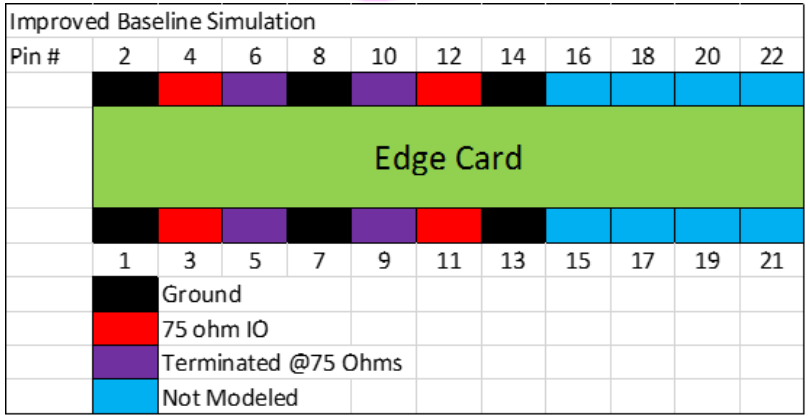
Improved Baseline Simulation											
Pin #	2	4	6	8	10	12	14	16	18	20	22
	Edge Card										
	1	3	5	7	9	11	13	15	17	19	21
	Ground										
	75 ohm IO										
	Terminated @75 Ohms										
	Not Modeled										

- Changes vs. Case 1
  - Radial ground stitching around HDBNC anti-pad
  - 75 ohm terminations on both sides of HSEC8 pin that was floating
  - Extra anti-pad tuning on HSEC8 Edge card
  - Pin out changes to increase physical spacing where necessary for improved isolation

Case 2: Performance Vs. Case 1

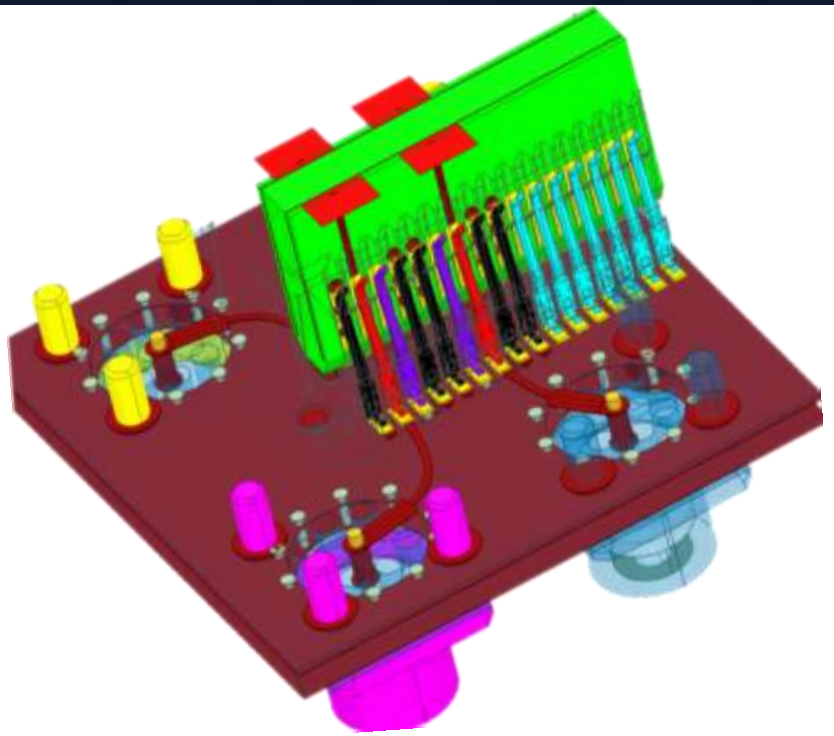


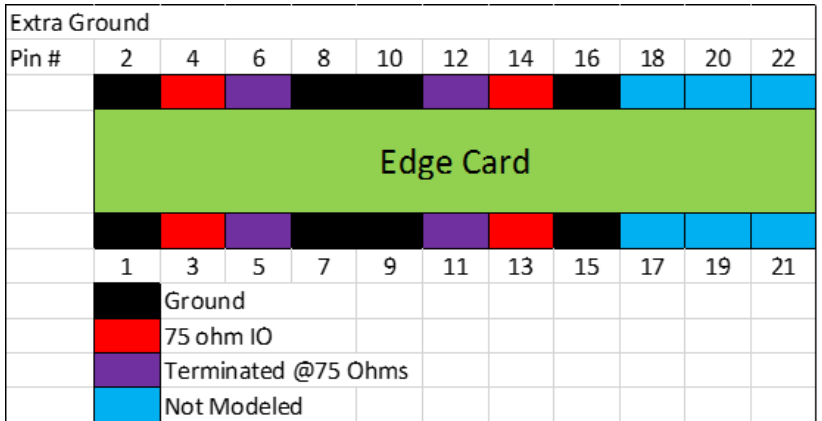


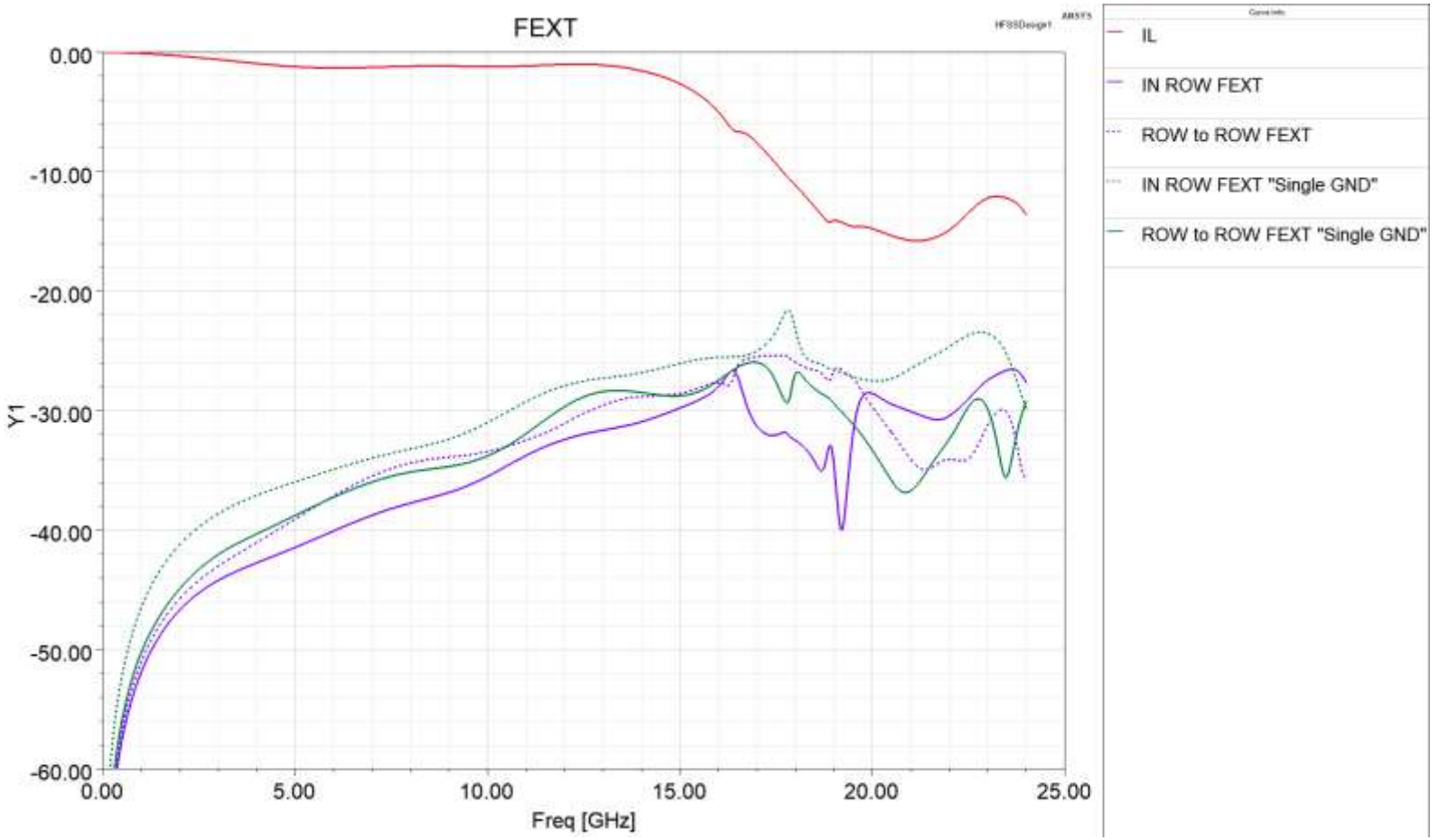


- Changes vs. Case 1
  - Radial ground stitching around HDBNC anti-pad
  - 75 ohm terminations on both sides of HSEC8 pin that was floating
  - Extra anti-pad tuning on HSEC8 Edge card
  - Pin out changes to increase physical spacing where necessary for improved isolation

Case 3: Performance

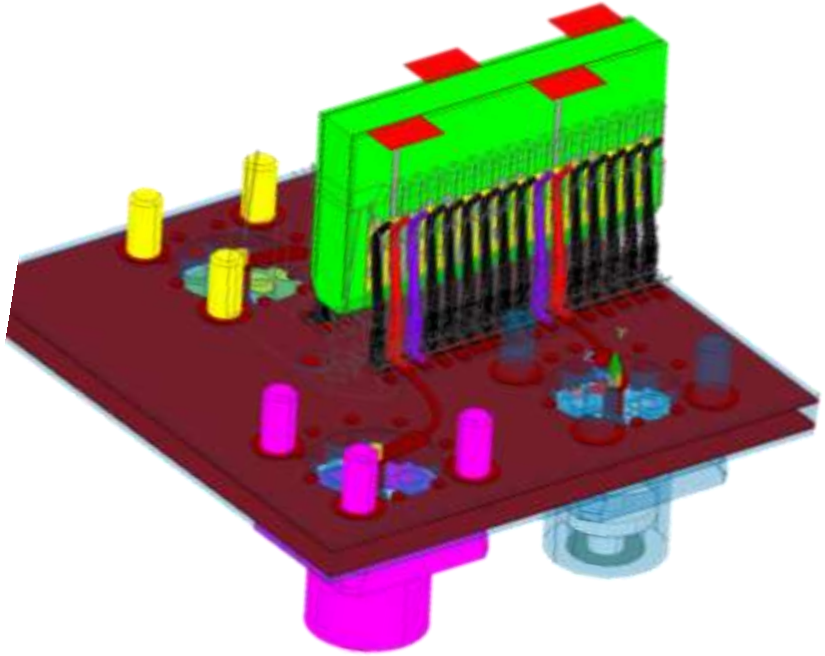


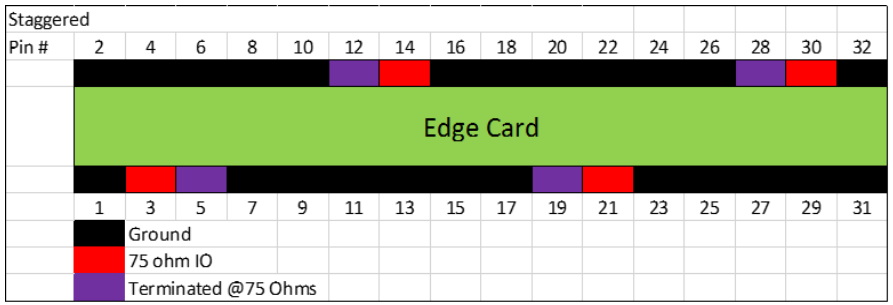


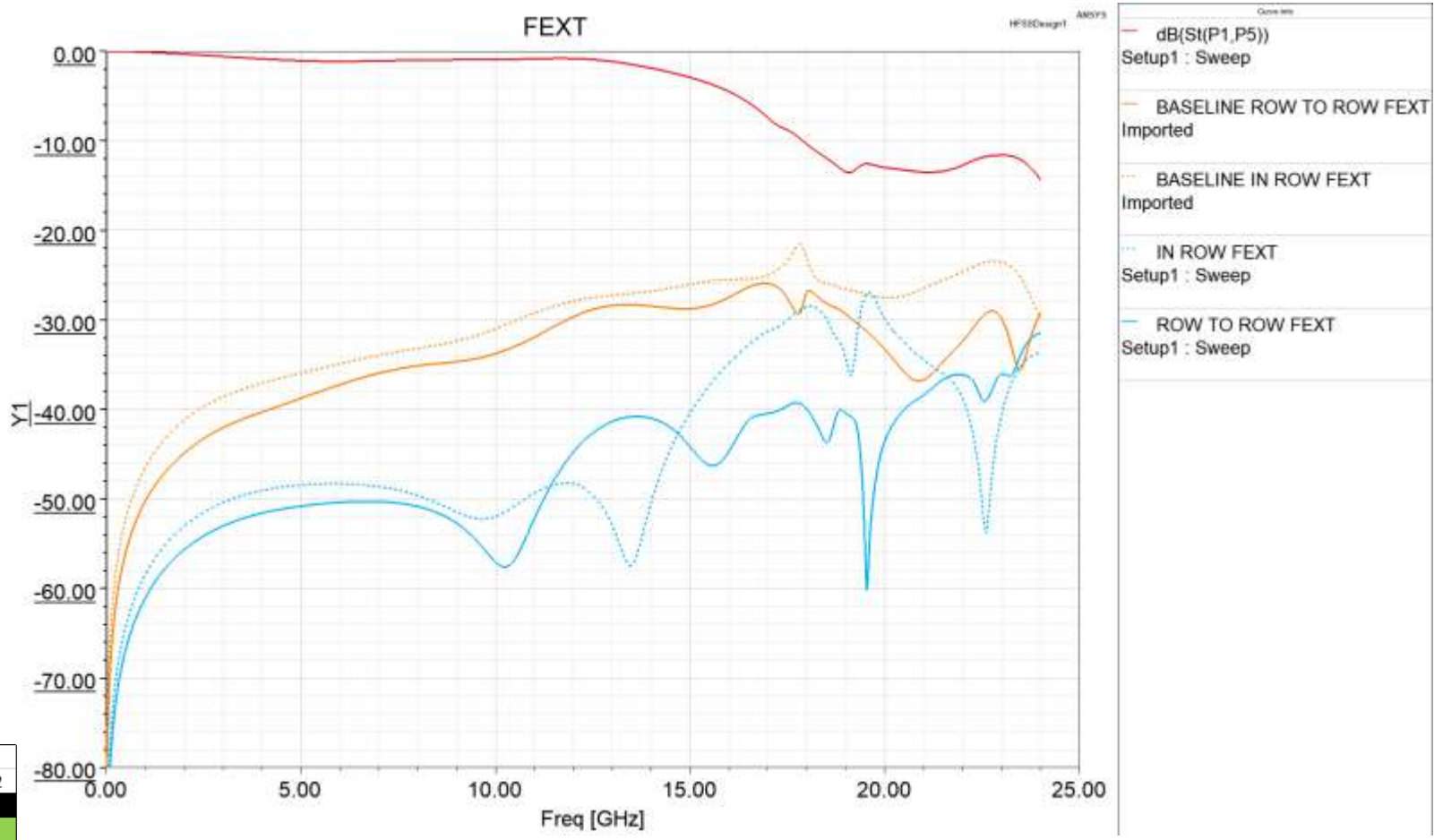


- This case added one more ground and introduces Row to Row XTLK issues.

Case 4: Performance





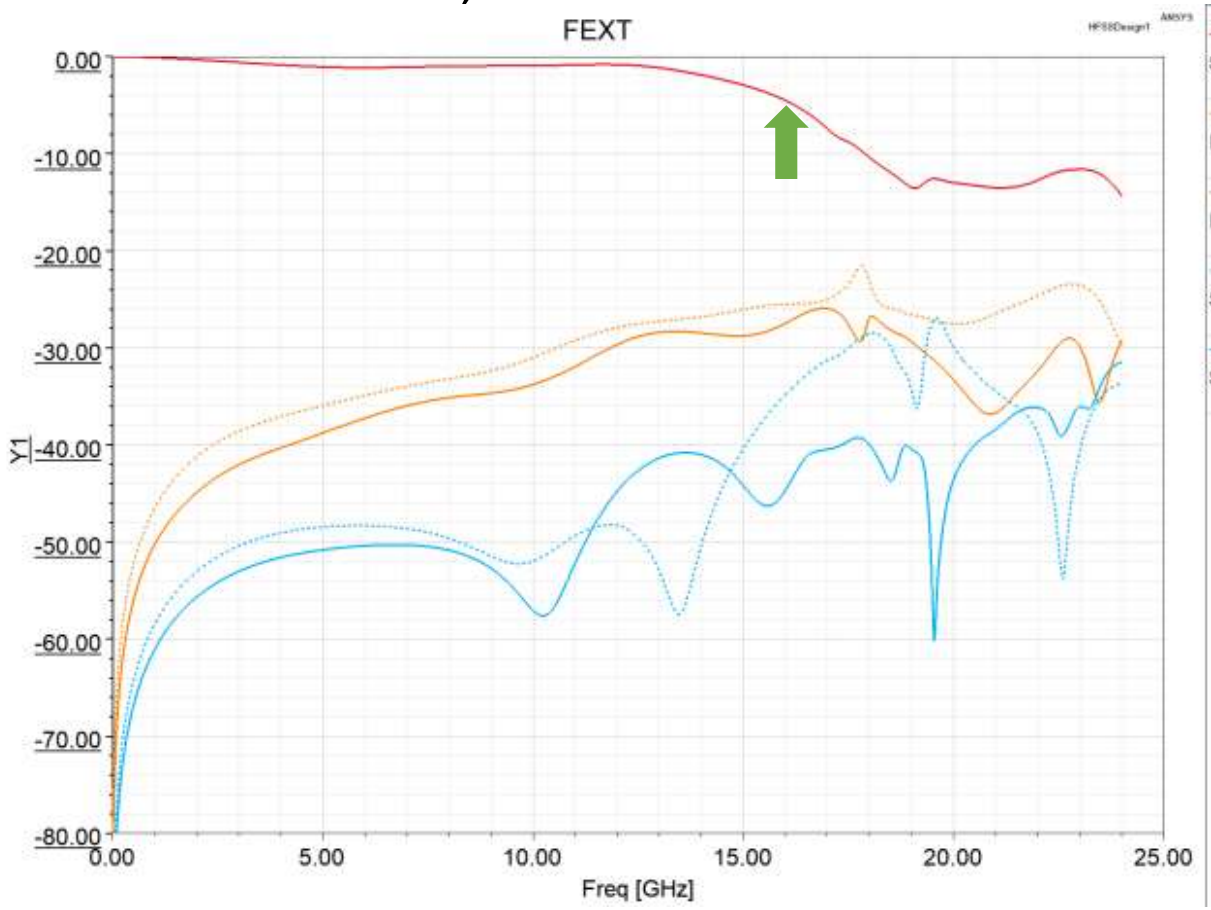


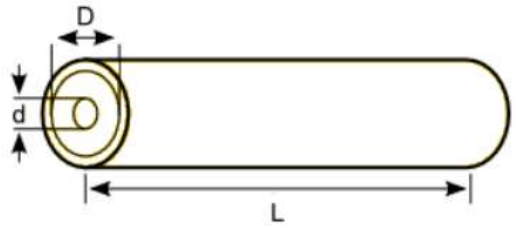
- This case adds staggering and 4 additional grounds between in row signals.

A Case For 24G-SDI

Let's look at the cut off frequency for the HD BNC and it's VIA transition.

- HDBNC Cut off = ~ 42GHz
- Via Field ~16 GHz, **Fr408

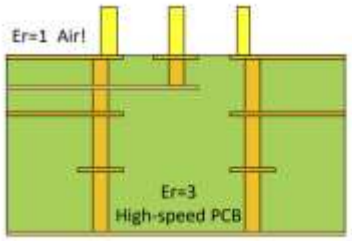




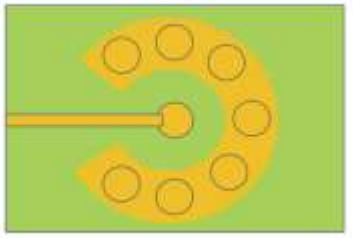
$$f_{cutoff} = \frac{c}{\pi\left(\frac{D+d}{2}\right)\sqrt{\varepsilon_r}}$$

Vertical Launches

- This could be the cross-section of any kind of vertical launch
  - Coax
  - GSG pins
- Often it's desirable to manage the step transition by keeping the ground continuous
  - "D" on coax, pitch on GSG
- The connector designer has an interest in making "D" large, to maximize "d" and reduce loss, make it easier to build, etc
- However, for a coax design, if you're near cutoff in air, the frequency will drop by 1/sqrt(3) (42%!) once the signal hits the board dielectric



$$f_c \propto \frac{1}{\sqrt{\varepsilon_r}}$$



Summary

1. Common design impairments and their resolution.
2. How to improve crosstalk in 12G-SDI systems whilst meeting RL requirements.
3. How single ended systems are crosstalk prone and what's needed to mitigate this deficiency.

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