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# Impacts of Solder Reflow on High Bandwidth RF Connectors

Michael Griesi and Chris Shelly

# Everything's Great Until You Apply Solder!



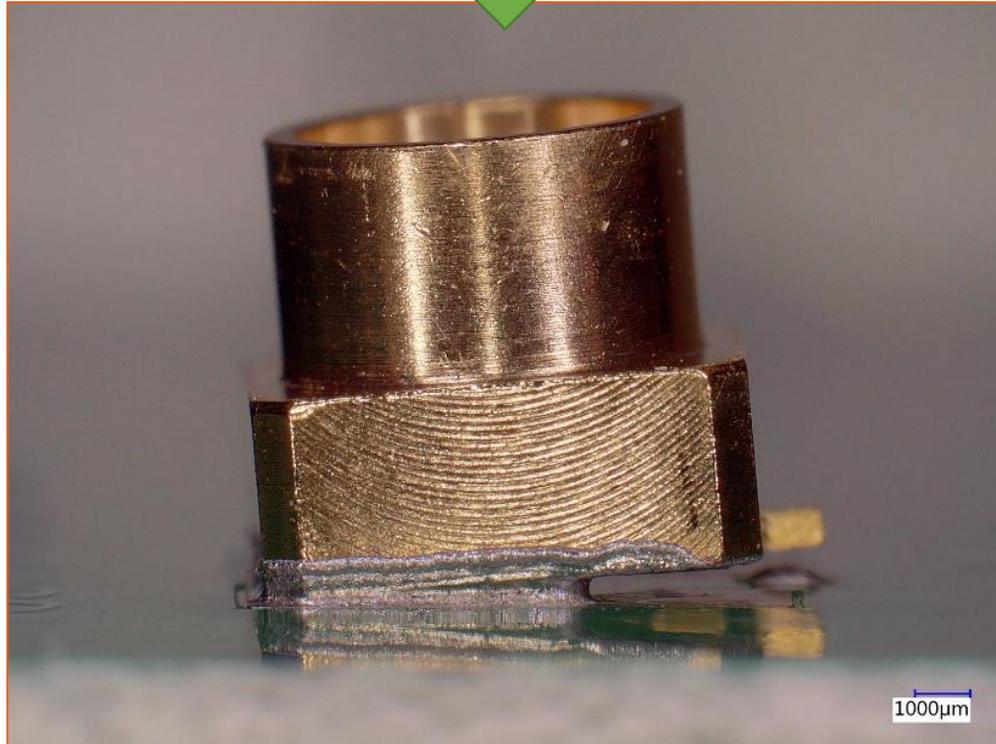
**IDEAL**



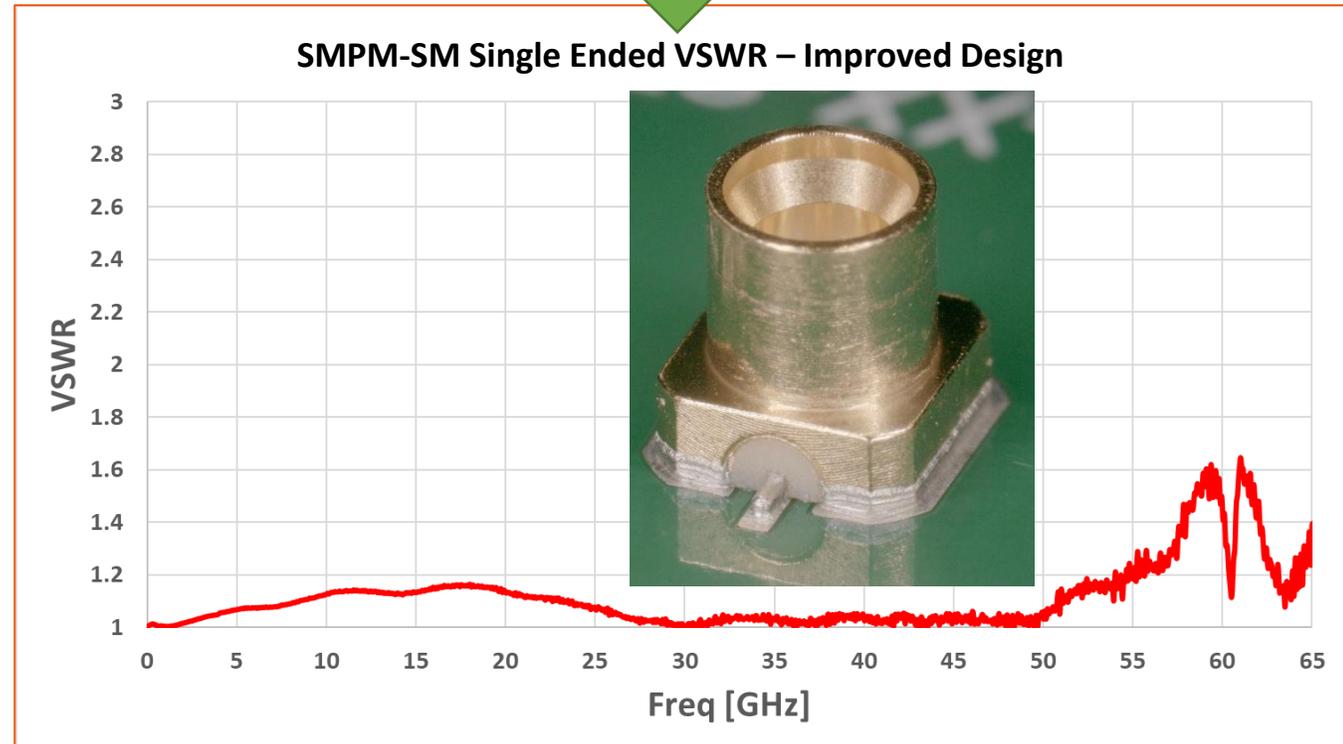
**REAL**

# Everything's Great Until You Apply Solder!

Getting from this



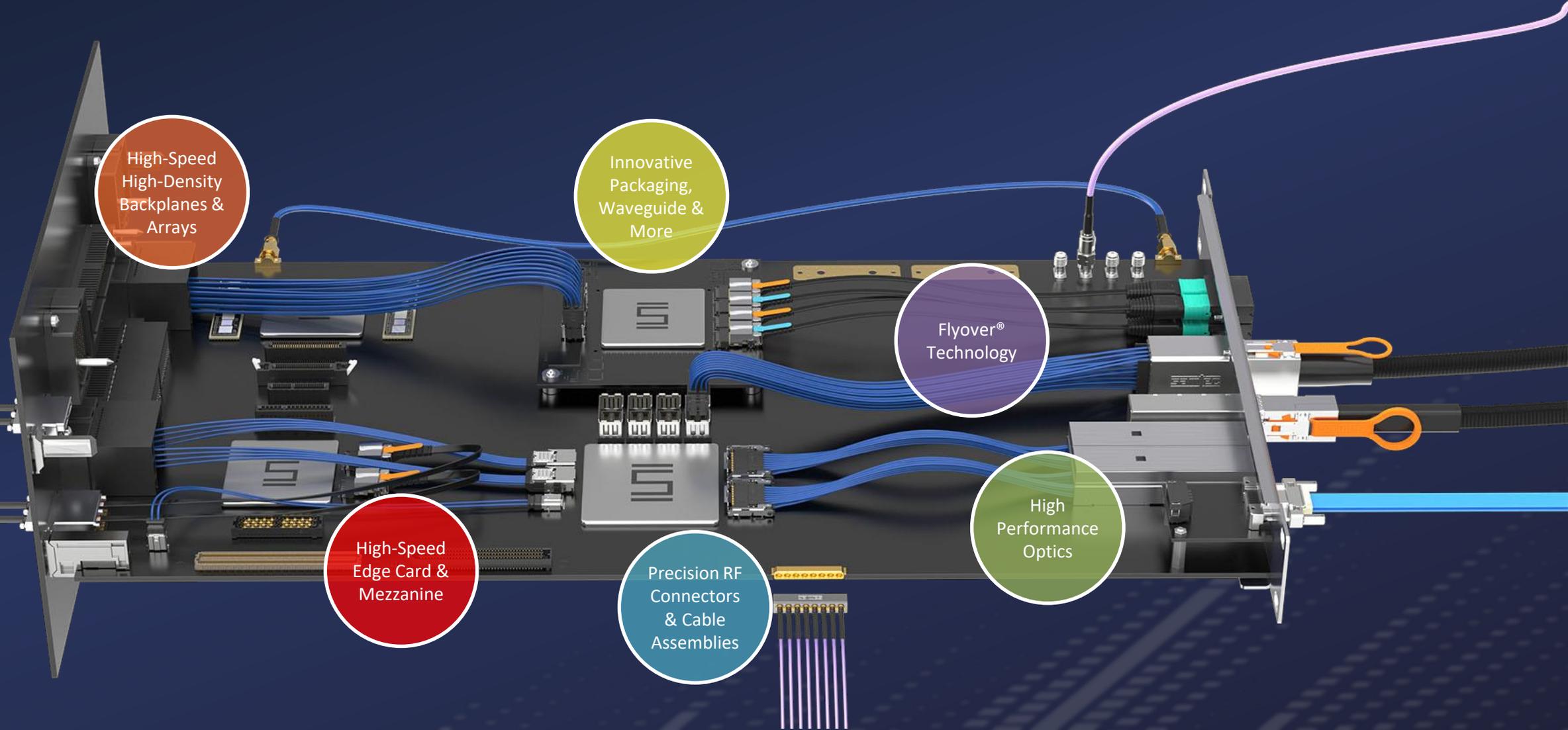
To this





# CURRENT & NEXT GEN CONNECTIVITY

## BOARD-TO-BOARD | SILICON-TO-SILICON



High-Speed  
High-Density  
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Innovative  
Packaging,  
Waveguide &  
More

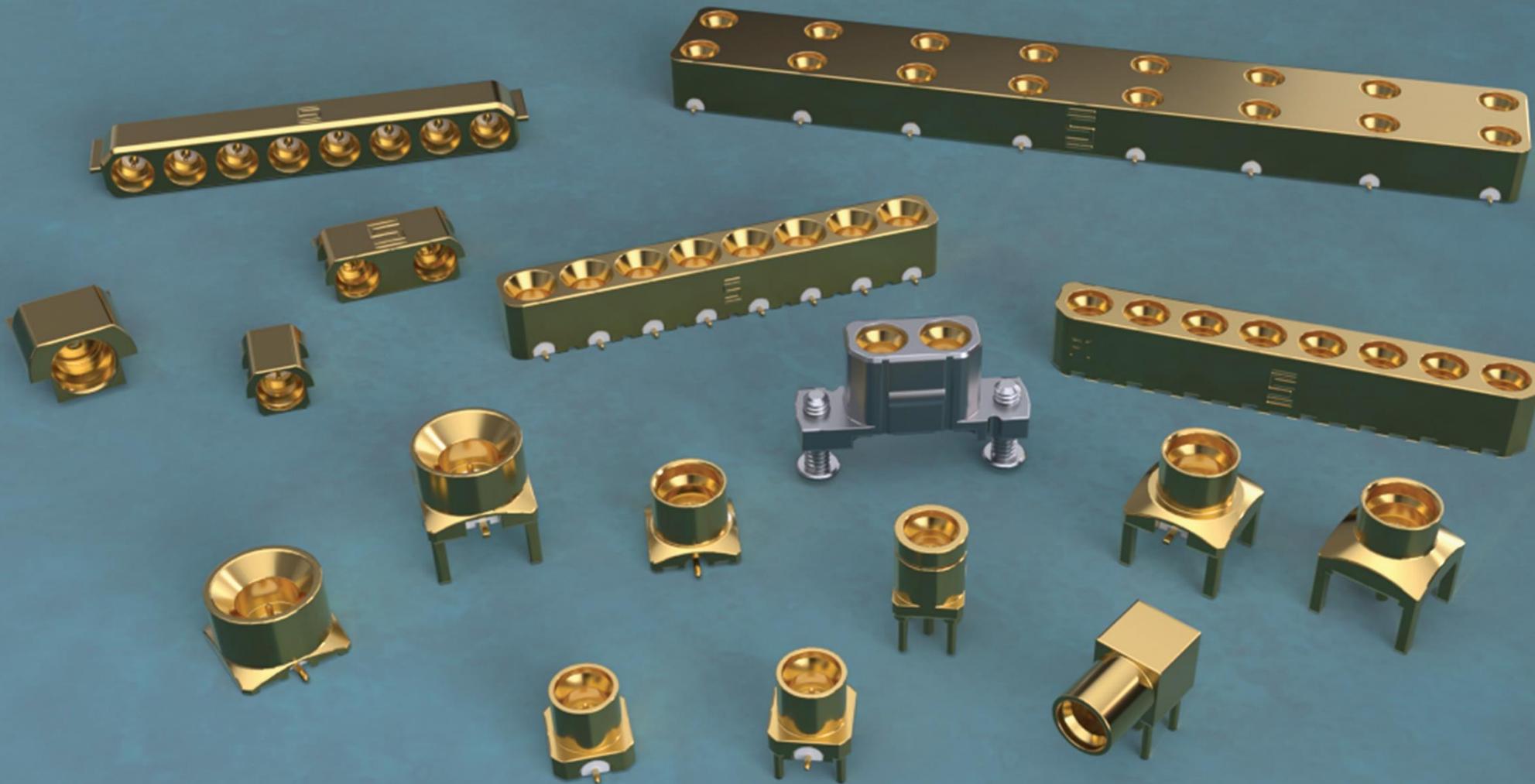
Flyover®  
Technology

High-Speed  
Edge Card &  
Mezzanine

Precision RF  
Connectors  
& Cable  
Assemblies

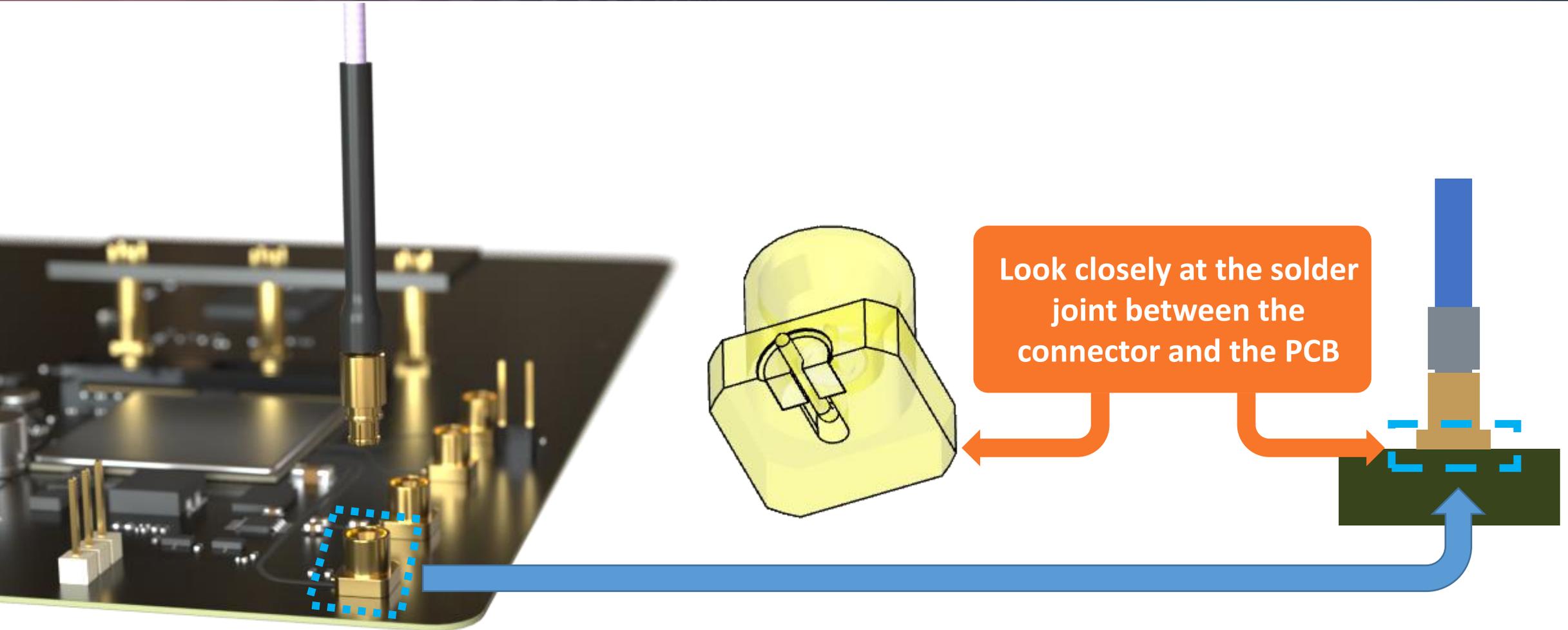
High  
Performance  
Optics

# PRECISION RF | Push-on Connectors



For more information visit [www.samtec.com/precisionrf](http://www.samtec.com/precisionrf)

# Focus on SMPM Surface Mount

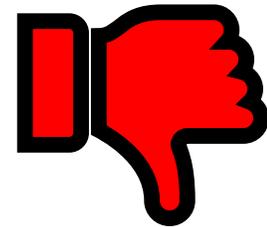
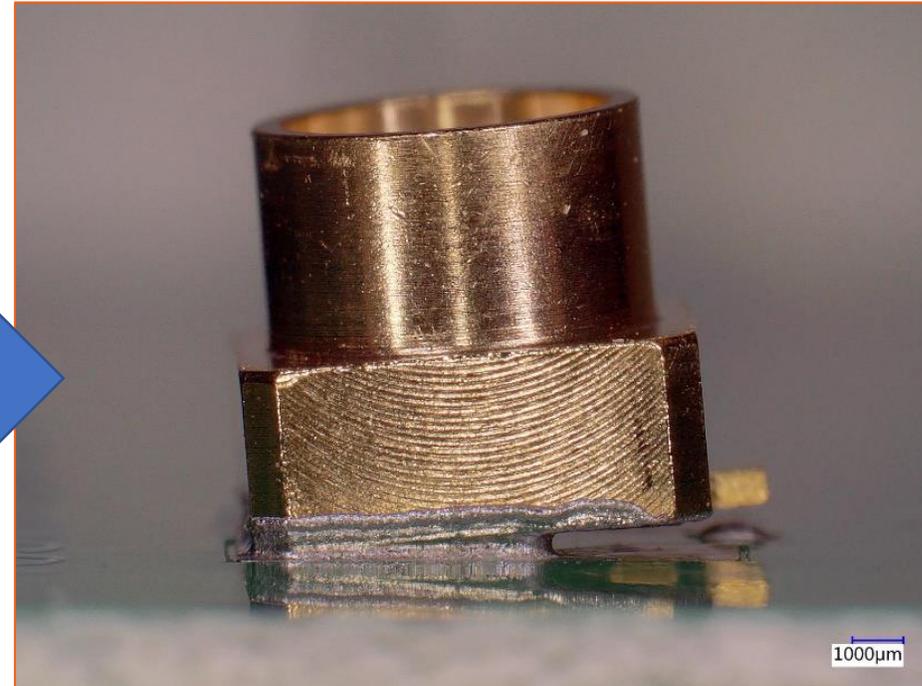
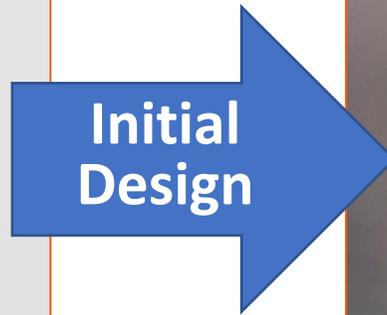
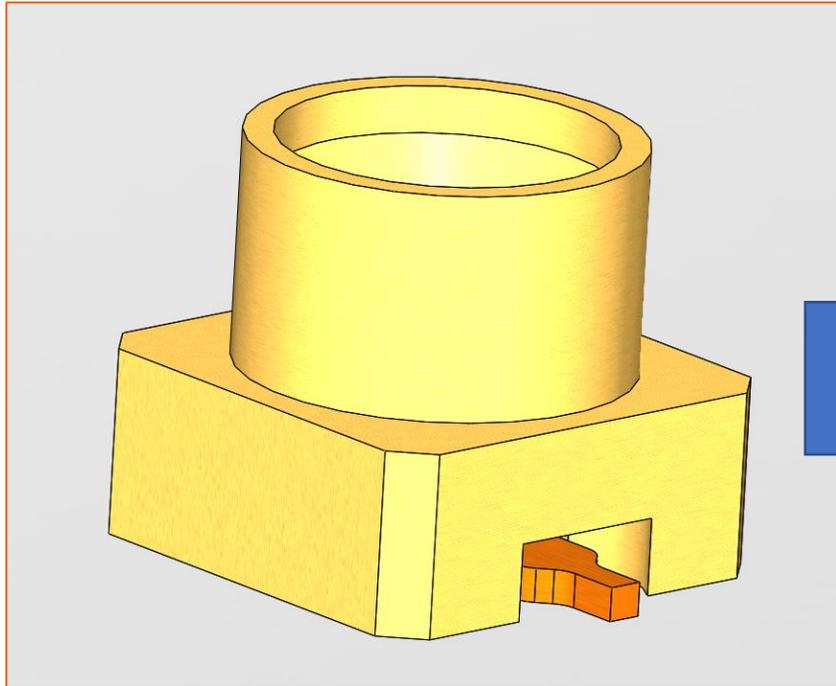


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# SMPM-SM INITIAL DESIGN

# Initial Trials



## Initial Design

### Design Targets:

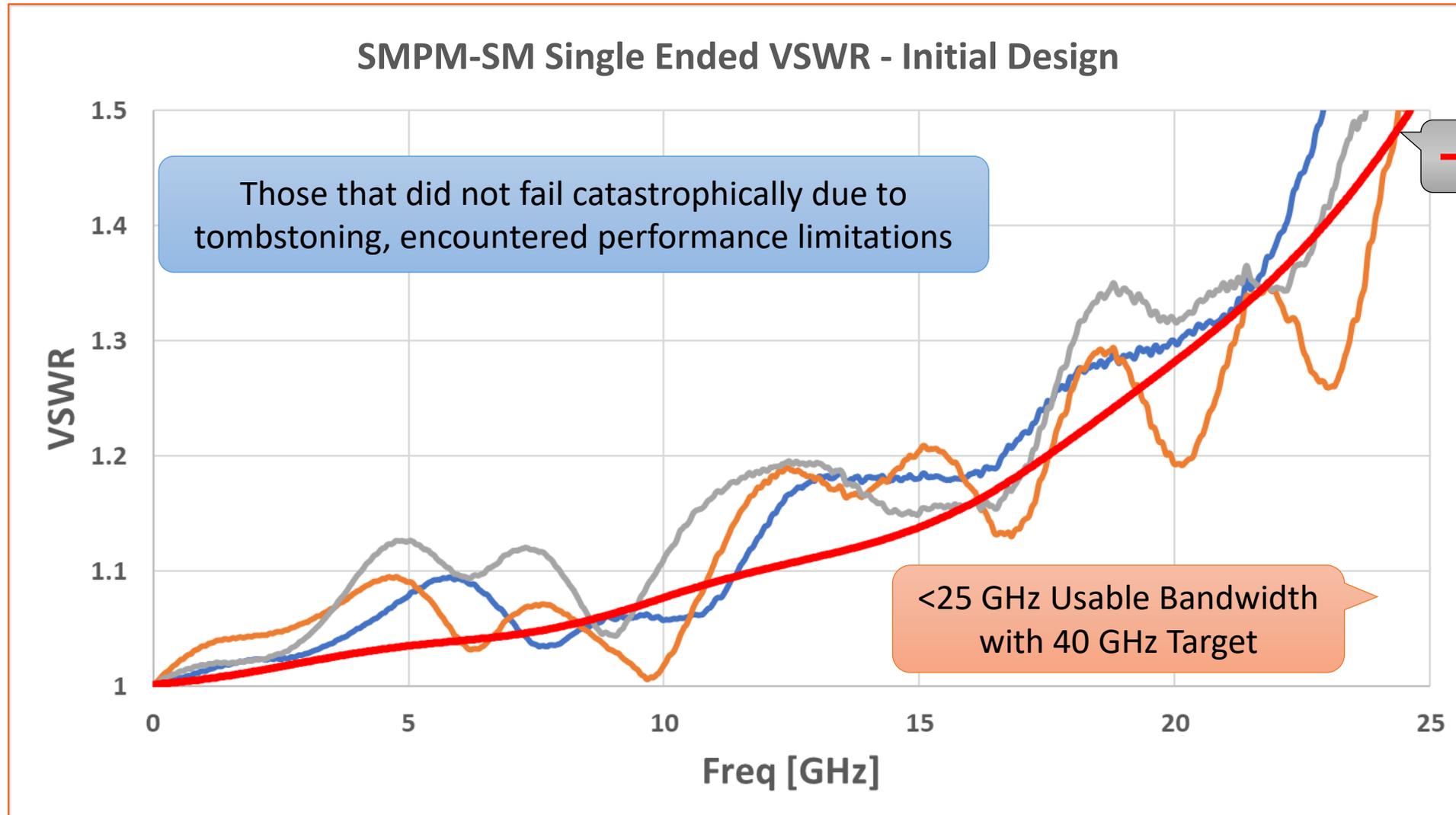
- Desired 40 GHz Bandwidth
- Simulation showed <25 GHz

## "Tombstoning"

### Probable Causes:

- Thick Gold Plating
- Insulator TCE (Thermal Expansion)
- Center contact barb mechanical stress

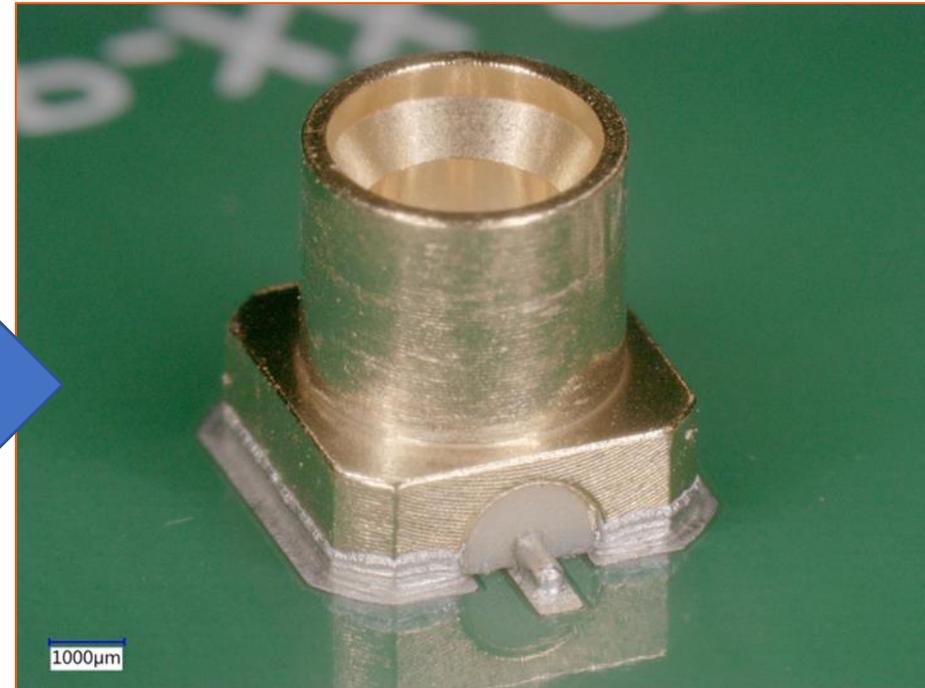
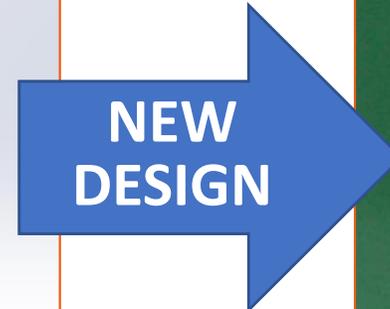
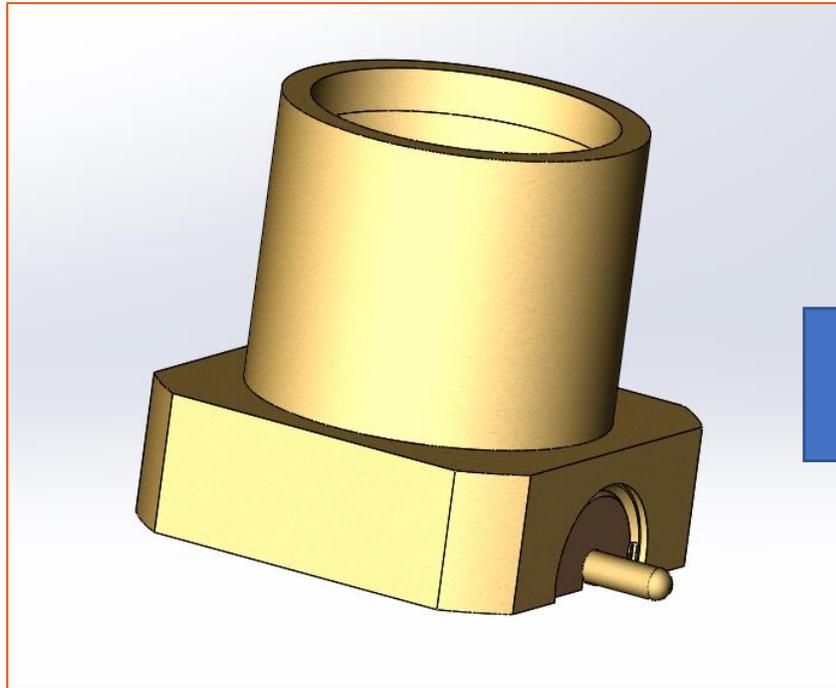
# Initial Trials





# SMPM-SM-1 NEW DESIGN

# New Design Looked Much Better Visually



## New Design

### Notable Changes:

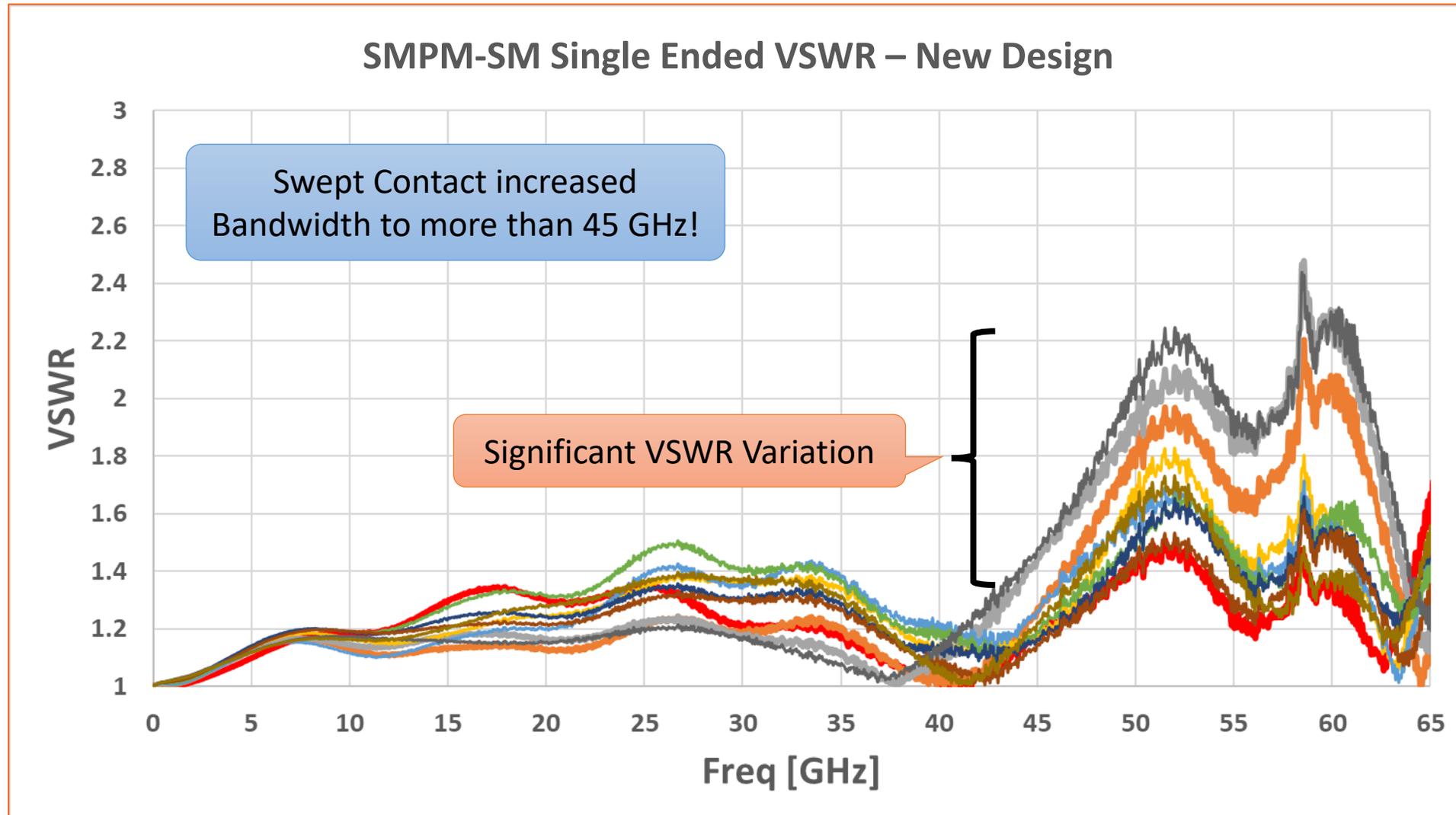
- Thinner gold plating
- Higher Temp Insulators
- Swept Contact

## No More "Tombstoning"

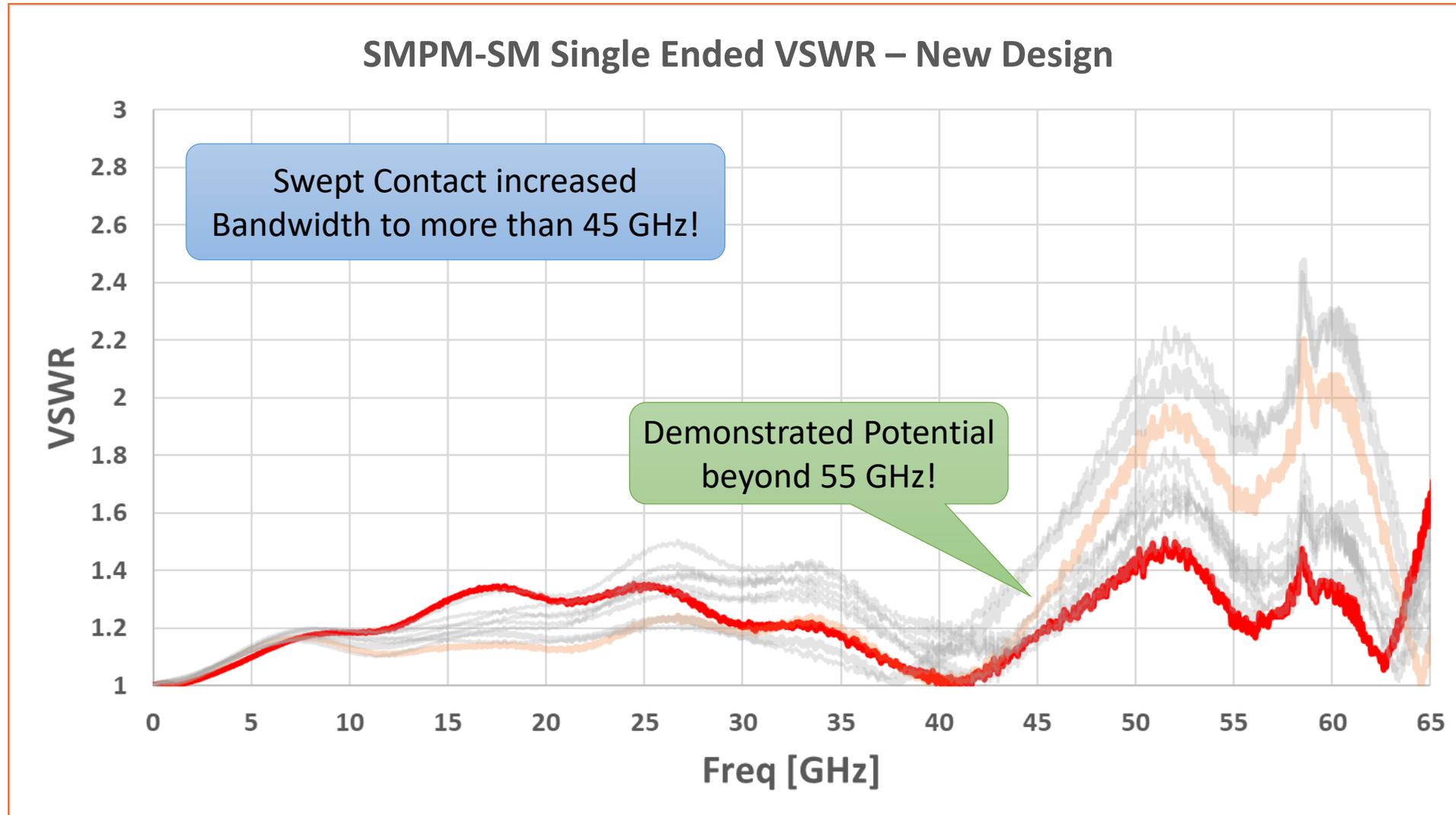
### Notable Improvements:

- Solder **"Looks"** Good

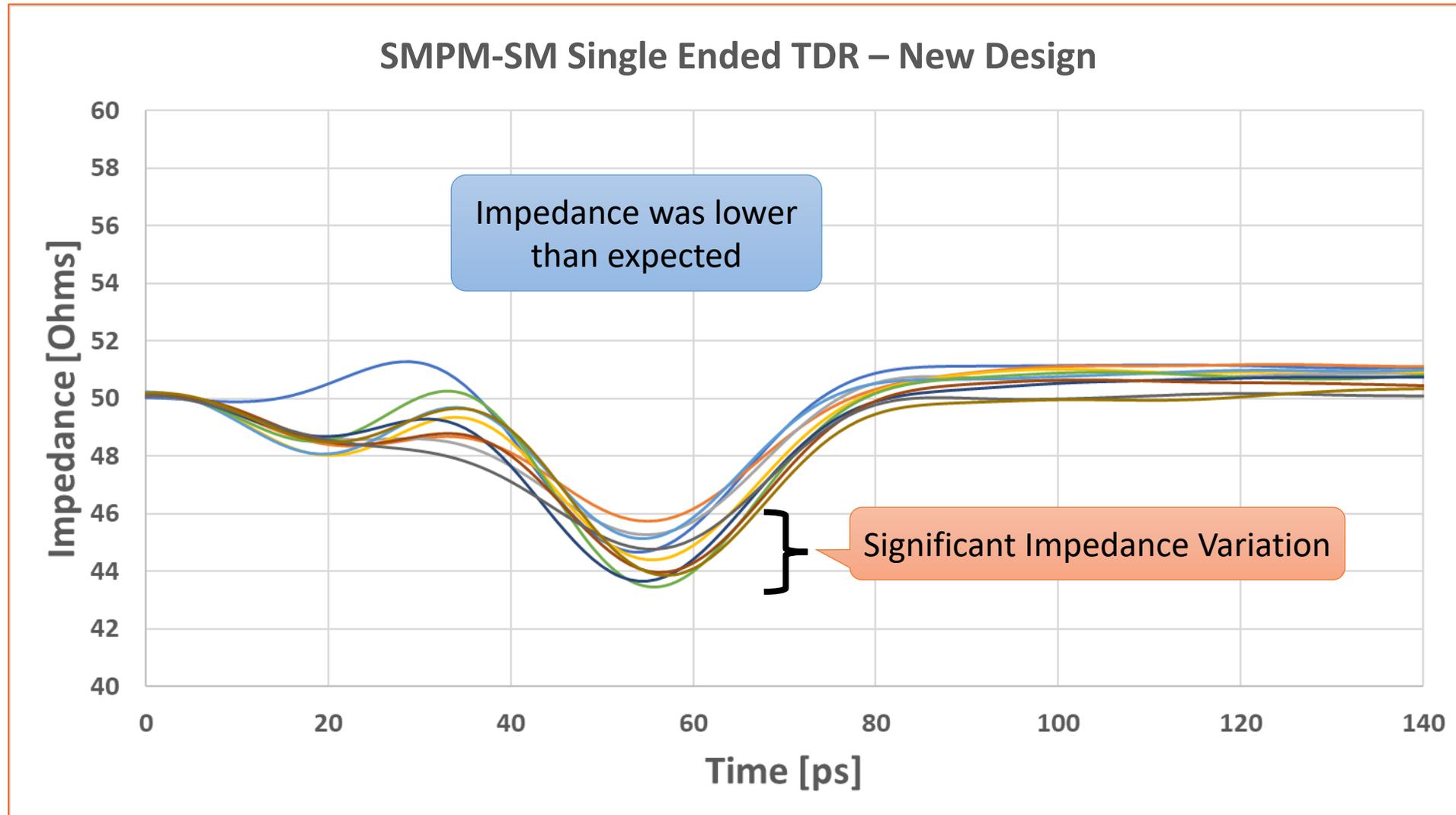
# New Design VSWR Showed Variation



# New Design VSWR Showed Potential



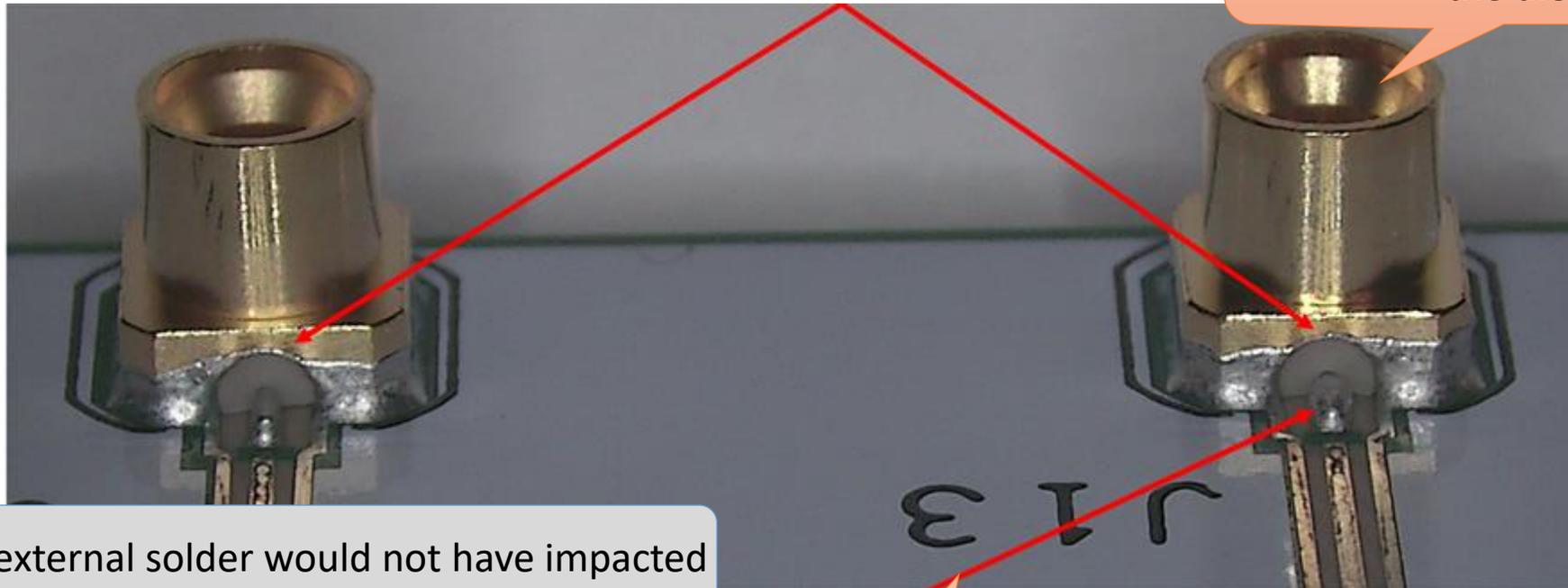
# Variation with Impedance





# THE HUNT FOR VARIATION

# Visible External Solder Wicking



Some of the samples had significant wicking up the body and around the dielectric

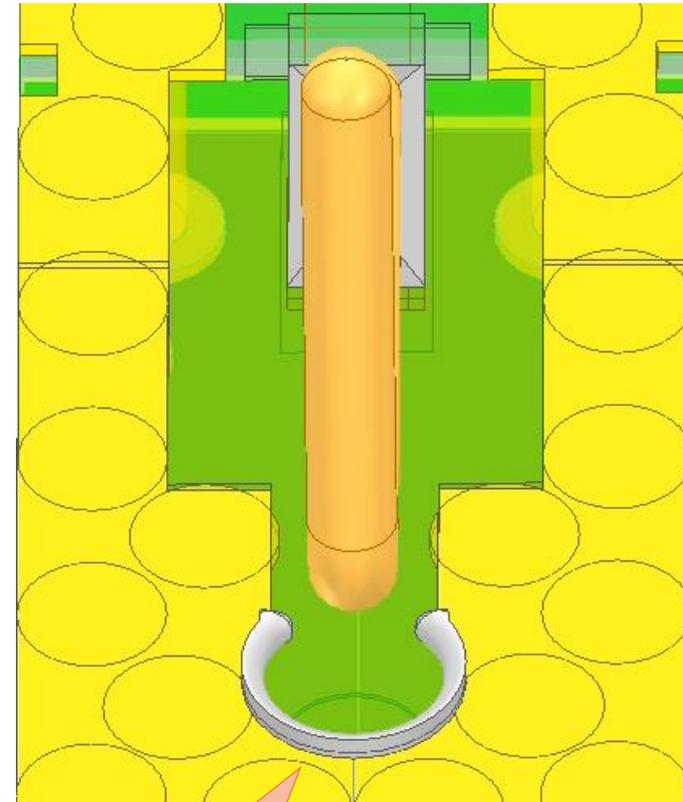
While the external solder would not have impacted the internal impedance... Wicking was significant enough to suggest solder might also be wicking under the connector which would not be visible

There was also excessive solder on the connector pin

# Hidden Solder Pooling Under the Connector

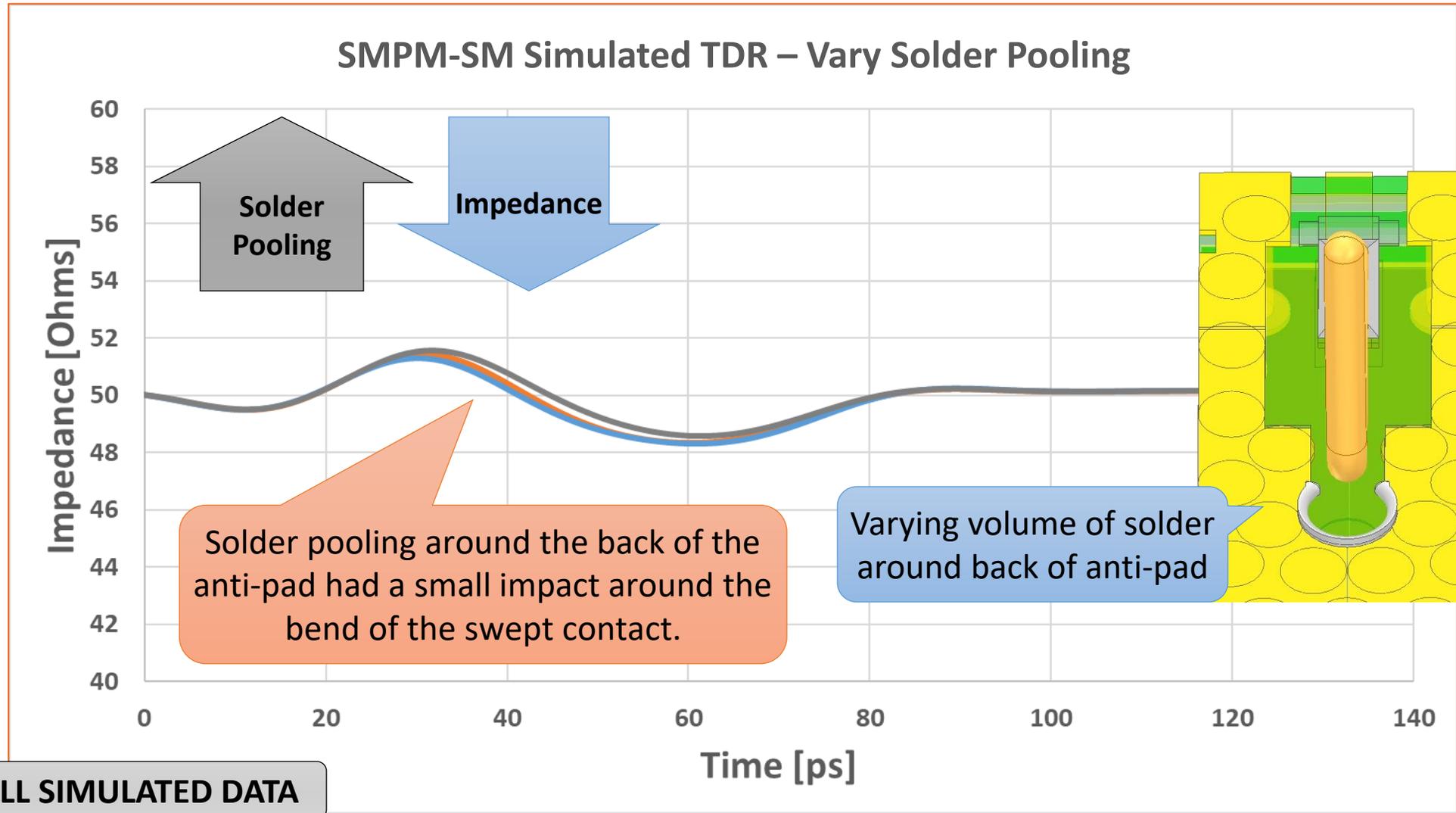


Sure enough, solder was found pooling along the inner edge of the connector at the pad

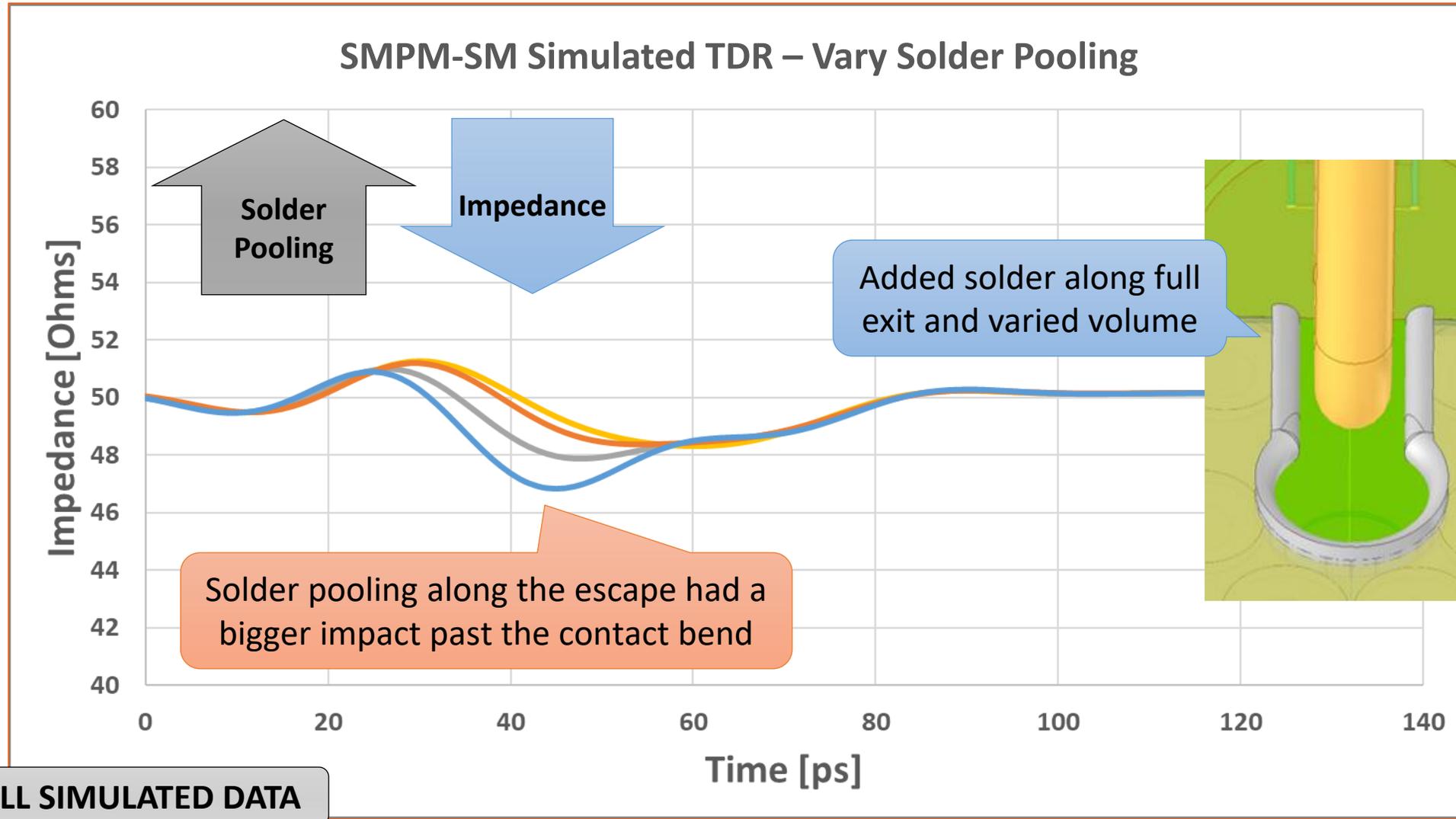


A solder pool was added to the simulation model to assess the potential impact

# Impedance Variation from Solder Pooling

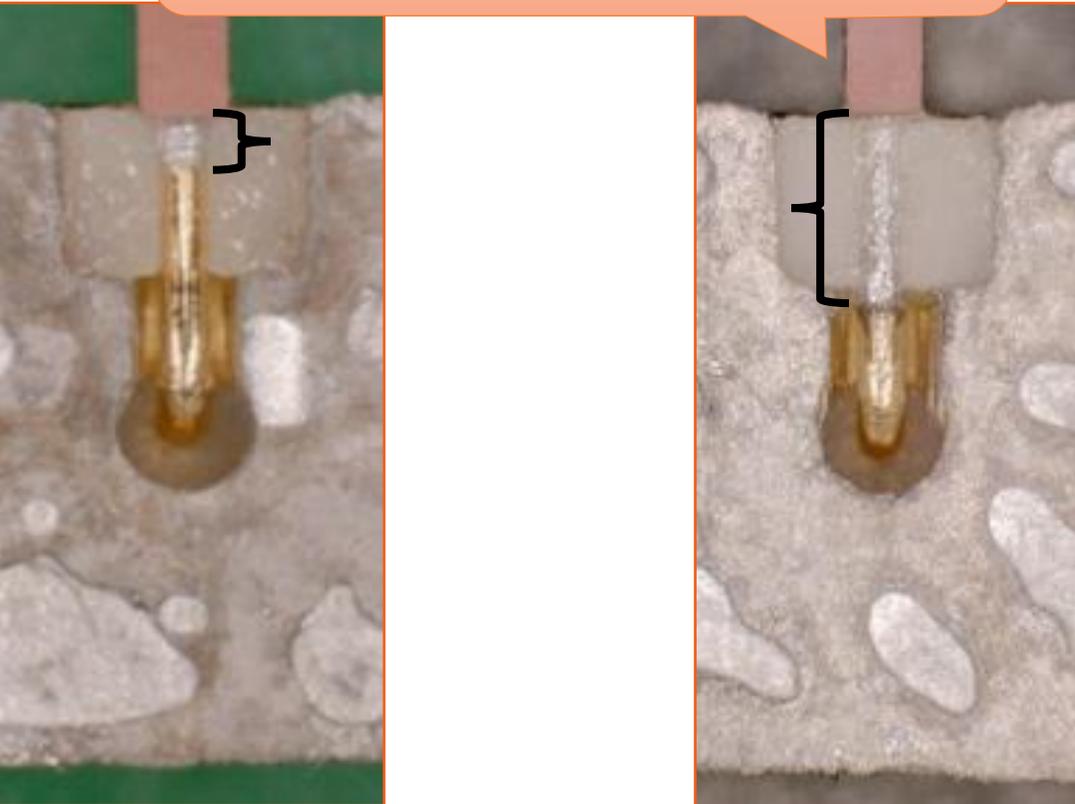


# Impedance Variation from Solder Pooling

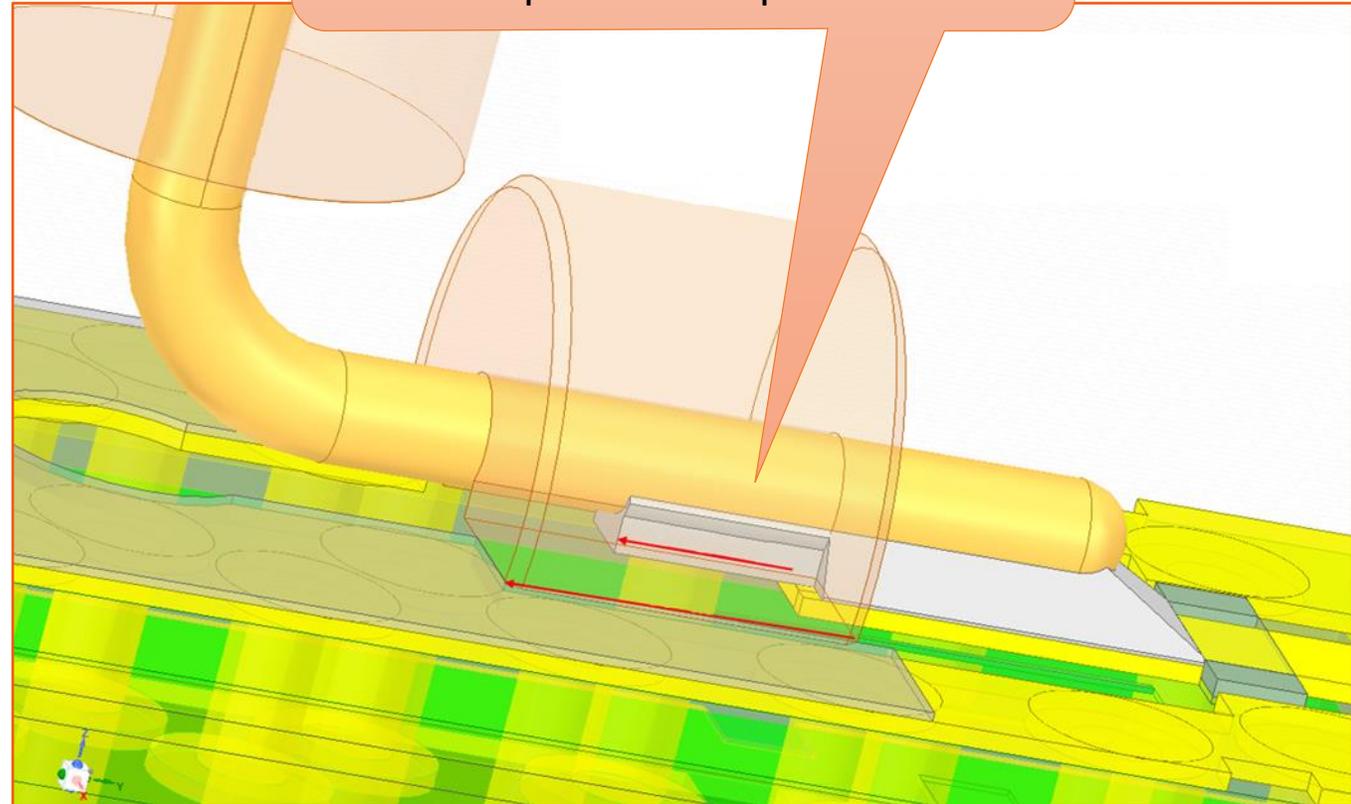


# Hidden Solder Wicking Up the Connector Pin

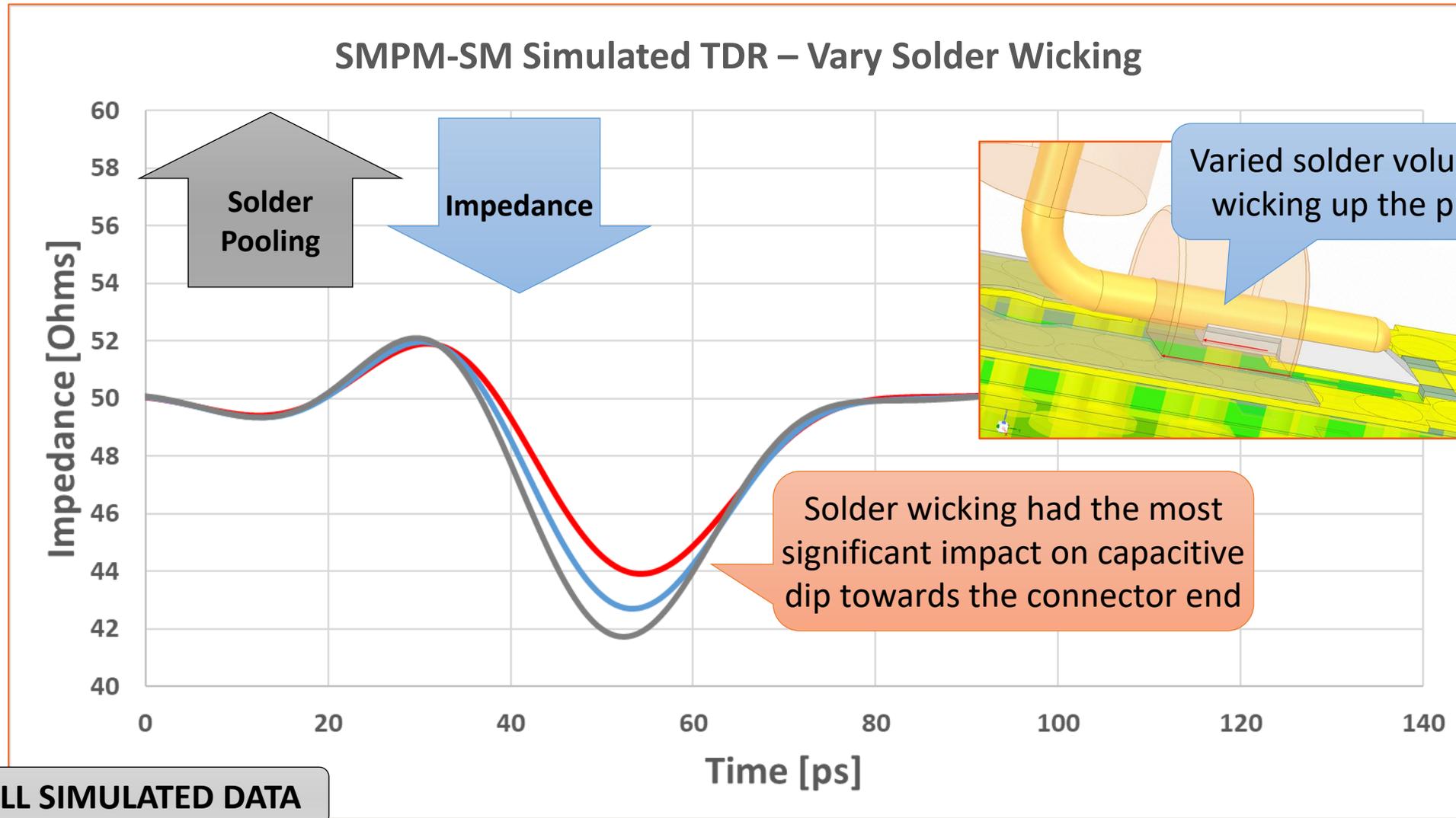
Solder was found wicking up the contact, under the insulator, with significant variation across samples



Solder wicking added to the simulation model and varied to assess the potential impact

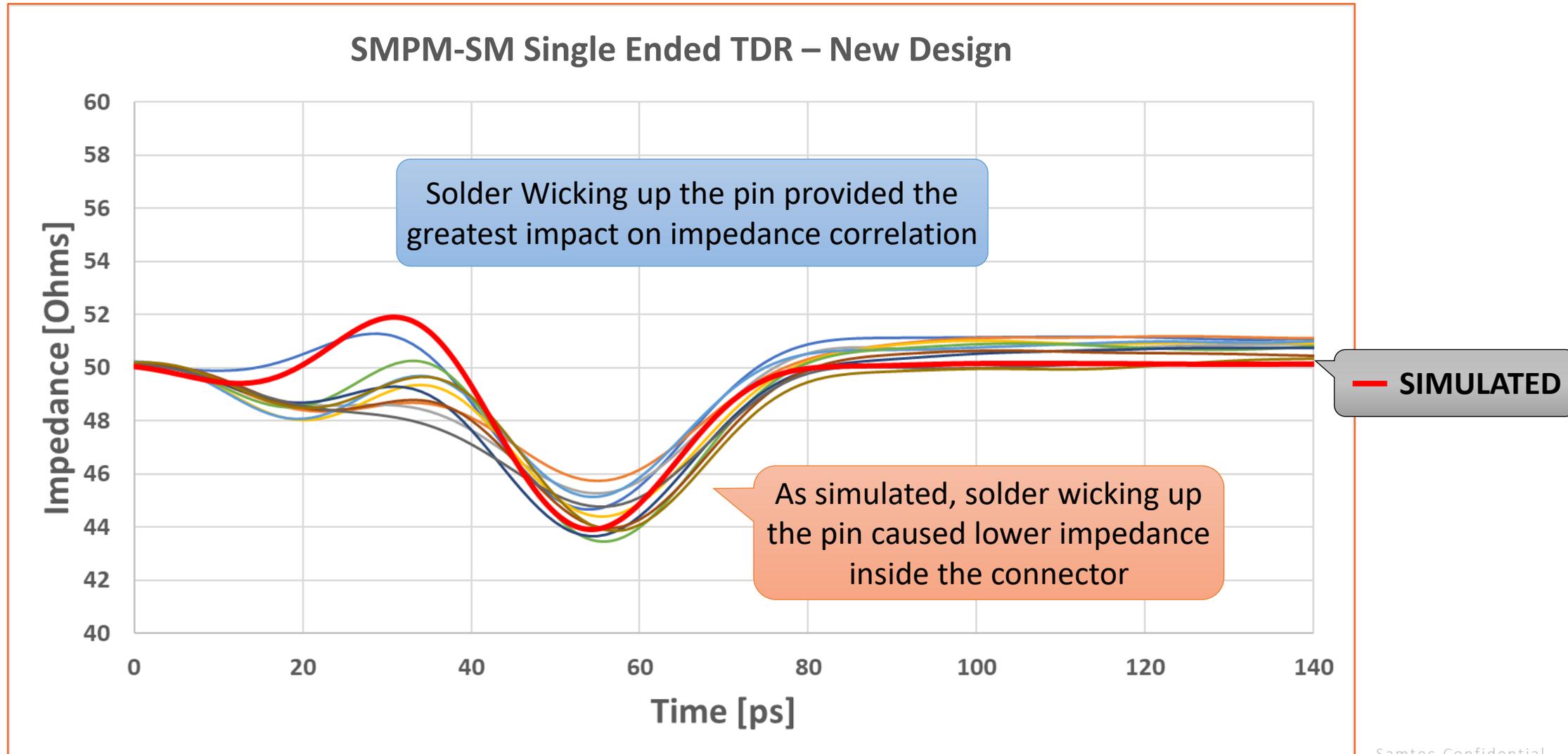


# Impedance Variation from Solder Wicking

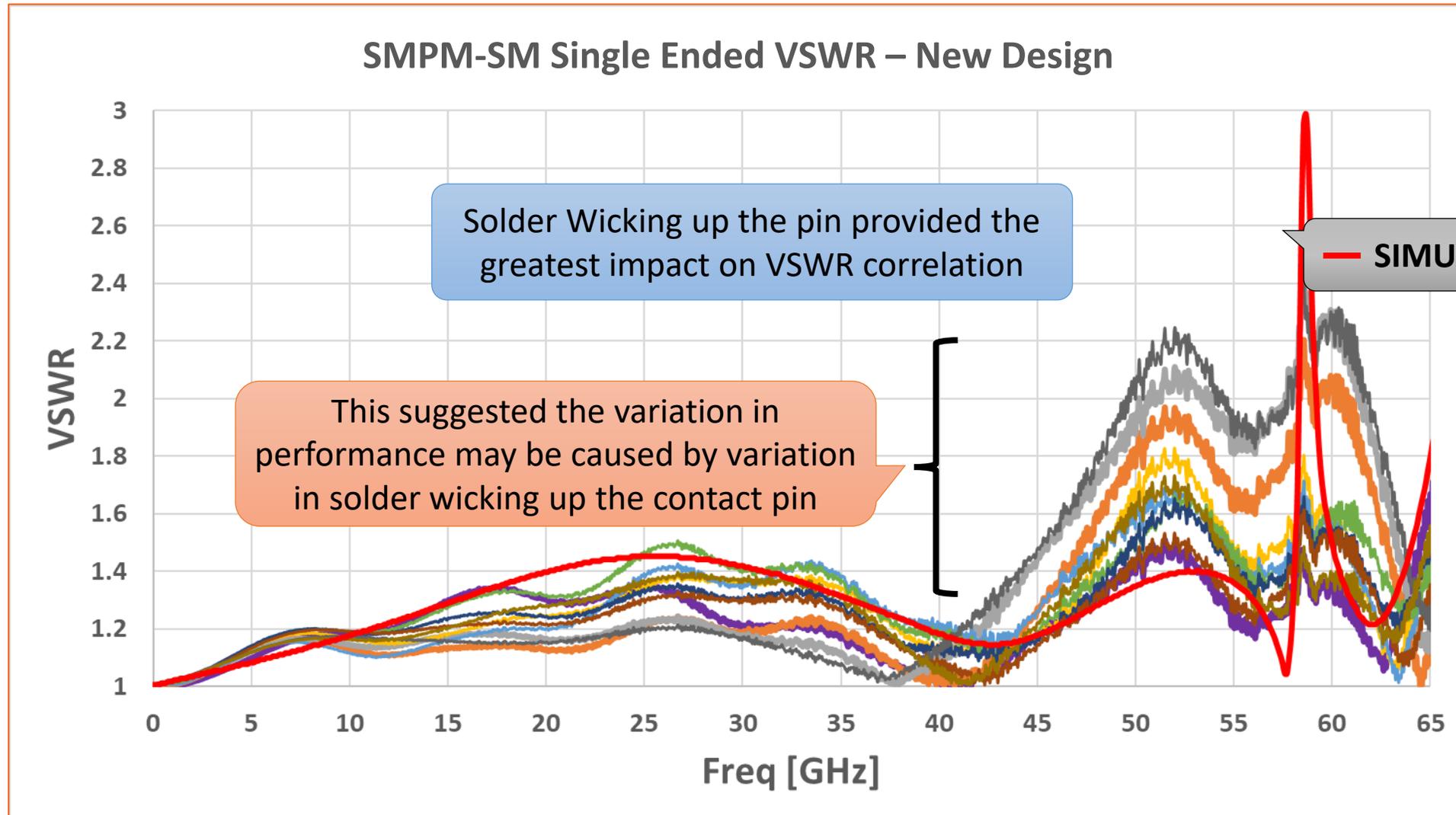


ALL SIMULATED DATA

# Simulation Model Correlation



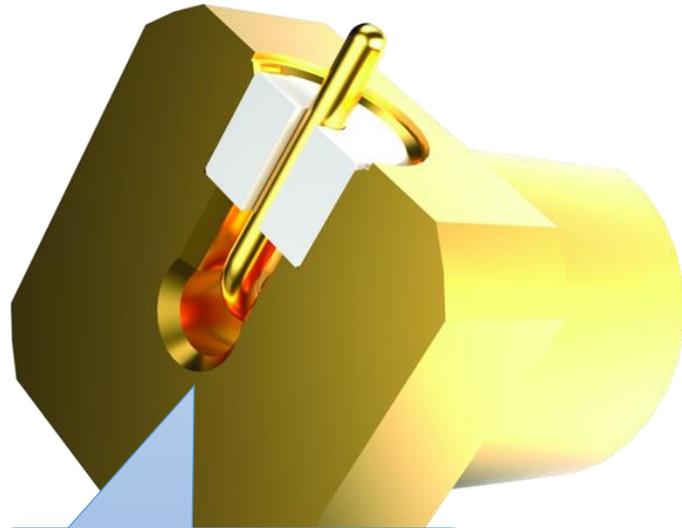
# New Design VSWR Showed Variation





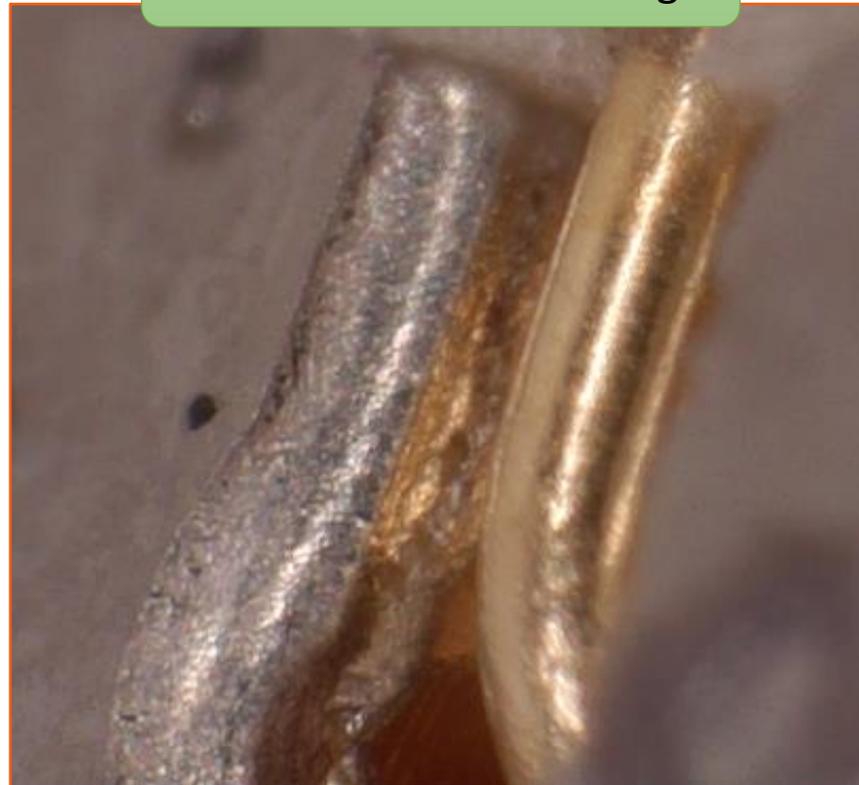
# MINIMIZING VARIATION

# Mitigating Solder Pooling



Added Chamfer to Connector Edge to Minimize Solder Pooling

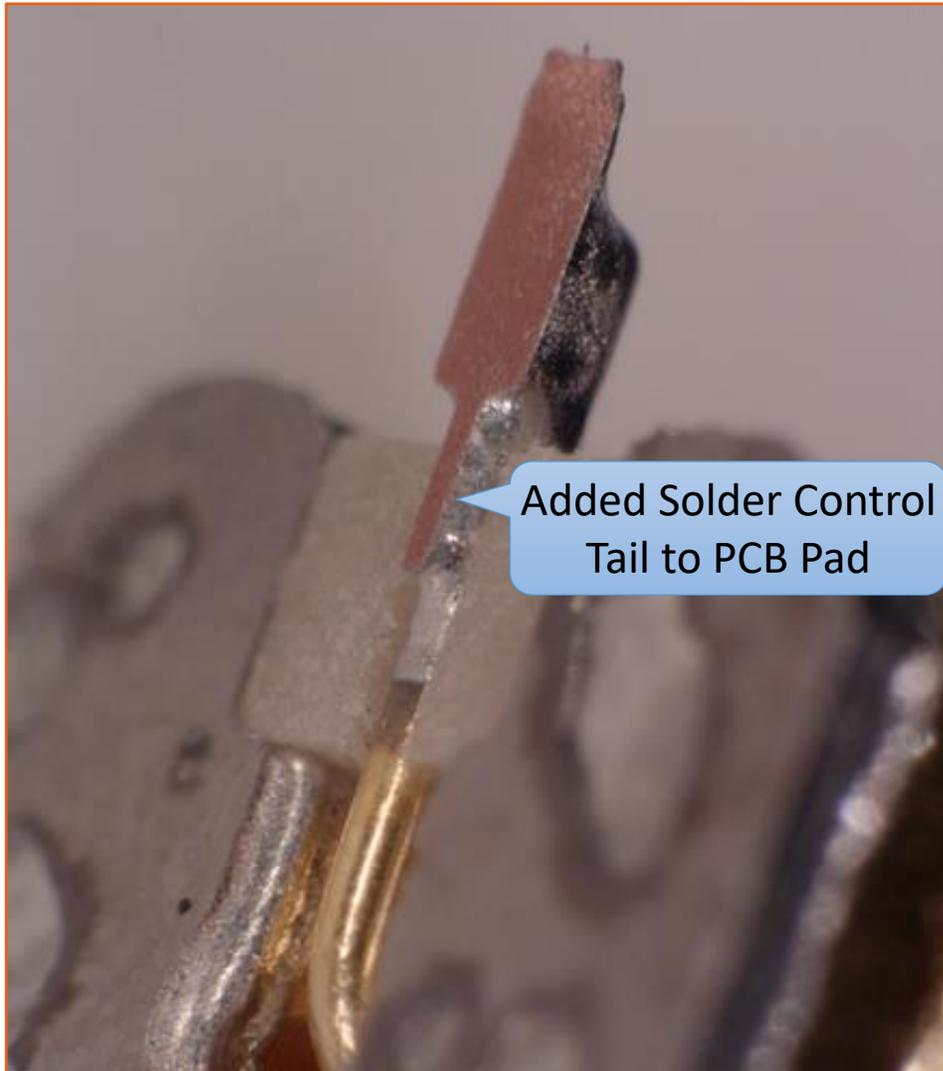
Connector Chamfer  
Minimized Solder Pooling!



Chamfer provided a space for the solder without impacting SI

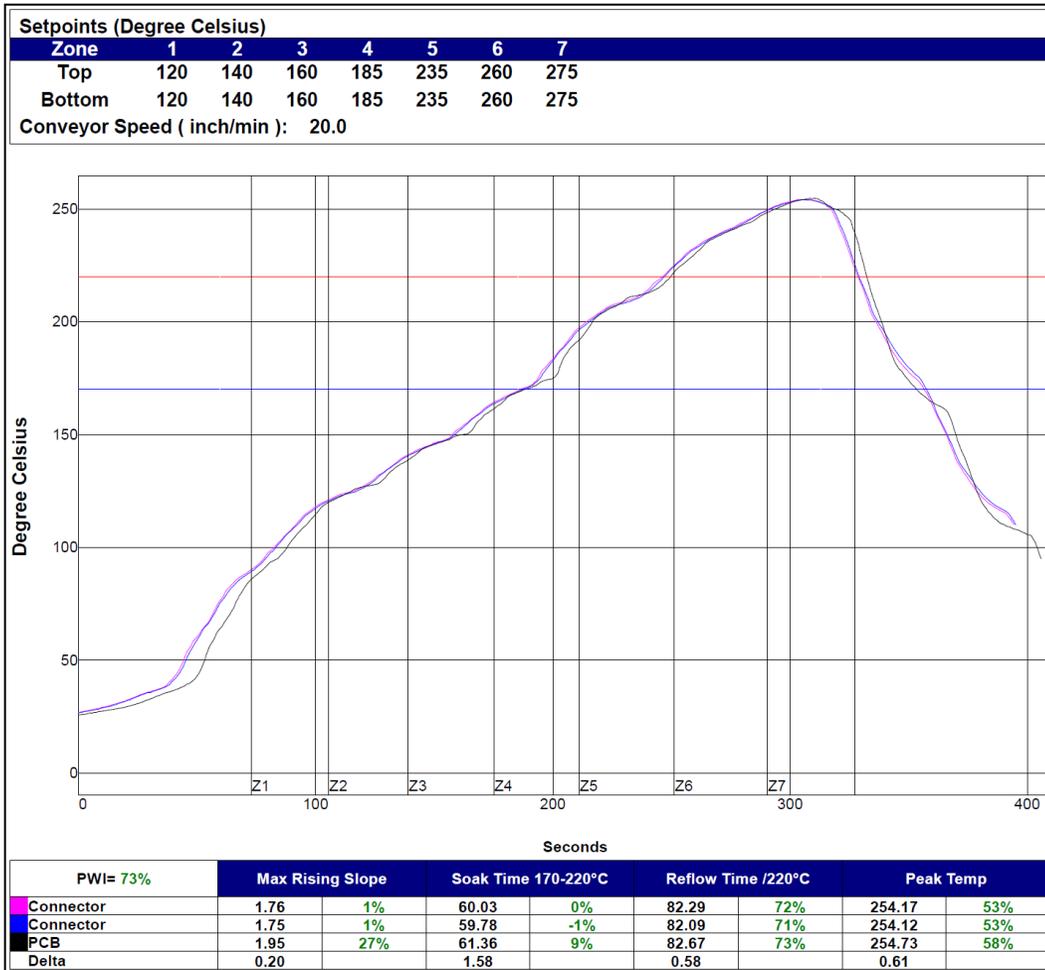


# Controlling Solder Wicking



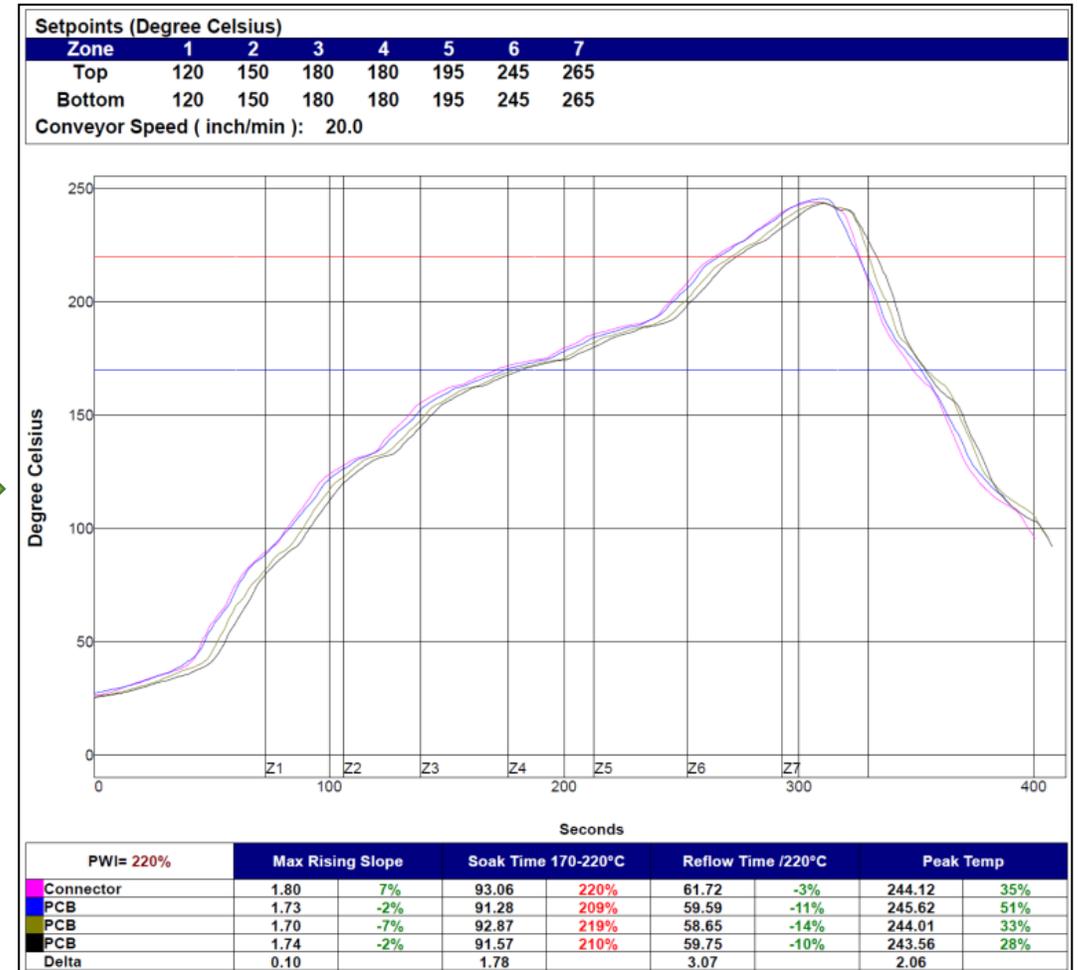
# Reflow Thermal Profile

## AGGRESSIVE THERMAL PROFILE



Peak Connector Temperature: **254°C** | Reflow Time: **82s**

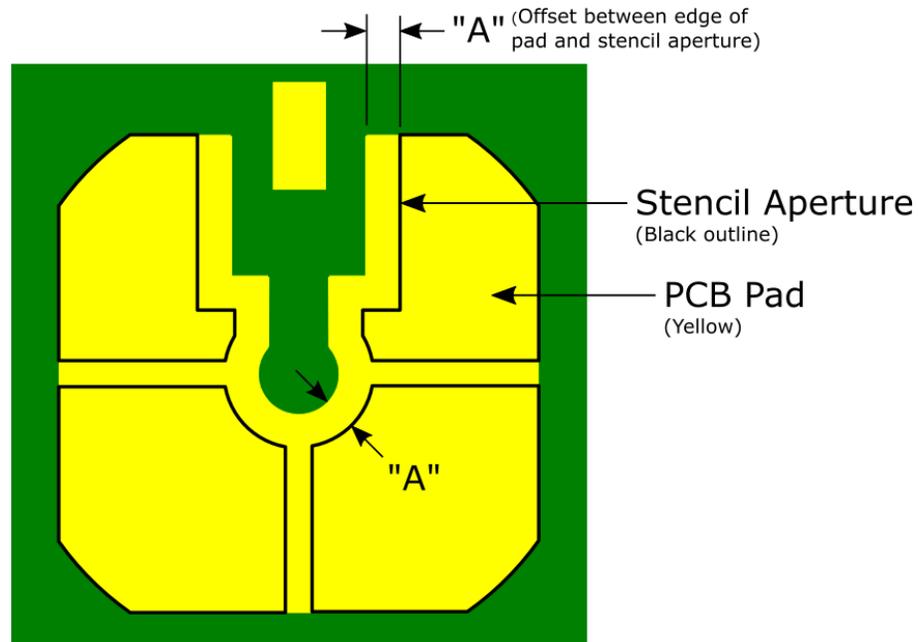
## MODERATE THERMAL PROFILE



Peak Connector Temperature: **244°C** | Reflow Time: **62s**

# Reflow Process Adjustments

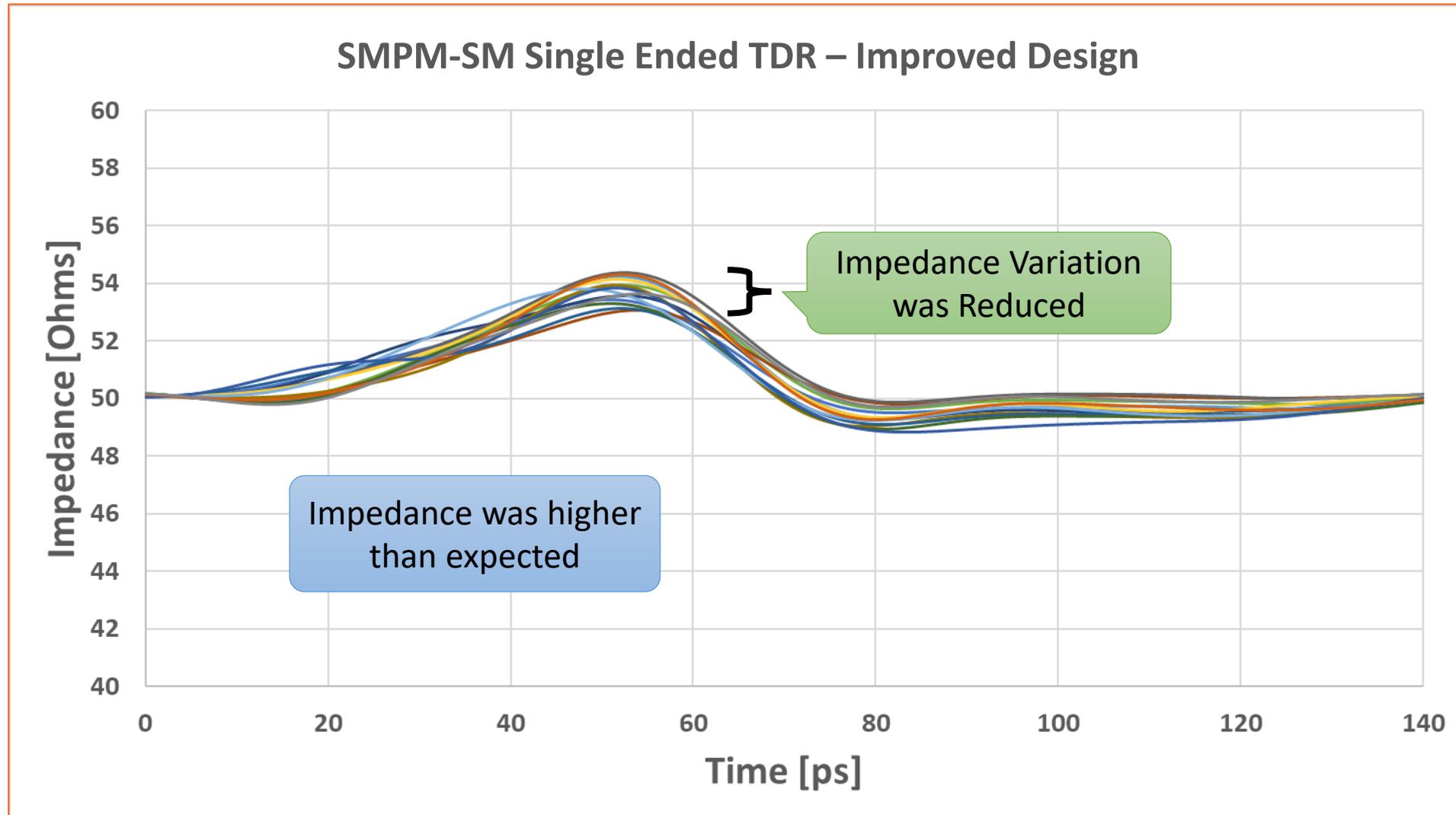
Process Parameter Adjustments			
Solder Paste:	Water-Soluble	→	No-Clean
Reflow Environment:	Nitrogen	→	Air
Stencil Thickness:	.005"	→	.004"
Reflow Profile:	Aggressive	→	Moderate



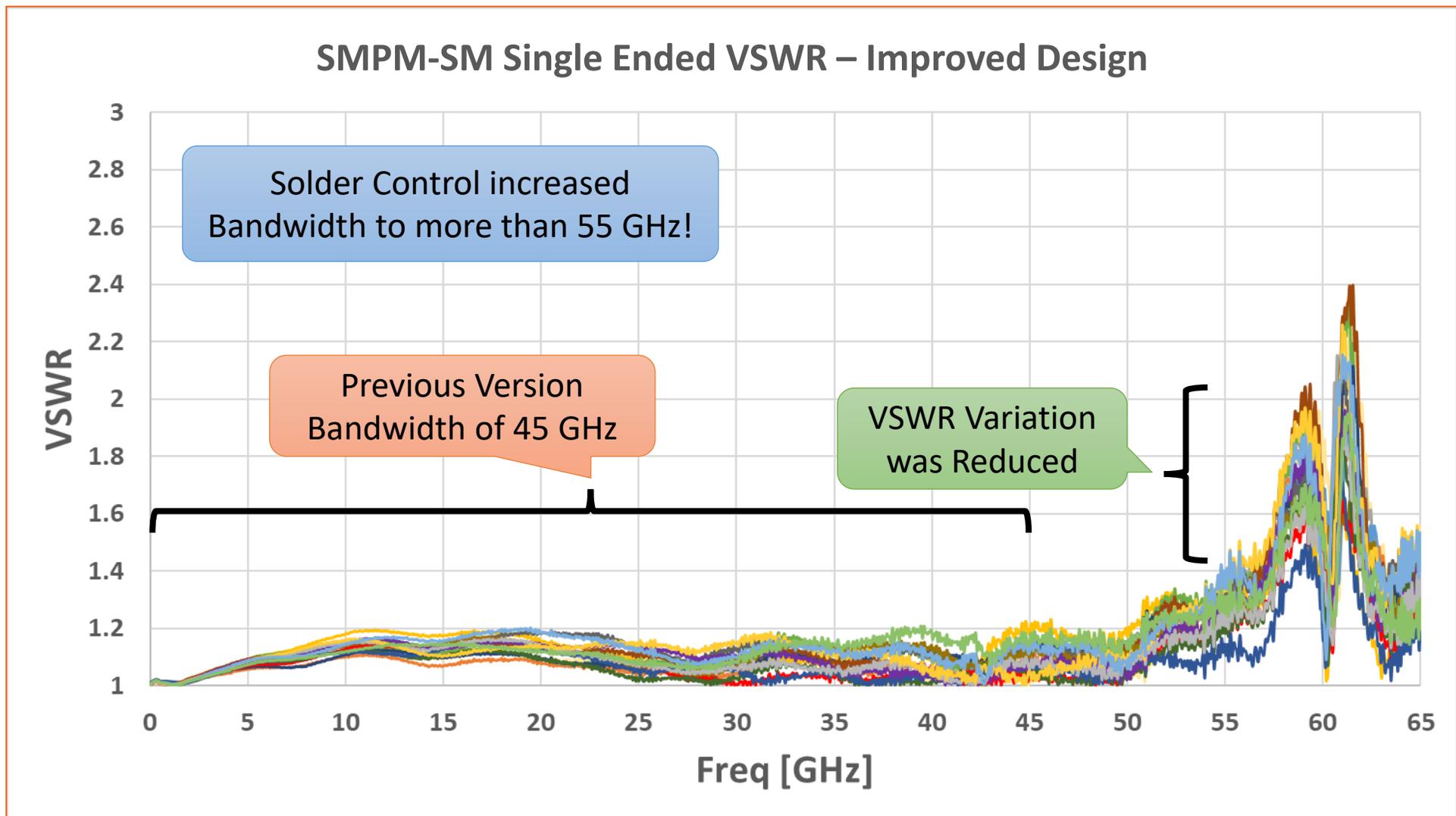
## Stencil Aperture Modifications:

"A" dimension (offset between edge of pad and stencil aperture) was increased in iterations to prevent solder from wicking/migrating into critical regions for SI.

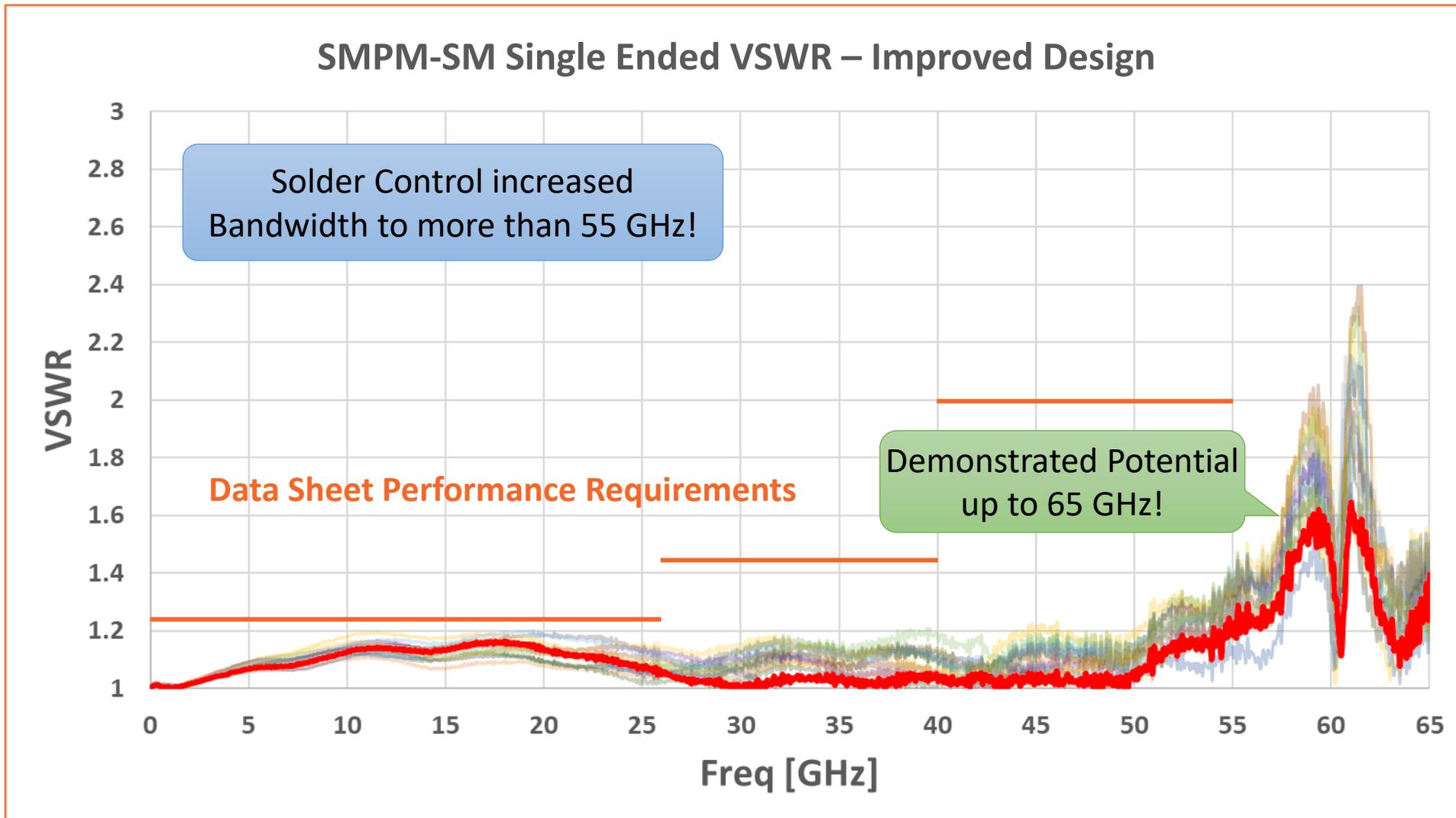
# Improved Design & Process Reduced Zo Variation



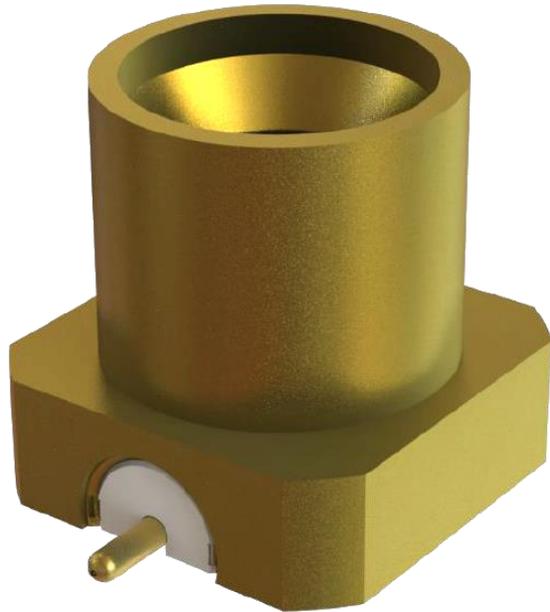
# Improved Design & Process Reduced VSWR Variation



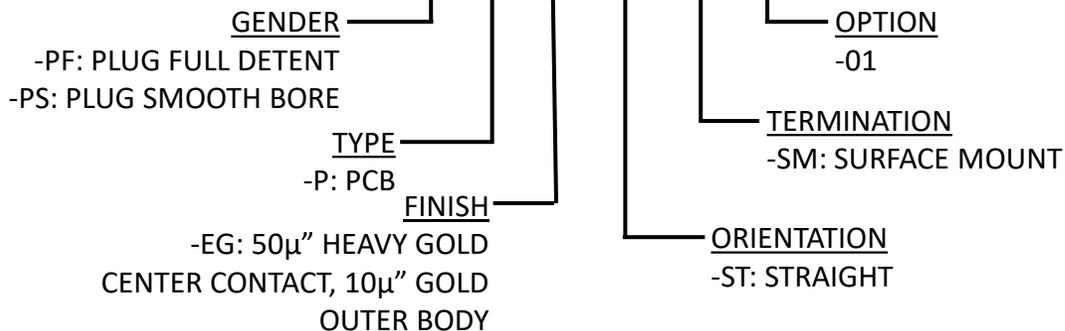
# Improved Design & Process Increased BW Potential



# SMPM-SM-1



## SMPM-XX-P-XX-ST-SM-1



## ELECTRICAL DATA

[www.samtec.com/products/smpm-sm](http://www.samtec.com/products/smpm-sm)

Impedance	50 Ohm
Frequency Range	DC to 55 GHz
VSWR <sup>1</sup>	DC to 26.5 GHz: 1.25:1 Max 26.5 GHz to 40 GHz: 1.45:1 Max 40 GHz to 55 GHz: 2:1 Max
Insertion Loss <sup>2</sup>	0.04 √F (GHz) dB Max
Insulation Resistance	5000 MOhm Min
Voltage Rating (Sea Level) <sup>3</sup>	170 Vrms Max
DWV <sup>3</sup>	325 Vrms Min (sea level)

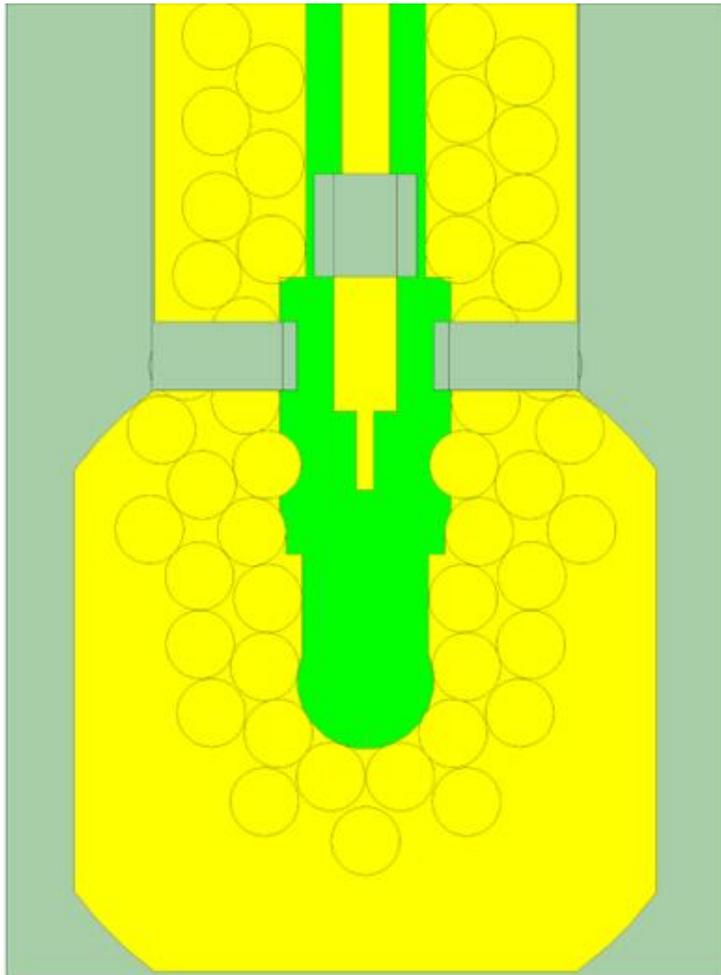
<sup>1</sup>VSWR per connector when tested on Samtec multi-layer test PCB

<sup>2</sup>Single connector insertion loss only

<sup>3</sup>May be further limited by PCB design

# PCB Reference Design

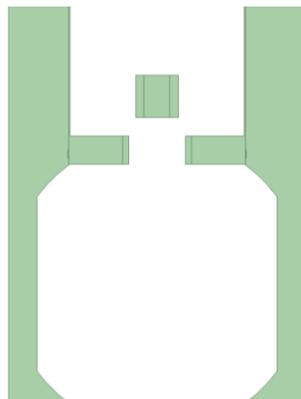
FOOTPRINT IMAGE



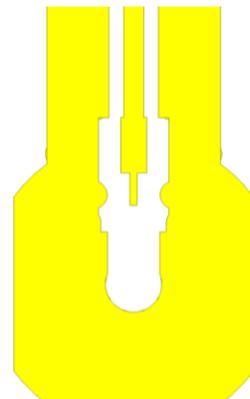
Layer Number	LayerName	Material	Thickness	
			mils	mm
	TOP_SM	PSR-4000-BN	0.71	0.018
1	TOP	PLATED COPPER (0_5oz)	2.09	0.053
	CORE01	I-TERA MT40 (2x1086) (67%) C	7.01	0.178
2	P02	COPPER (0_5oz) VLP2	0.59	0.015
	DIELO2	I-TERA MT40 (1x1080) (70%) PP	3.43	0.087
	DIELO3	I-TERA MT40 (1x1080) (70%) PP	3.43	0.087
	CORE04	I-TERA MT40 (2x1086) (67%) C	7.01	0.178
	DIELO5	I-TERA MT40 (1x1080) (70%) PP	3.43	0.087
	DIELO6	I-TERA MT40 (1x1080) (70%) PP	3.43	0.087
3	P03	COPPER (0_5oz) VLP2	0.59	0.015
	CORE07	I-TERA MT40 (2x1086) (67%) C	7.01	0.178
4	BOTTOM	PLATED COPPER (0_5oz)	2.09	0.053
	BOTTOM_SM	PSR-4000-BN	0.71	0.018
Total thickness over solder mask and plated copper			41.53	1.054

PCB STACK UP

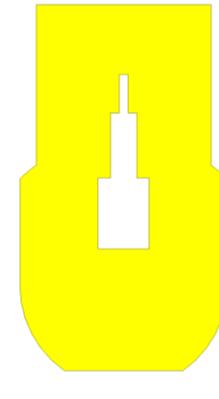
SOLDERMASK



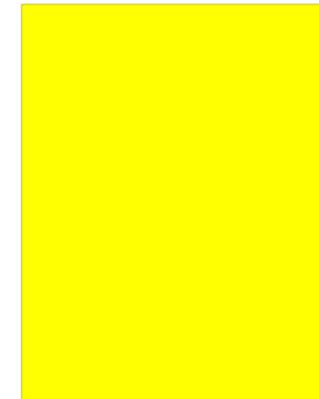
LAYER 1



LAYER 2



LAYER 3

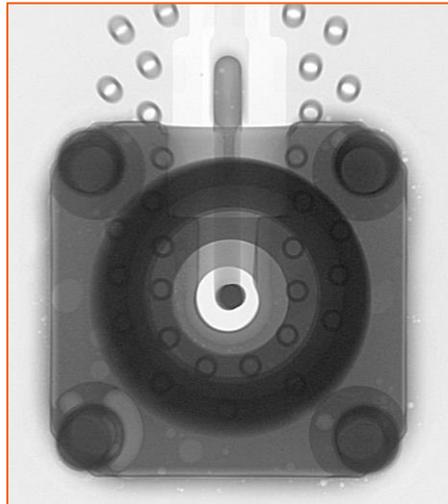
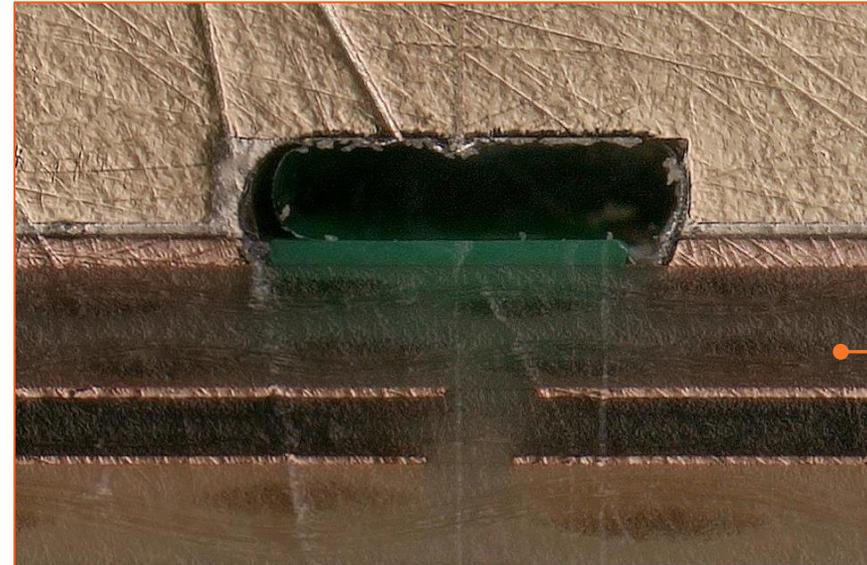
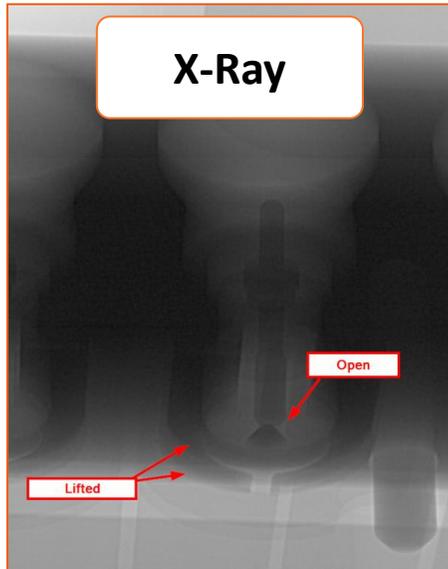


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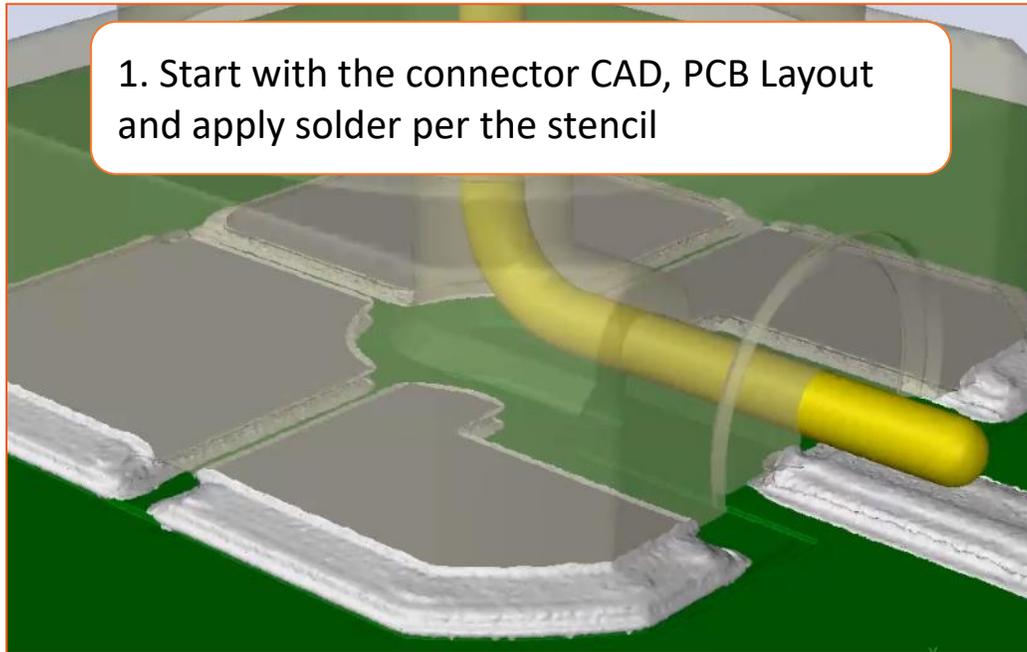
# RELATED WORK

# Tools & Techniques

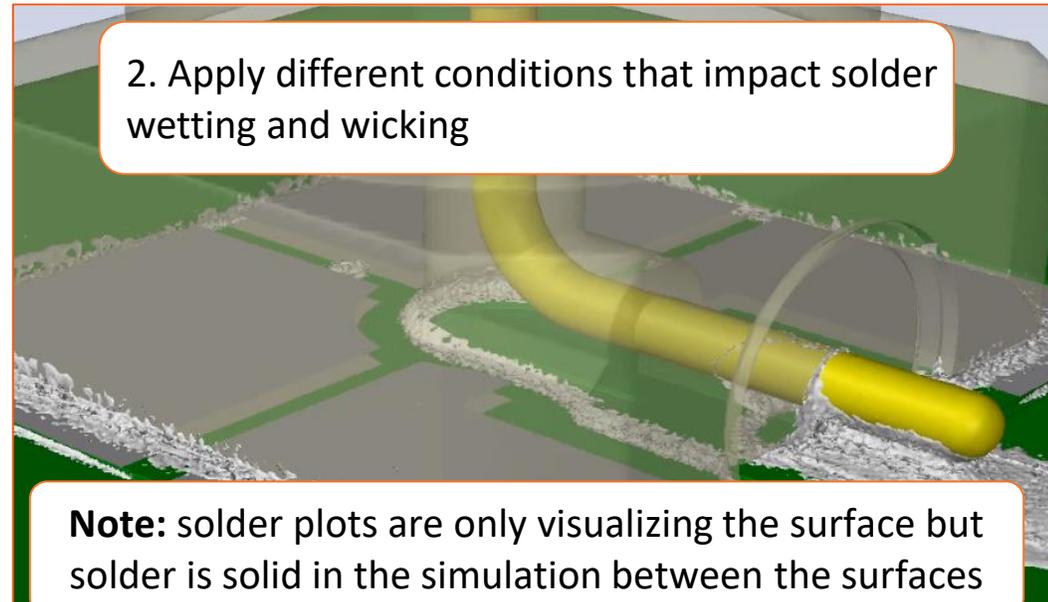


# Modeling Solder Reflow

1. Start with the connector CAD, PCB Layout and apply solder per the stencil



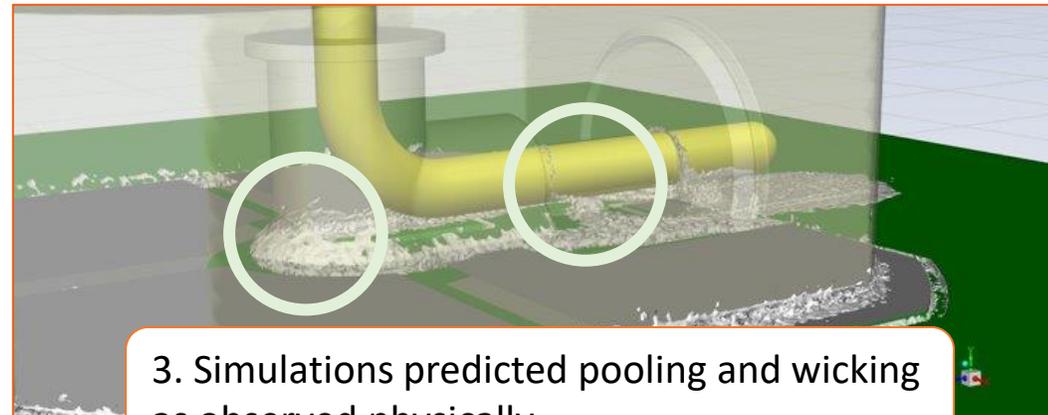
2. Apply different conditions that impact solder wetting and wicking



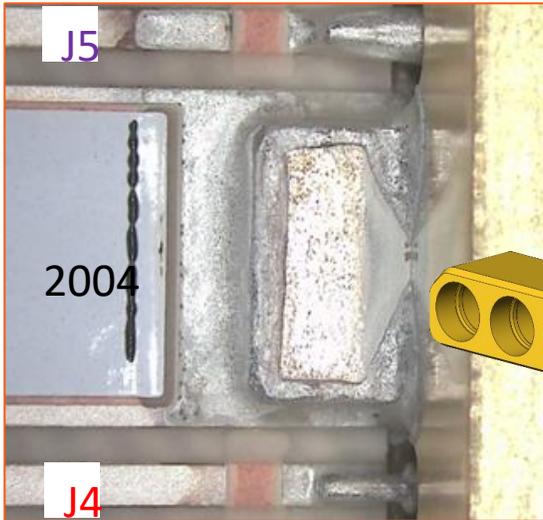
**Note:** solder plots are only visualizing the surface but solder is solid in the simulation between the surfaces

We are actively exploring workflows, developing modeling capabilities and refining material characteristics in order to develop improved methods of predicting solder reflow to minimize design iterations.

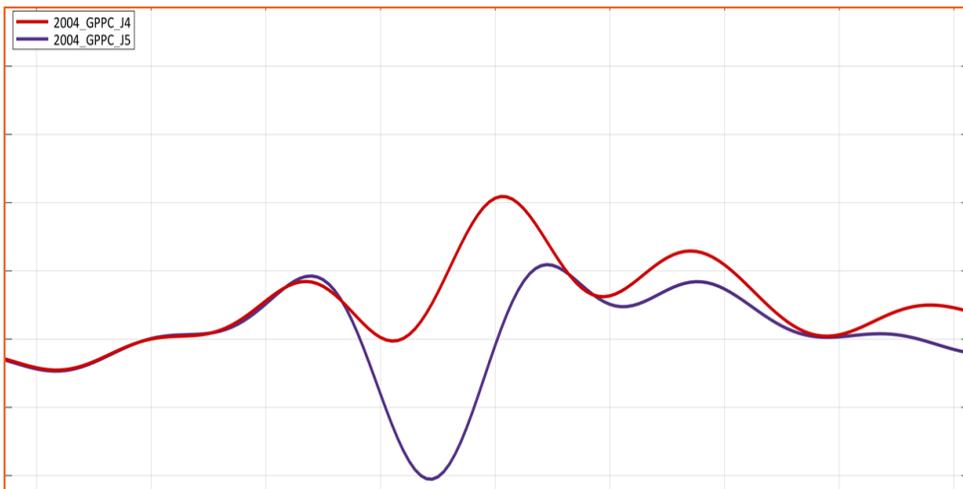
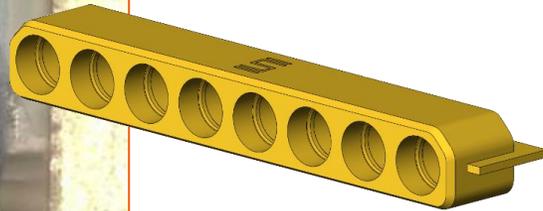
3. Simulations predicted pooling and wicking as observed physically



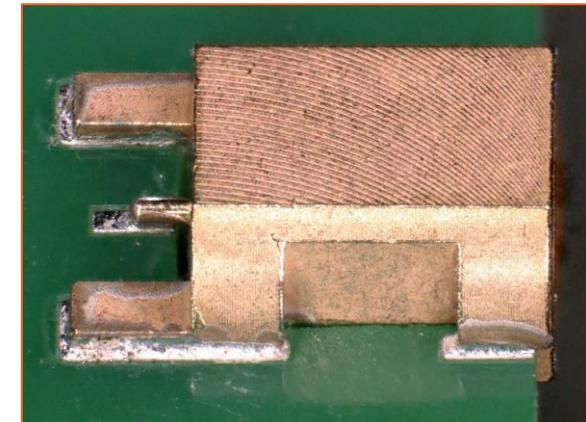
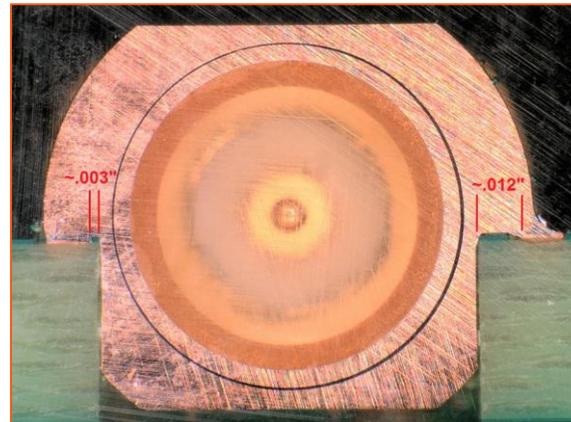
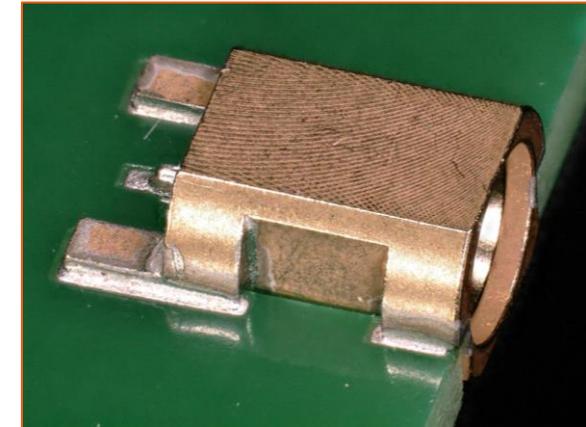
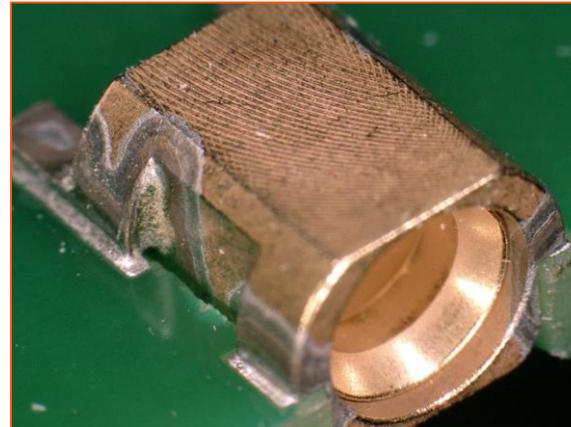
# Other Connectors



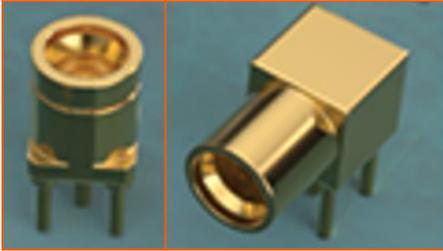
Ganged SMPM  
Edge Mount



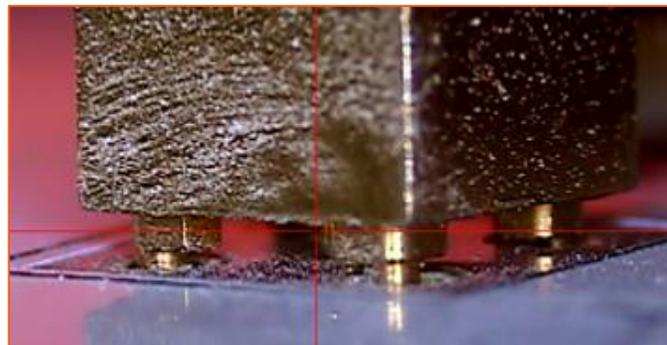
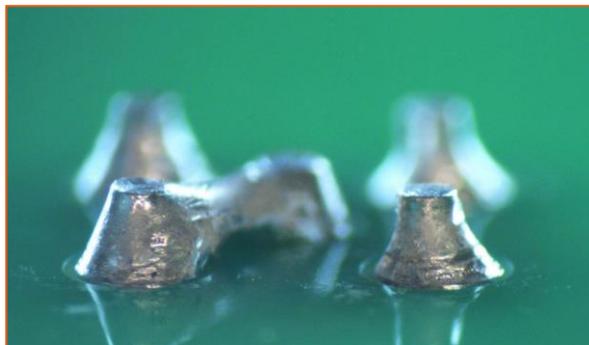
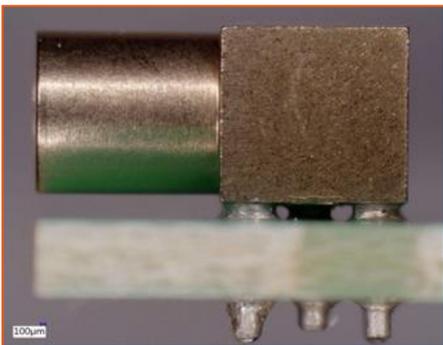
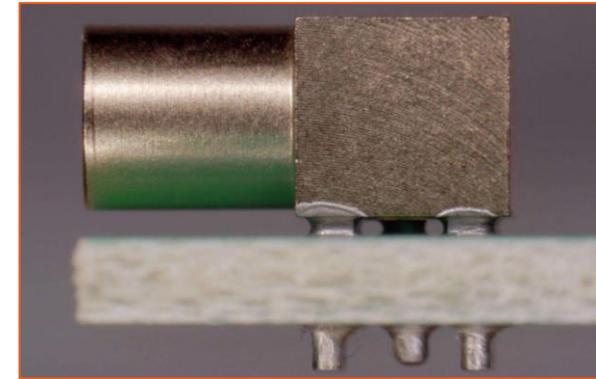
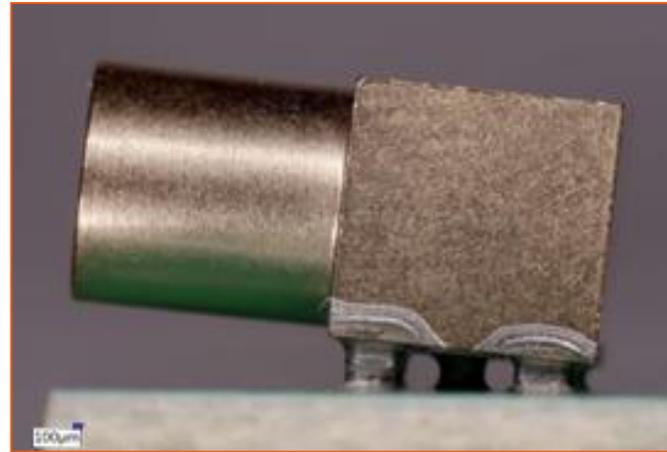
SMPM Edge Mount



# Other Connectors



SMPM Through-hole

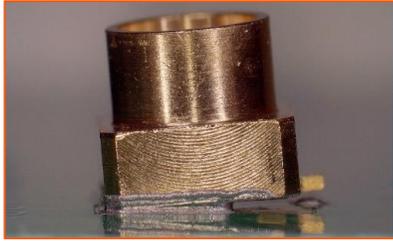


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TAKEAWAYS

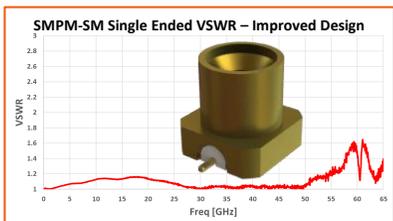
# TAKEAWAYS



- 1) Solder reflow plays an important role in the success and performance of high bandwidth RF connectors



- 2) To better control solder reflow, changes can be made to the connector, the PCB, and the process



- 3) The connector, PCB, and process were all improved to develop Samtec's high performance SMPM-XX-P-XX-ST-SM-1



- 4) The challenges of solder reflow and the impact it has on performance extends to all high bandwidth RF connectors



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SUDDEN SERVICE®

## PRECISION RF

Visit: <http://www.samtec.com/precisionrf>

Contact: [rfgroup@samtec.com](mailto:rfgroup@samtec.com)

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