gEEk® spEEk

Break Out Design by Inspection | Presenter: Travis Ellis

INTRODUCTION

The purpose of today's discussion is to cover connector to board transitions and common impairments to their performance.

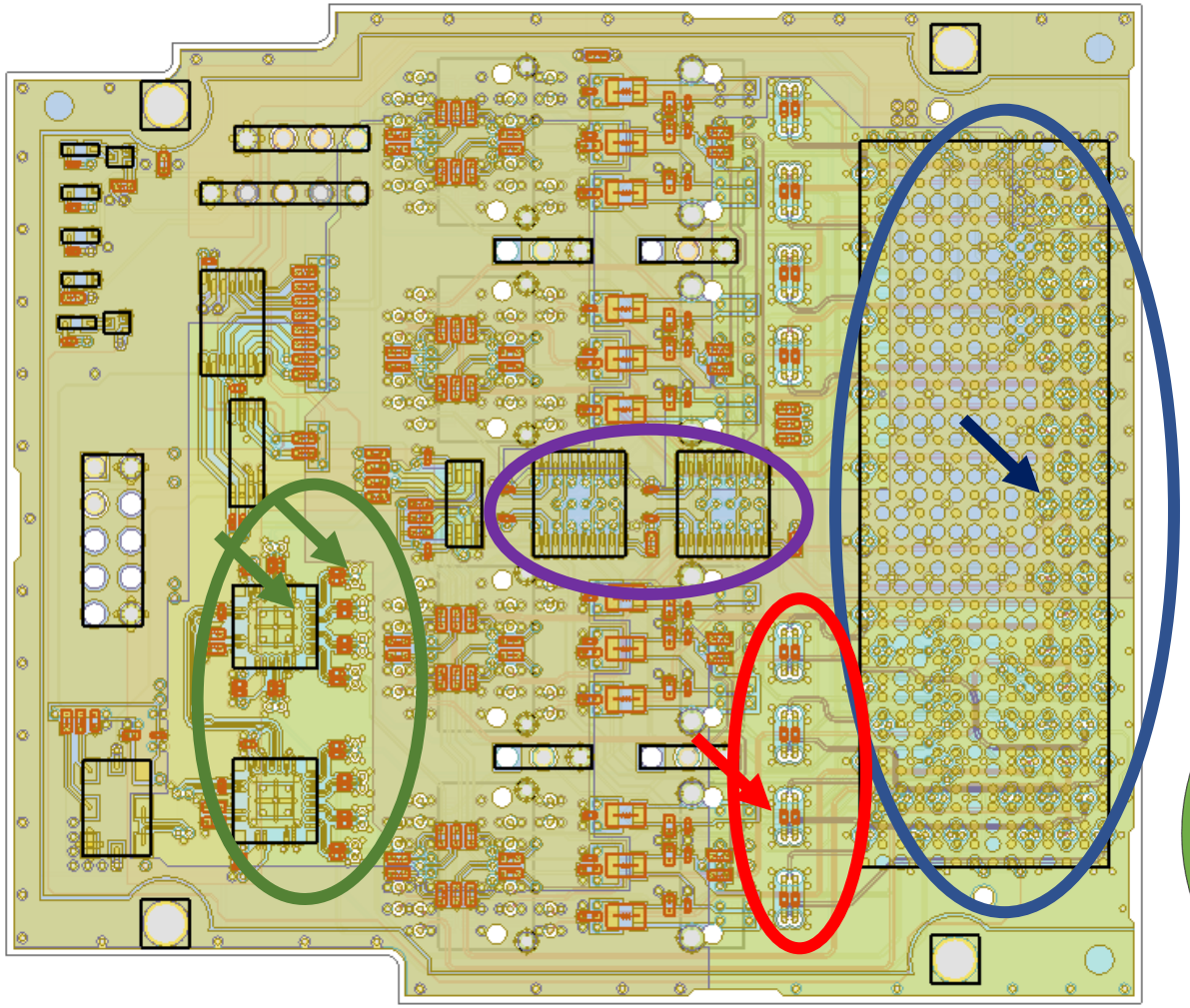
Some key points:

- Visually Designing Breakouts
  - Trace/pad relative sizes
  - Where are the ground vias?
- Impedance Control
- Return Path Management

What we'll cover

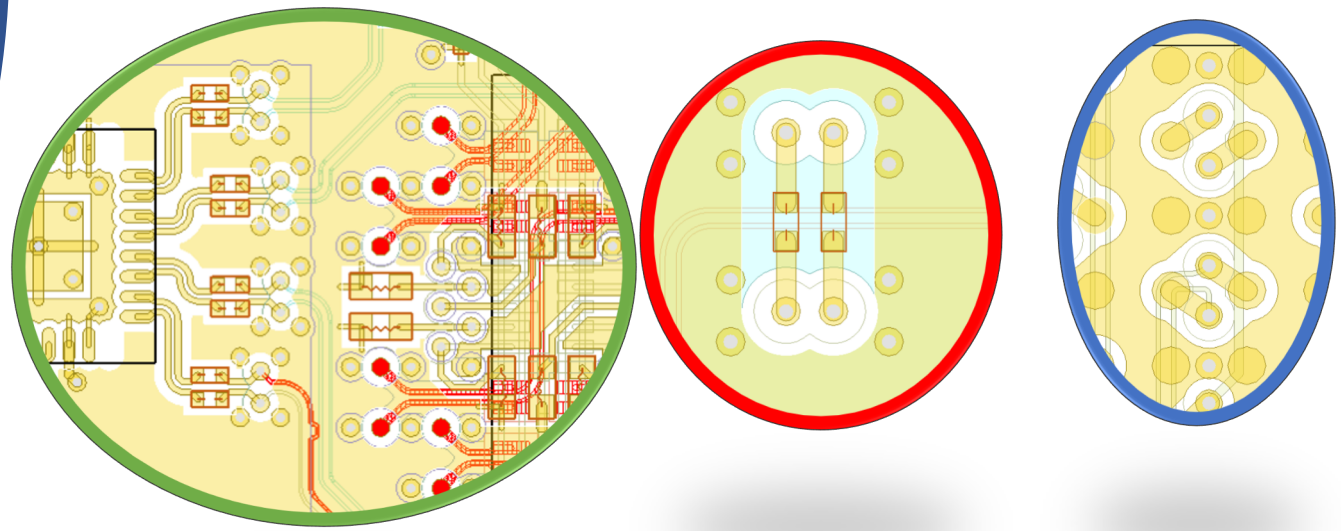
- High level view of a printed circuit board
- 2 Row connector breakout region optimization
- Moore's law applied to breakout regions

Making Sense Of The Noise

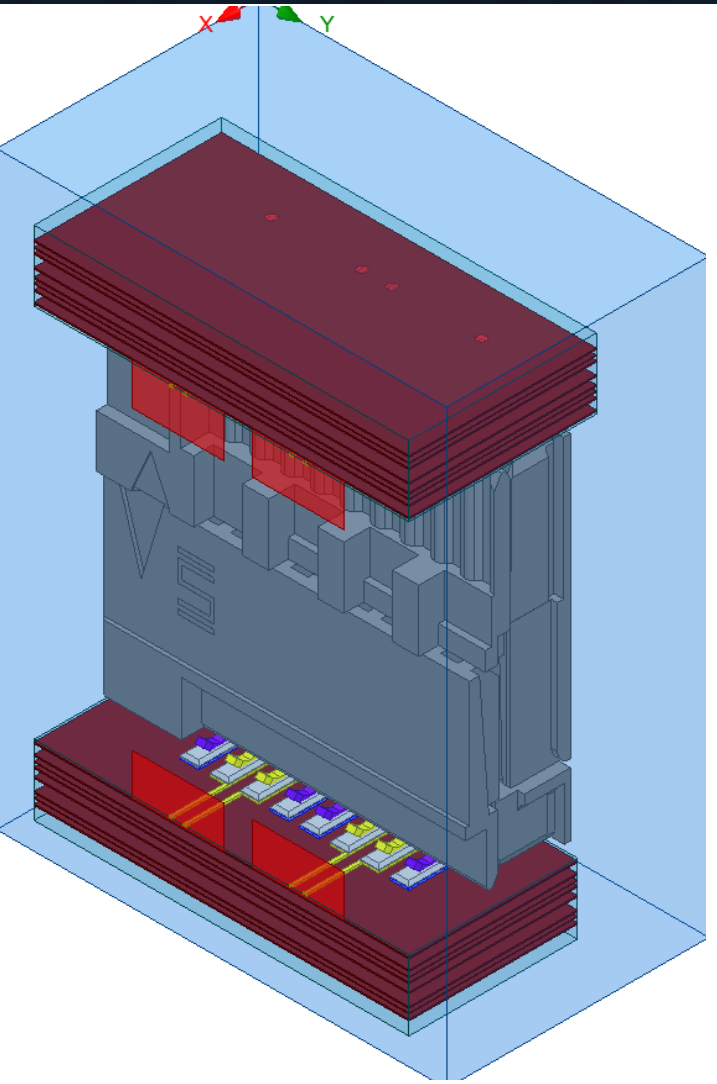


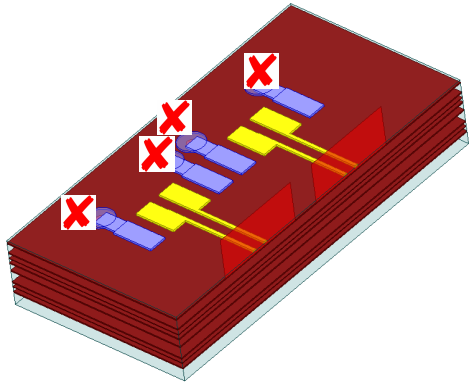
Higher density requirements lead to designs where breakout regions become melded between components.

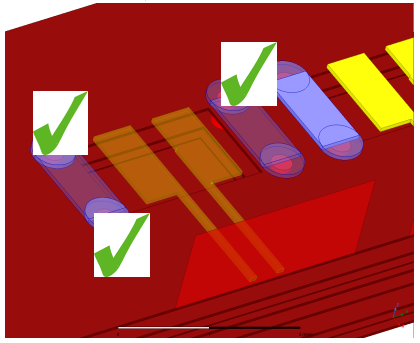
- Start on one end of the transmission path
  1. **High Speed IC's and DC Blocks**
  2. **Lower Speed Digital Logic**
  3. **DC Blocks With Tuned Vias**
  4. **LPAX Breakout**

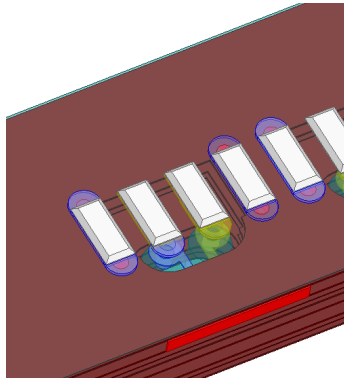


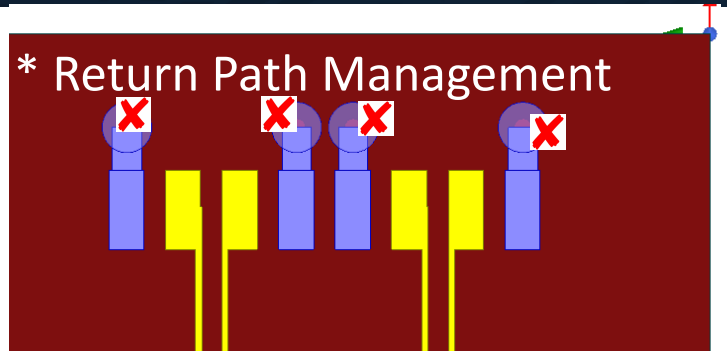
Common Breakout Mistakes

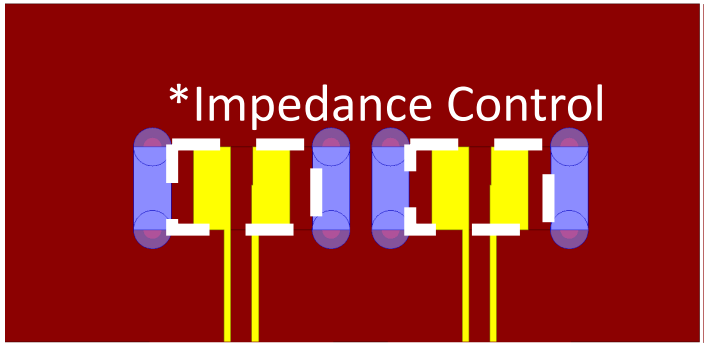


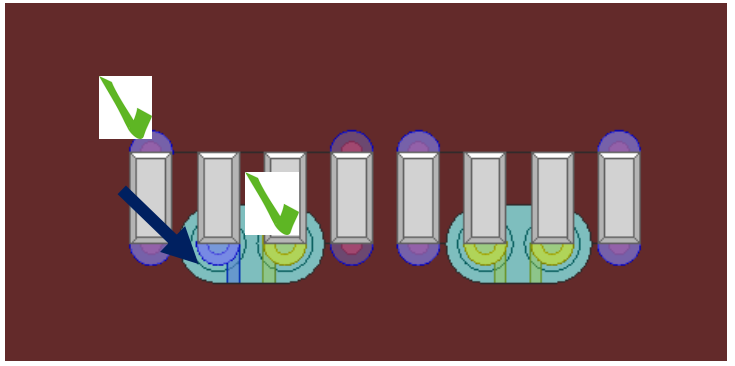




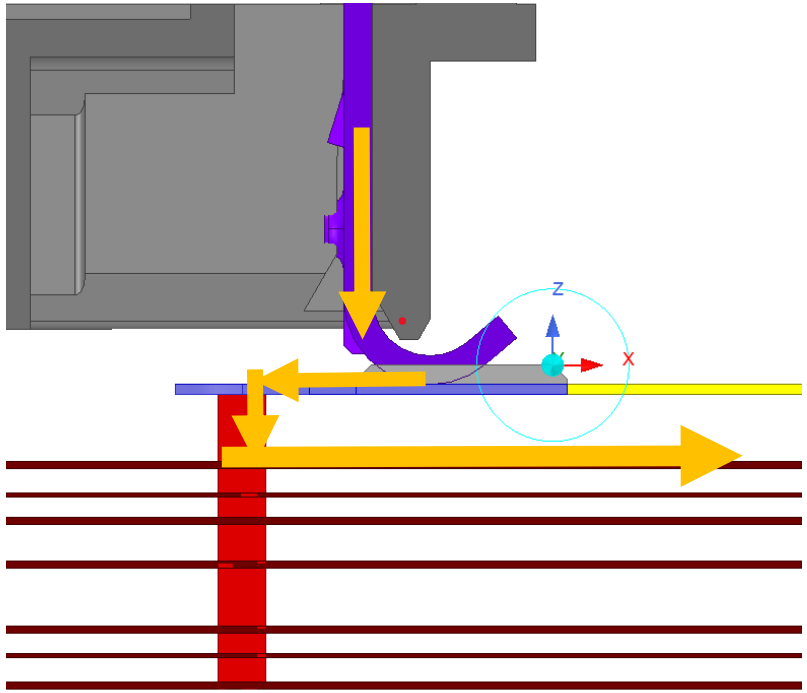


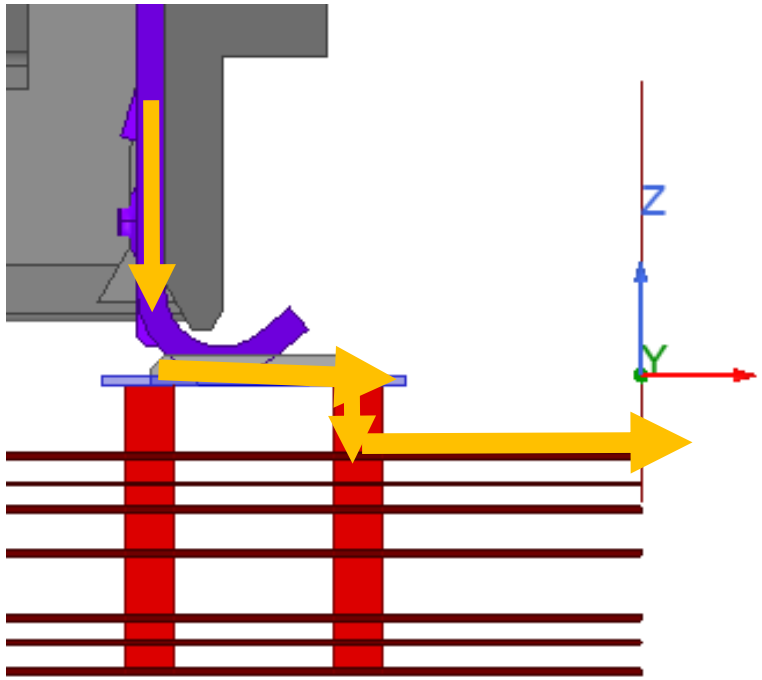






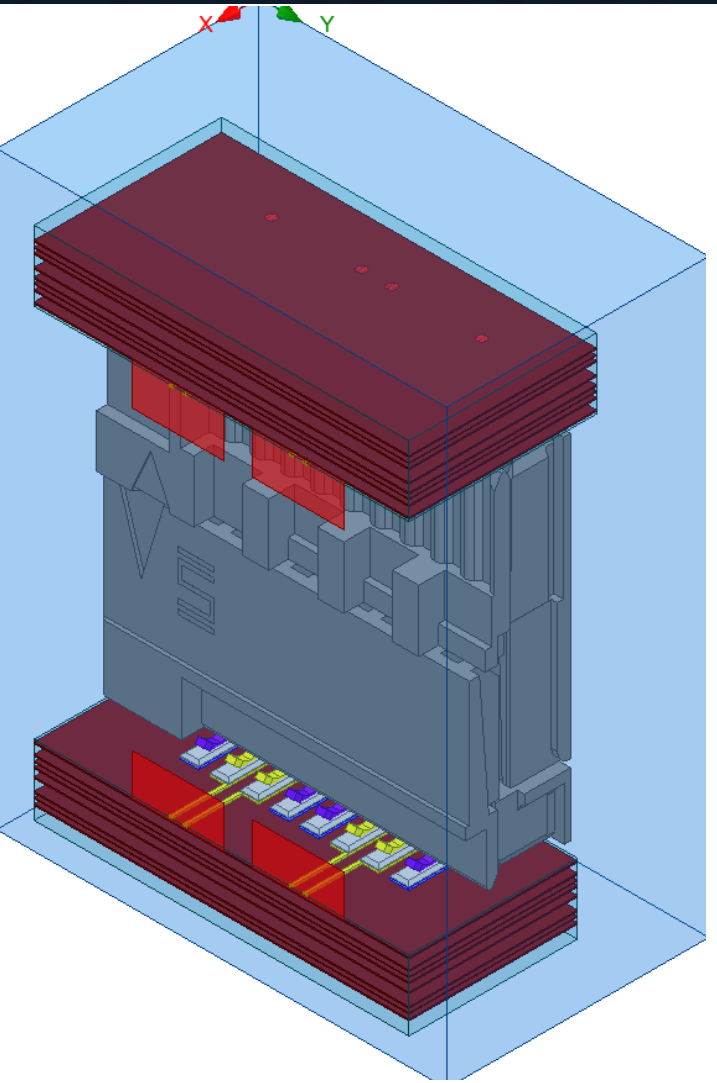
Return Path Management



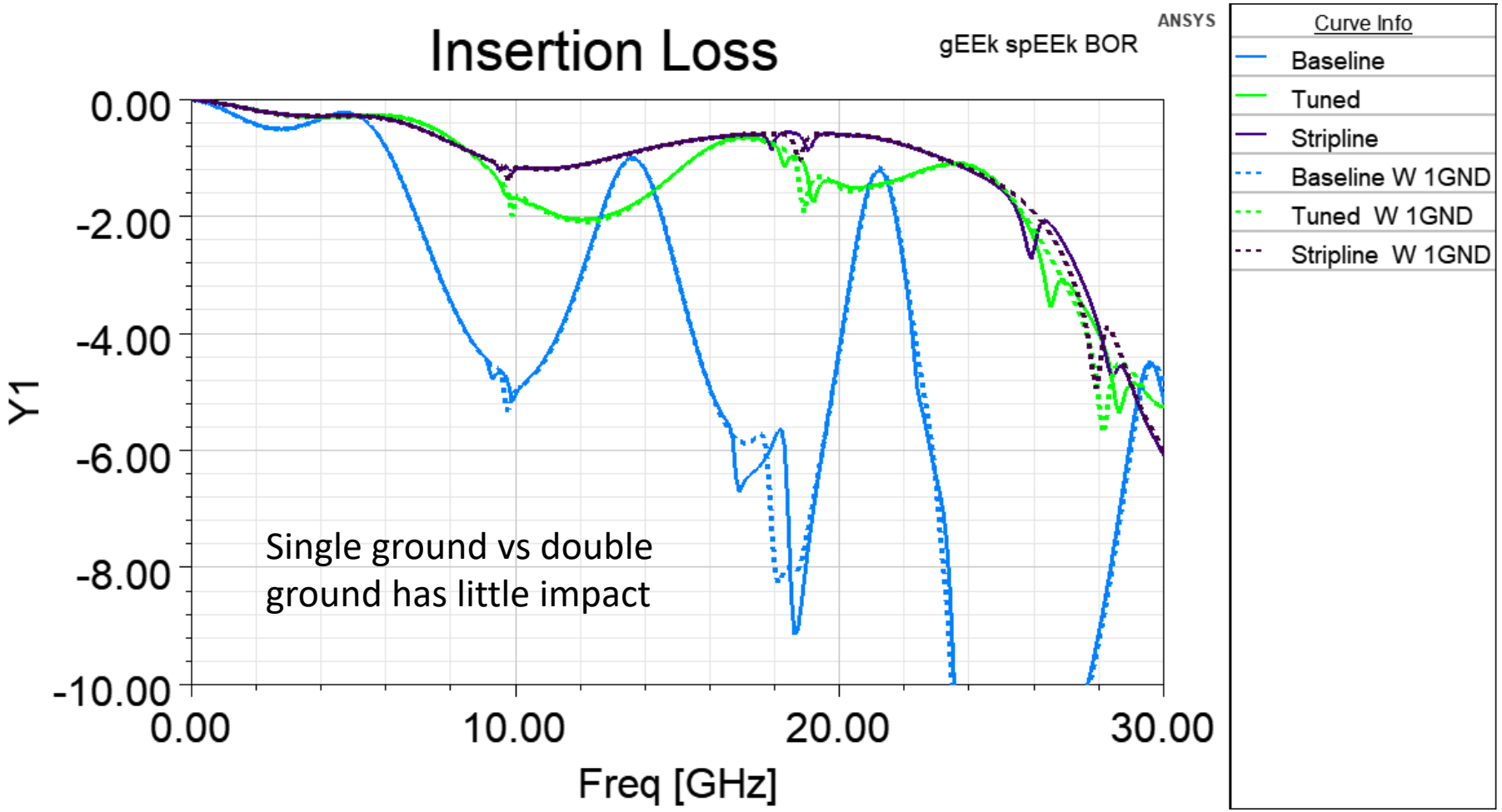


The return path is physically longer then the signal path. This impairs performance, increases Crosstalk and shifts peaking lower in the frequency band.

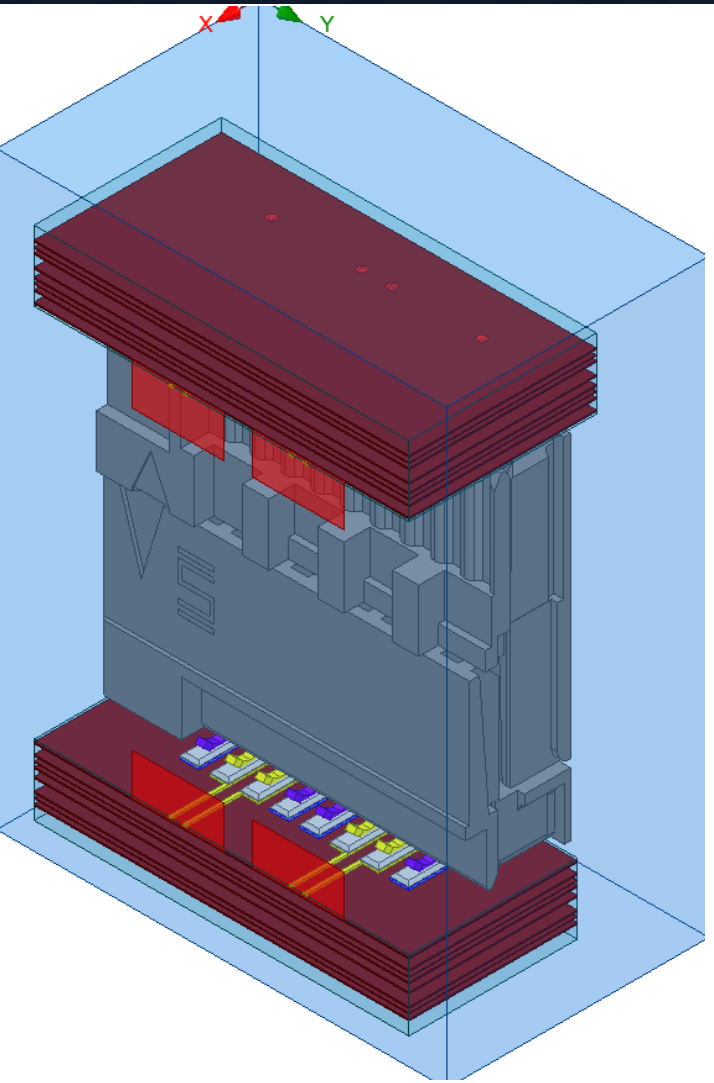
The consequences



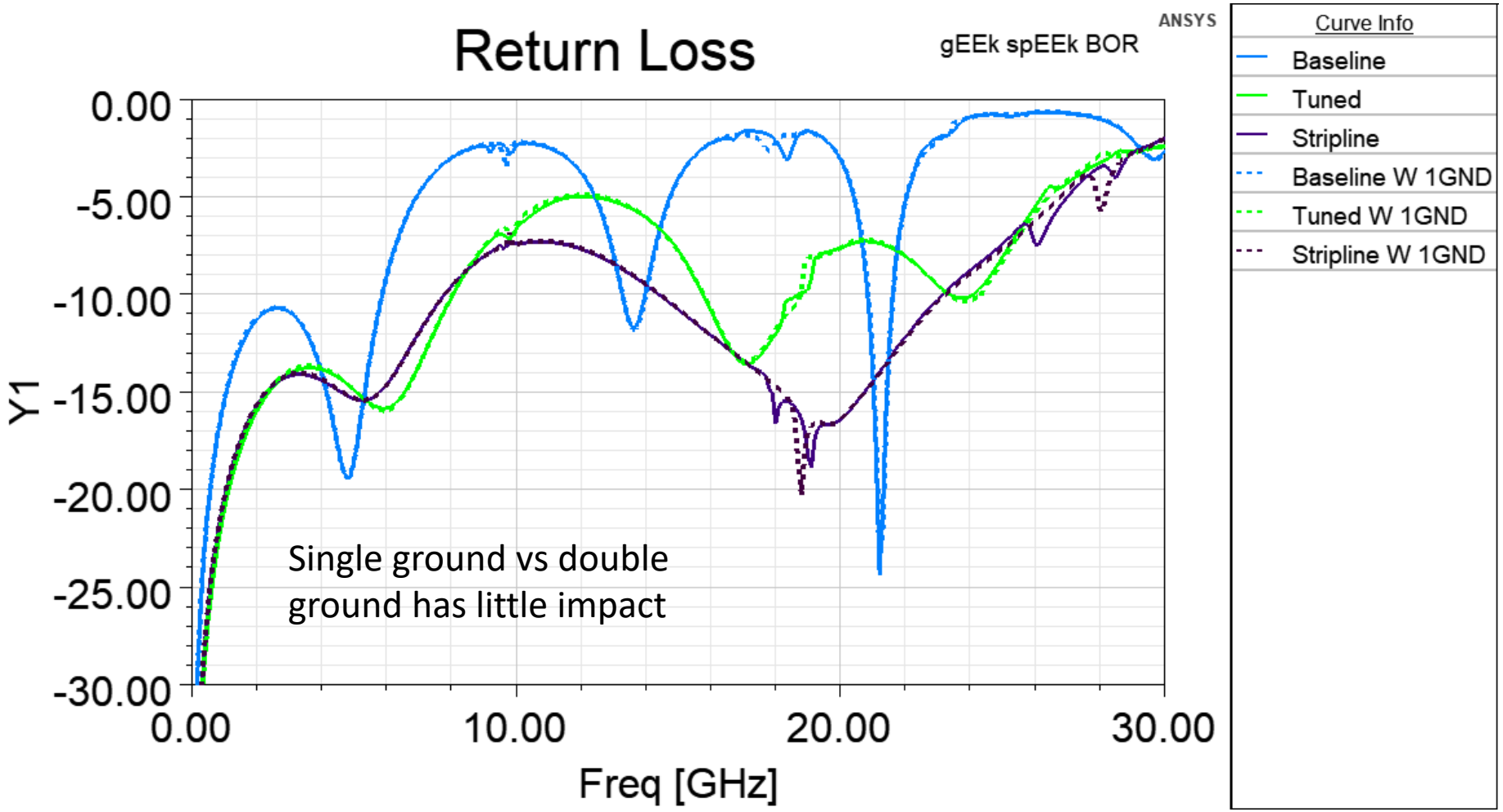
10 mm Mated Height



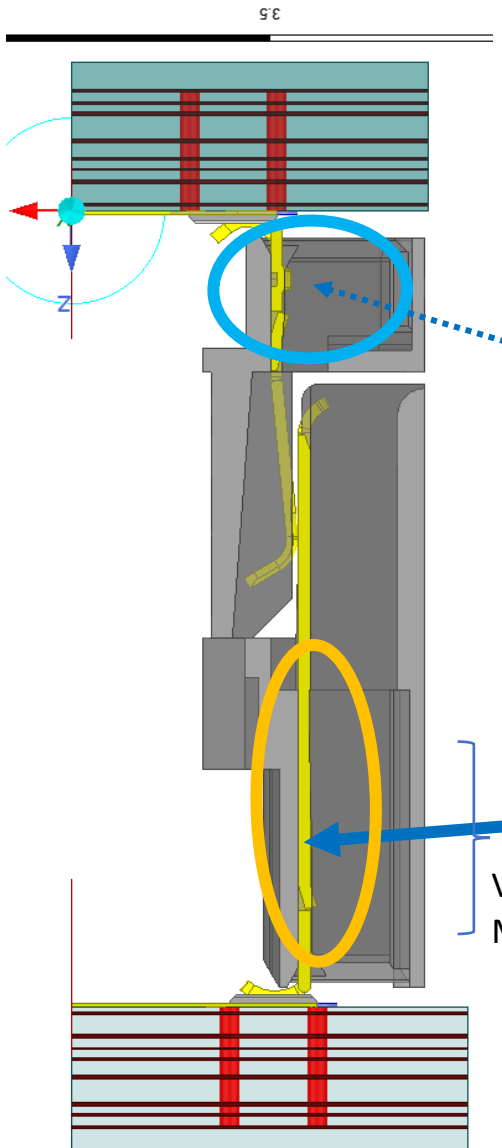
The consequences



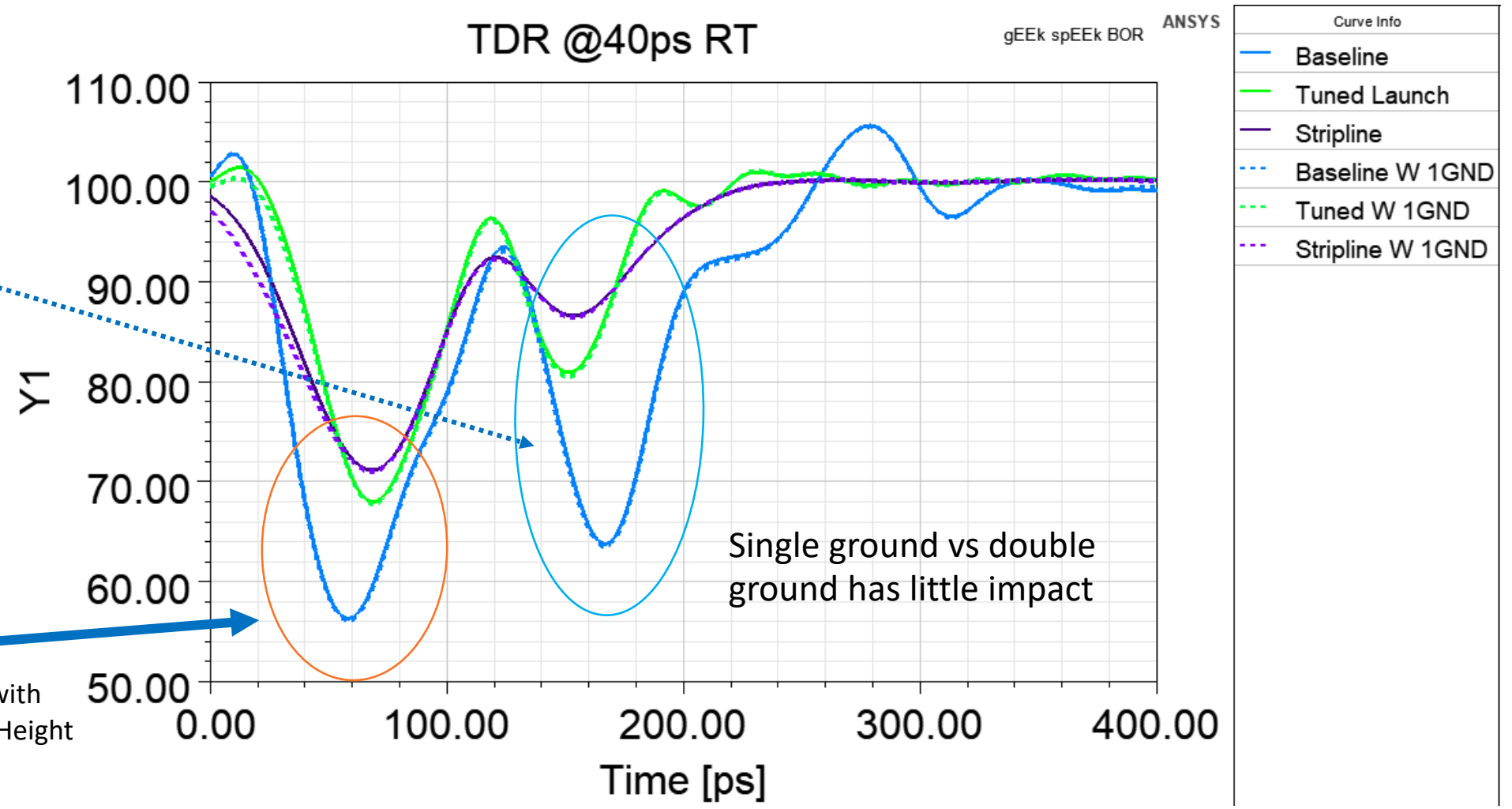
10 mm Mated Height



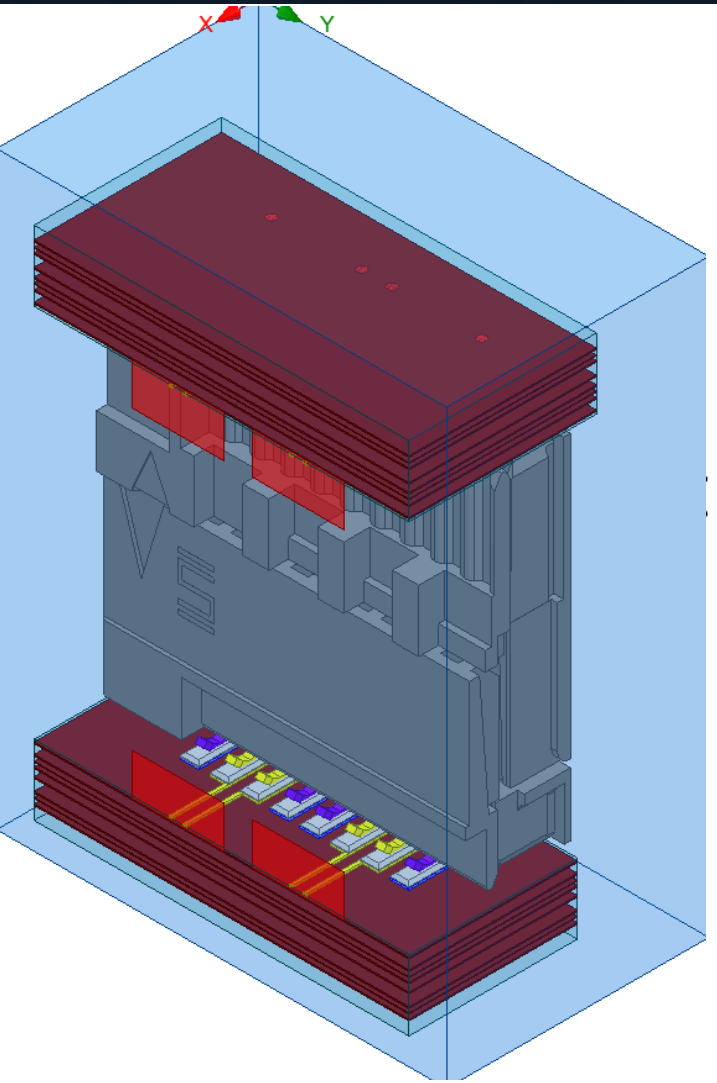
The consequences



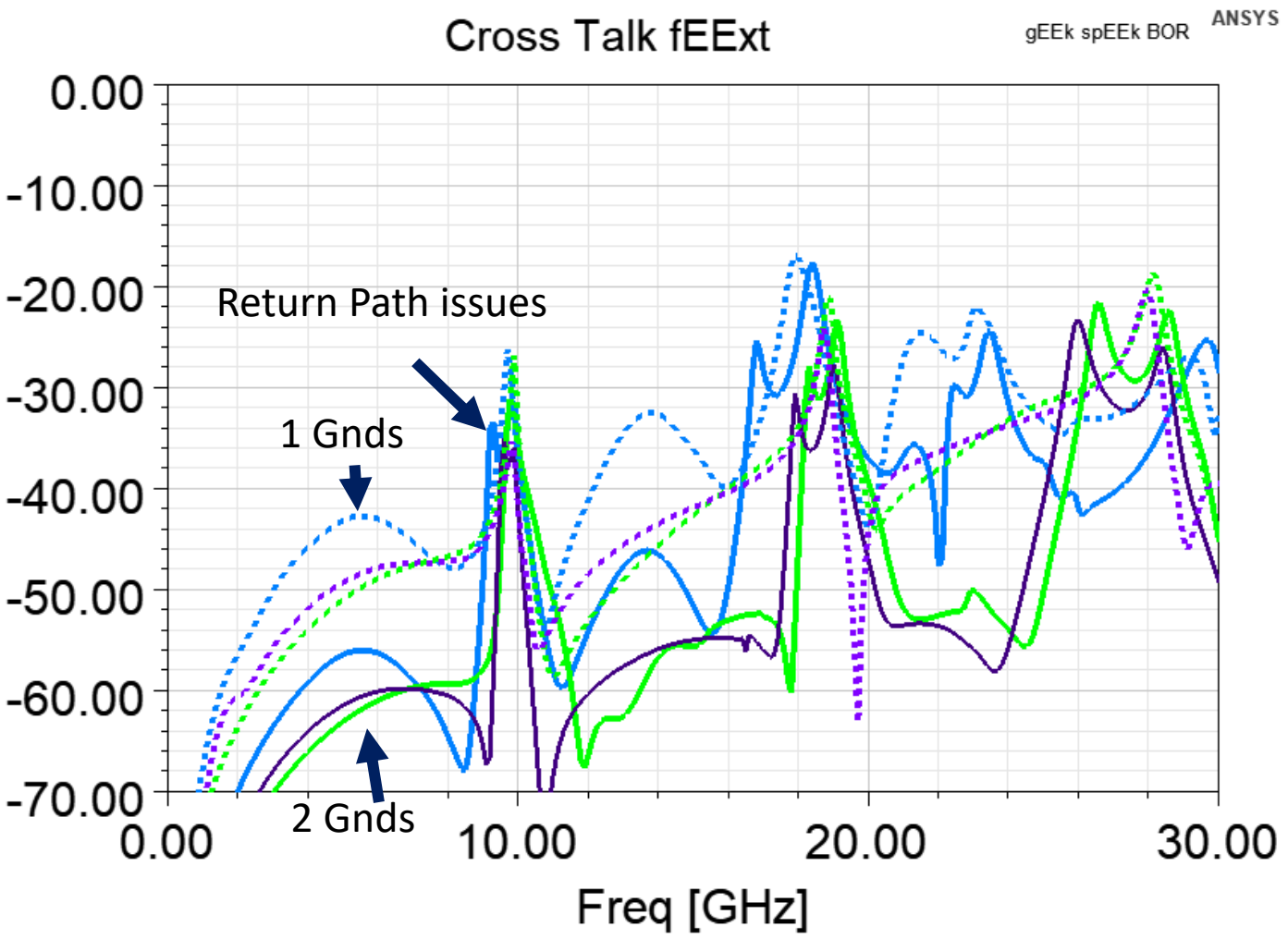
Varies with
Mated Height



The consequences FEXT

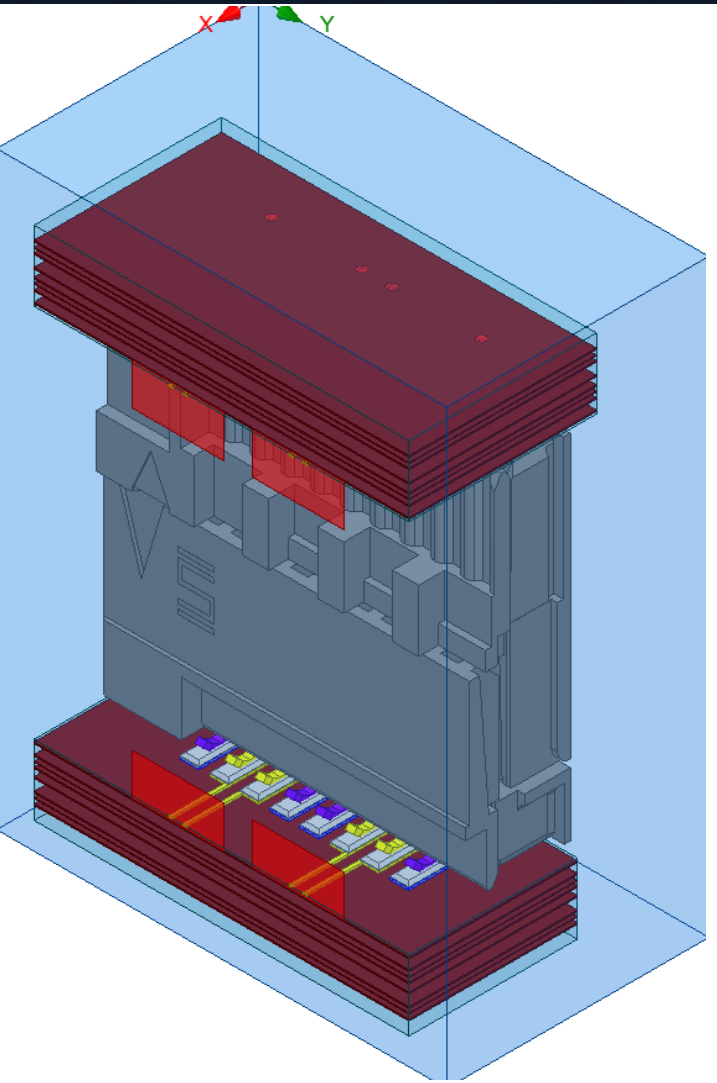


10 mm Mated Height

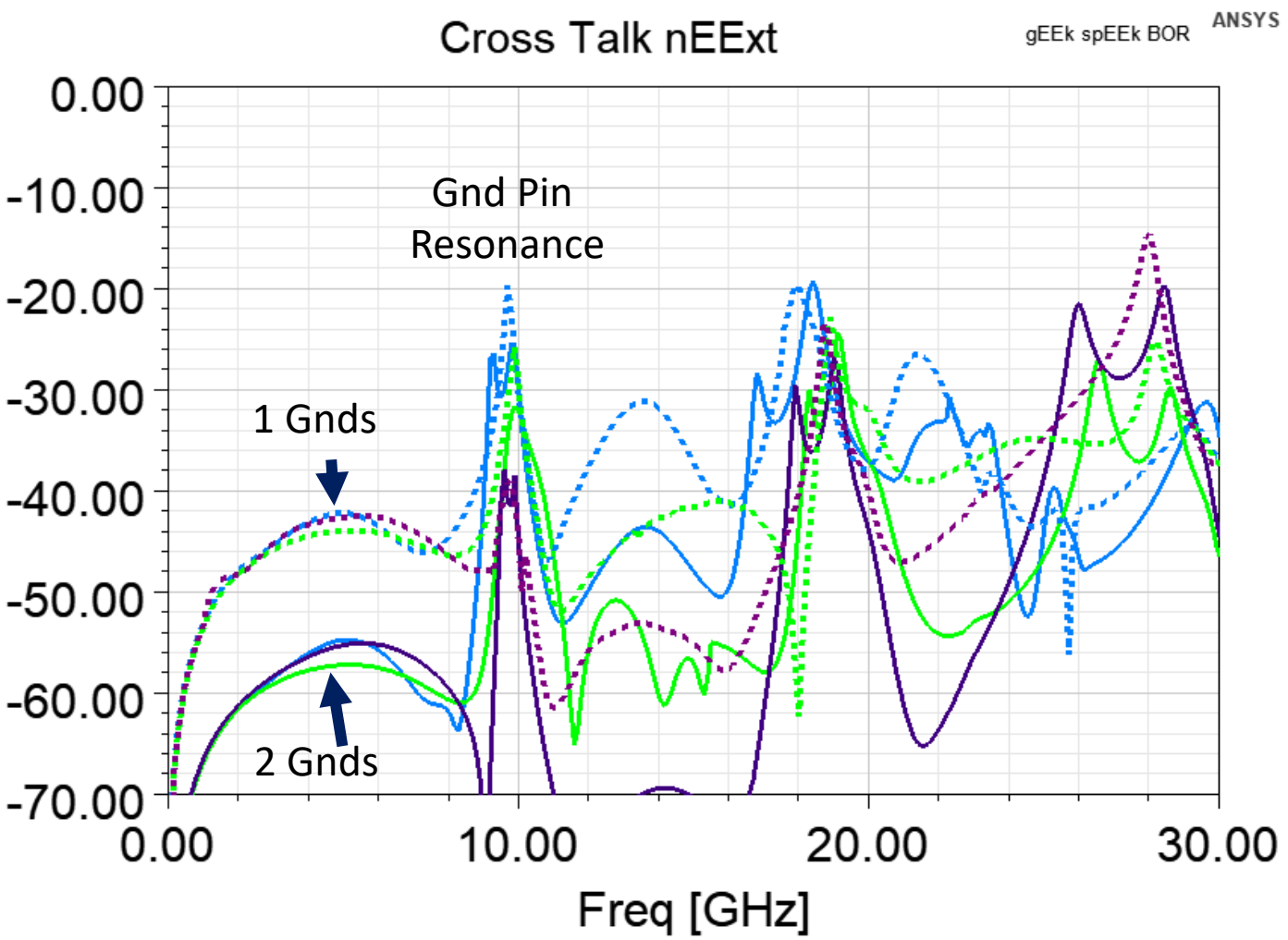


**A shorter connector would shift resonances higher.

The consequences NEXT



10 mm Mated Height



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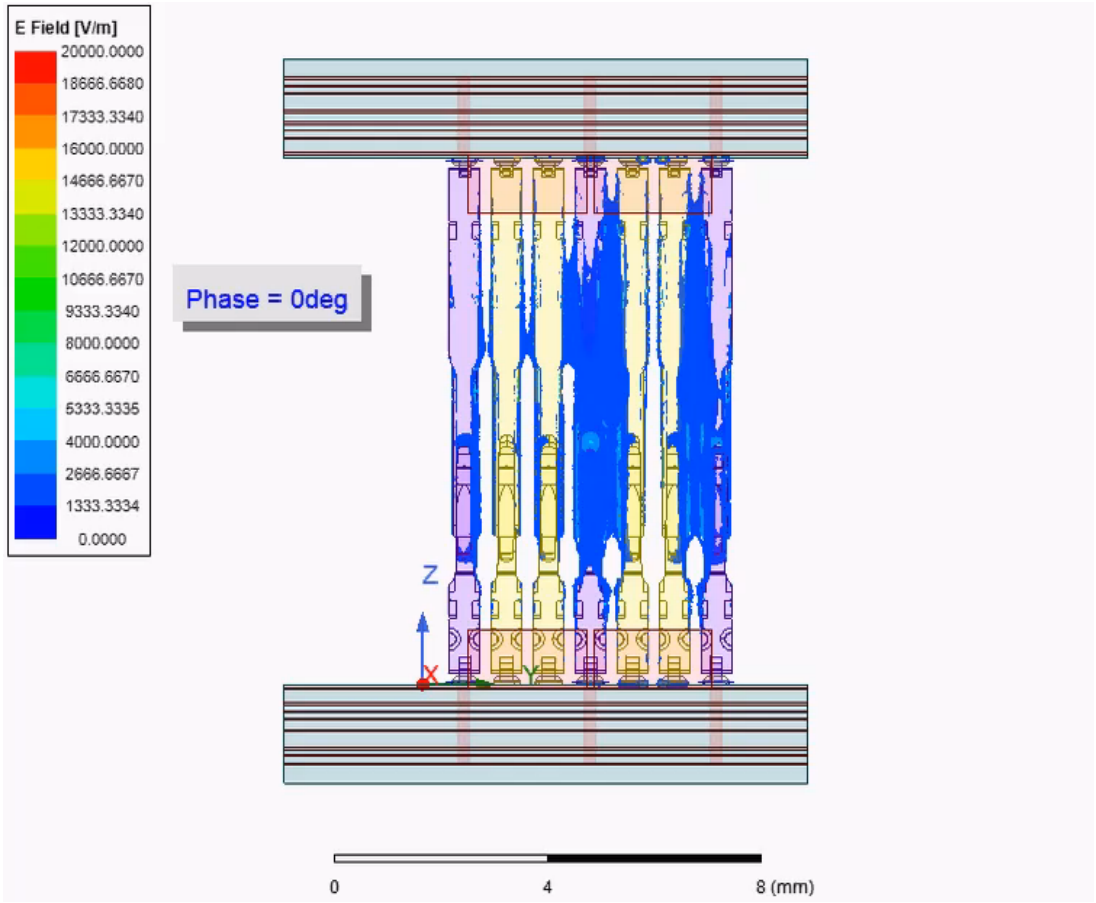
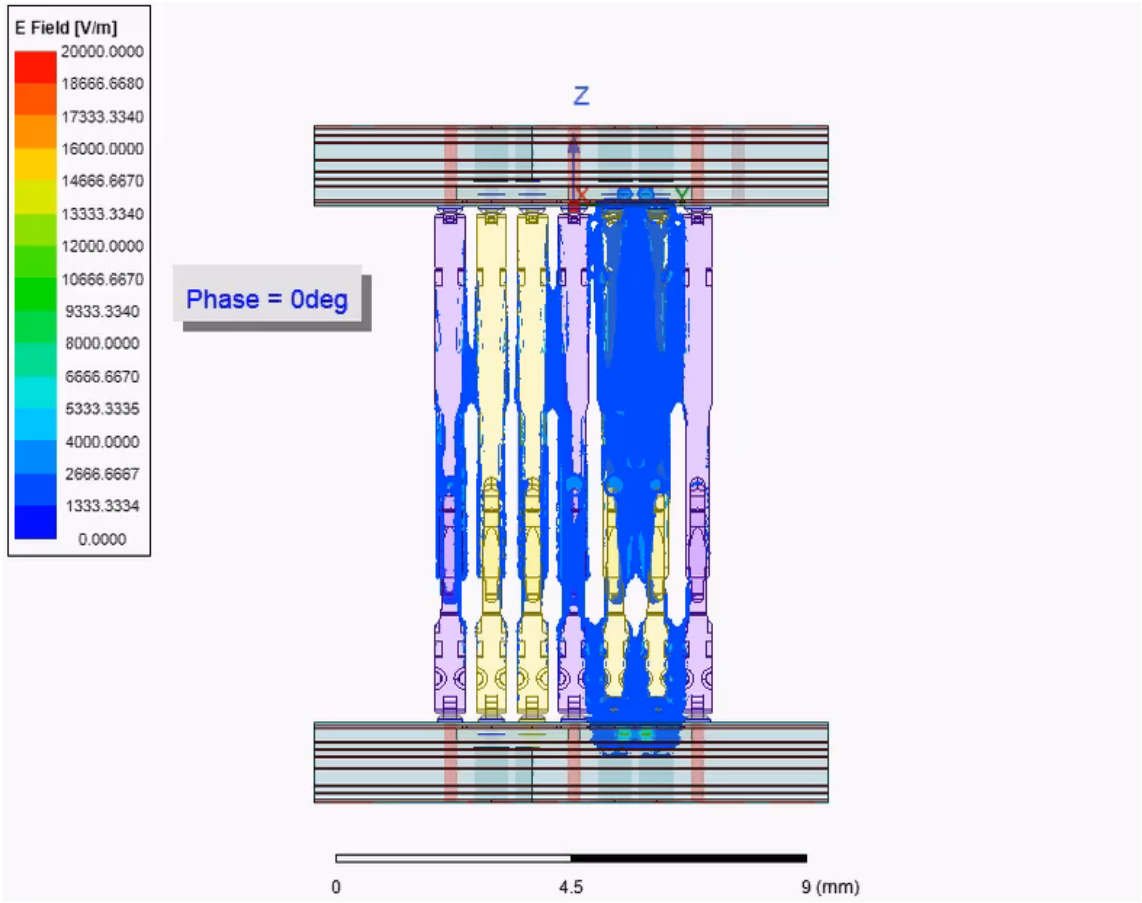
Field Plots

Microstrip

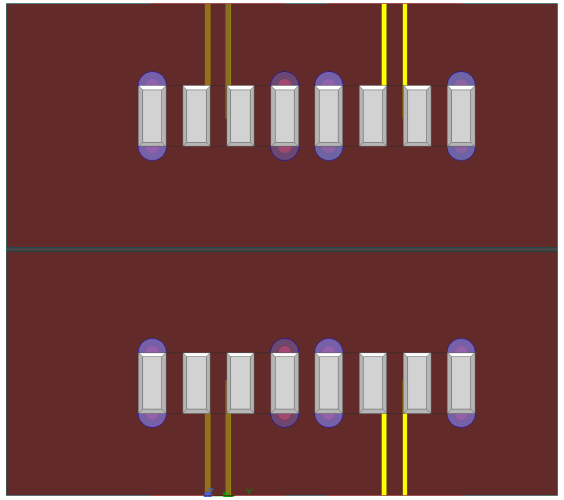


Stripline

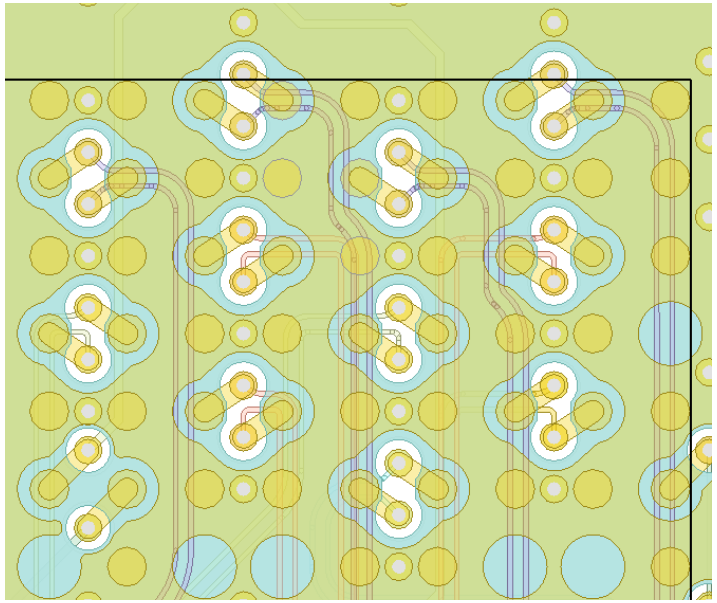


Moore's Law applied to breakouts

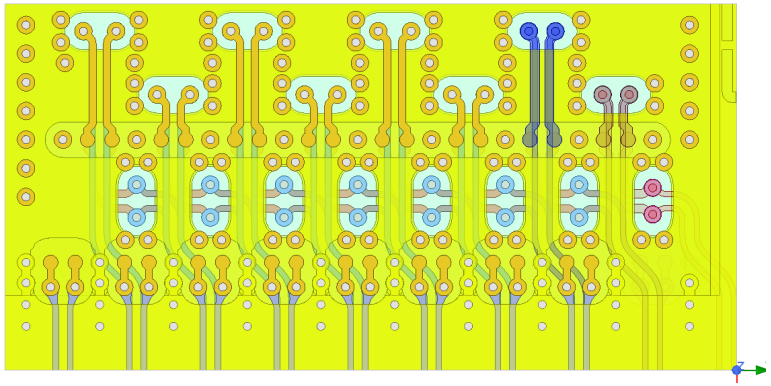
Generic 2 Row
Nyquist ~8Ghz



1.25 mm Pitch Arrays
Nyquist ~16Ghz



0.635 mm State of the art Arrays
Nyquist > 32Ghz



Connectors and their BOR ecosystem evolve to support greater data rates on roughly a 5-year cycle.

What was covered

1. Using impedance concepts to determine when plane voiding is appropriate
2. How return path impairments affect crosstalk
3. How to reduce insertion losses of connector and their **B**reak **O**ut **R**egion ecosystem with careful design.

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