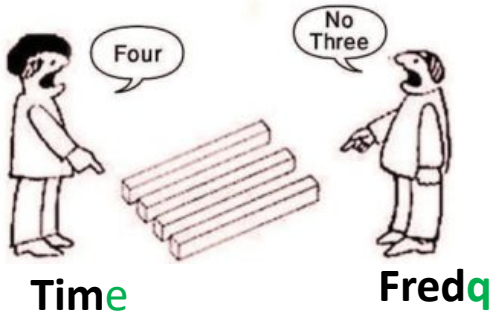
gEEk® spEEk

DC Block Capacitor Location (Does it matter?)

Presenter: Gustavo Blando

SCOPE



Where should we put Capacitors?

Close to TX or RX ?

Symmetry and Reciprocity (S-parameters)

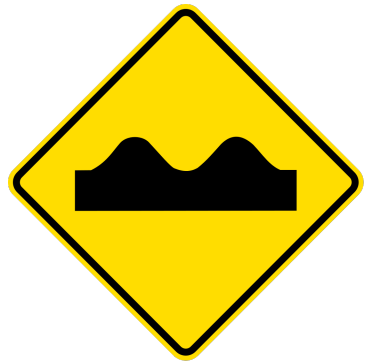
Time Domain Reflections

Test Cases

Simple Capacitor Representation

Topologies

Some Math

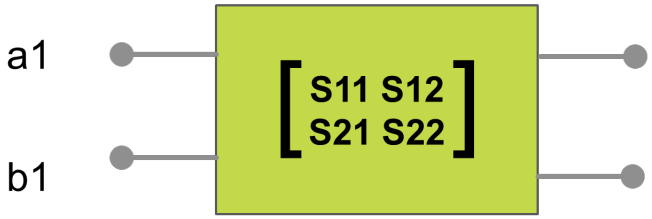


Impedance Discontinuity in Capacitors

How to get a transparent DC-Blocking cap?

Conclusions

SYMMETRY/RECIPROCITY



$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S11\ S12 \\ S21\ S22 \end{bmatrix} \begin{bmatrix} a1 \\ a2 \end{bmatrix}$$

b1 = S11*a1 + S12*a2
b2 = S21*a1 + S22*a2

Symmetric → **S11 == S22**

Reciprocal → **S21 == S12**

Most passive topologies are **Reciprocal**, not **Symmetrical**

S11 <> S22
S21 == S12

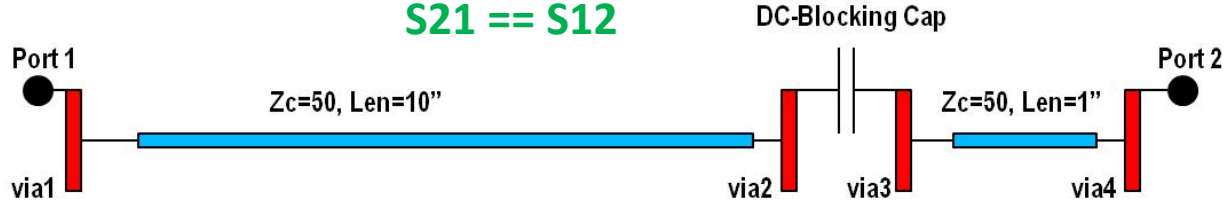
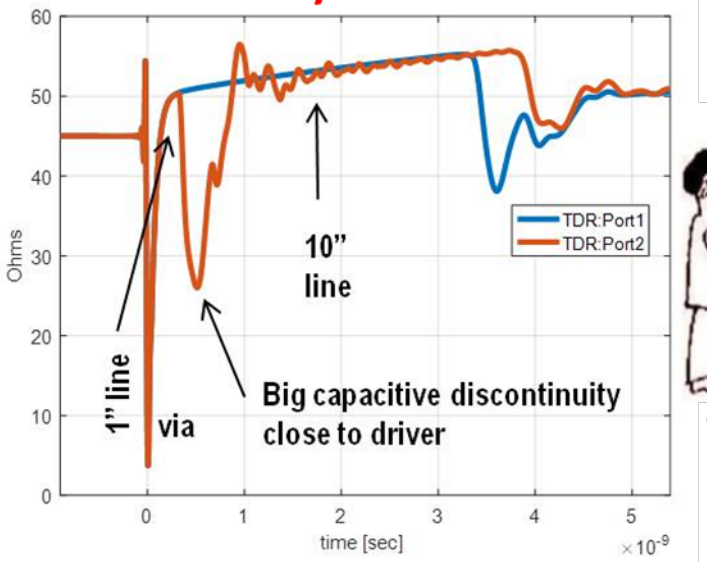
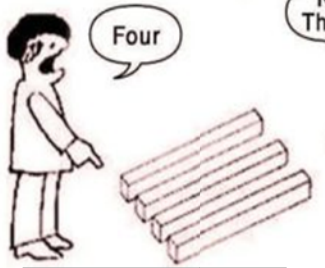


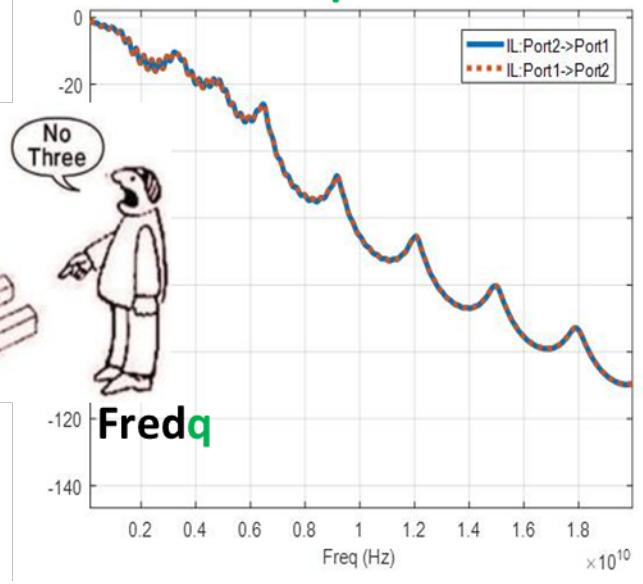
Figure 1: Simple topology, (capacitor close to one end)

Non-Symmetrical





Reciprocal



WHO IS RIGHT?

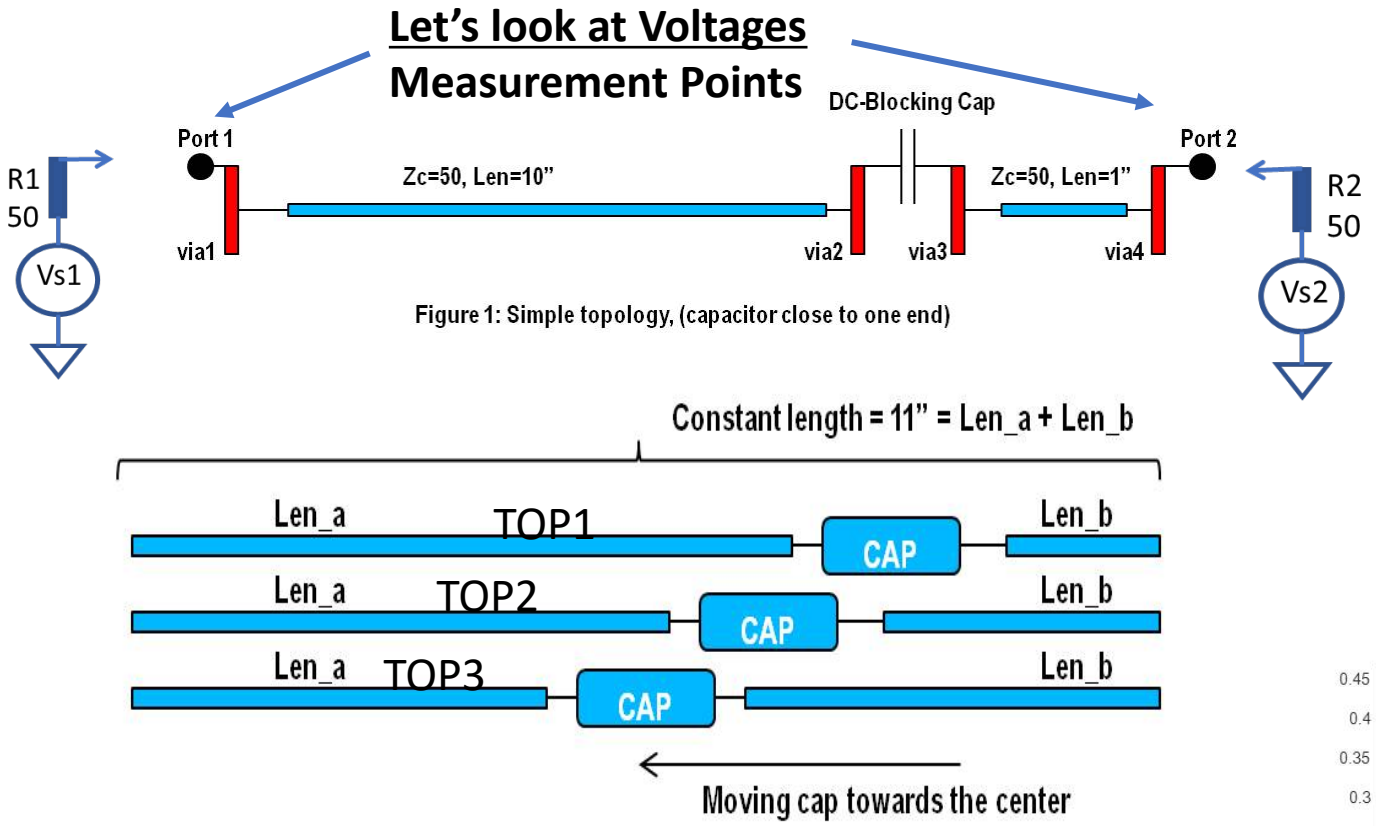
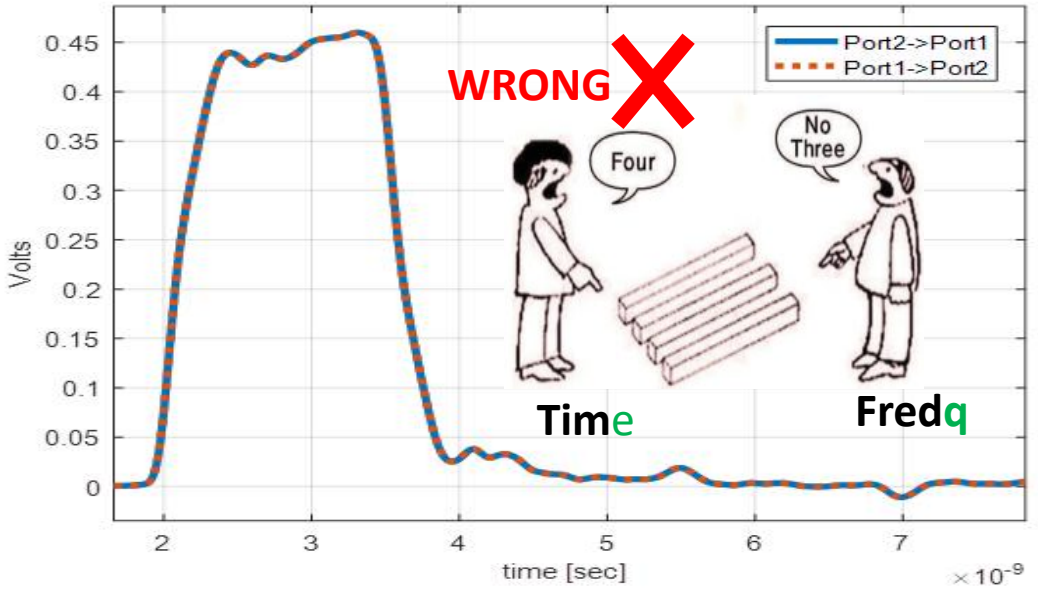
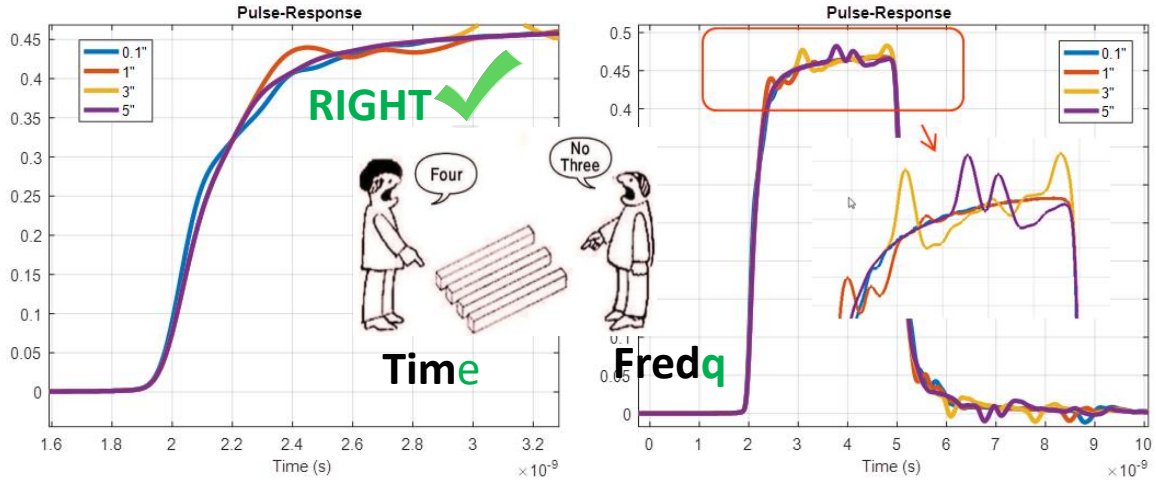


Figure 1: Simple topology, (capacitor close to one end)





- For any given topology, same results are obtained, driving from left or right. **(Fred was right!!)**
- If we change the location of the capacitor, it's a different topology and results change **(Tim is also sort of right!!)**

LET'S COMPLICATE THINGS!!

Voltage Transfer Function

$$H(s) = \frac{V_2(s)}{V_S(s)} = \frac{S_{21}}{2}\left[\frac{(1-\Gamma_S)(1+\Gamma_L)}{(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{12}S_{21}(\Gamma_S\Gamma_L)}\right]$$

Reflection Coefficient (source) & (load)

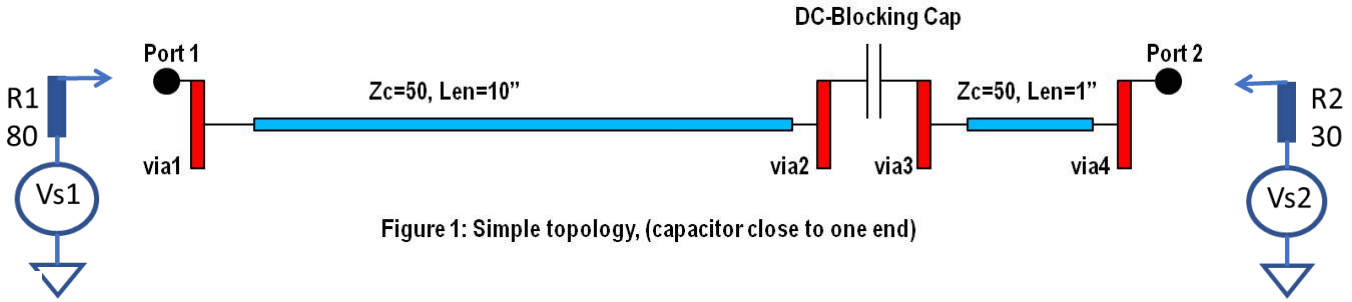
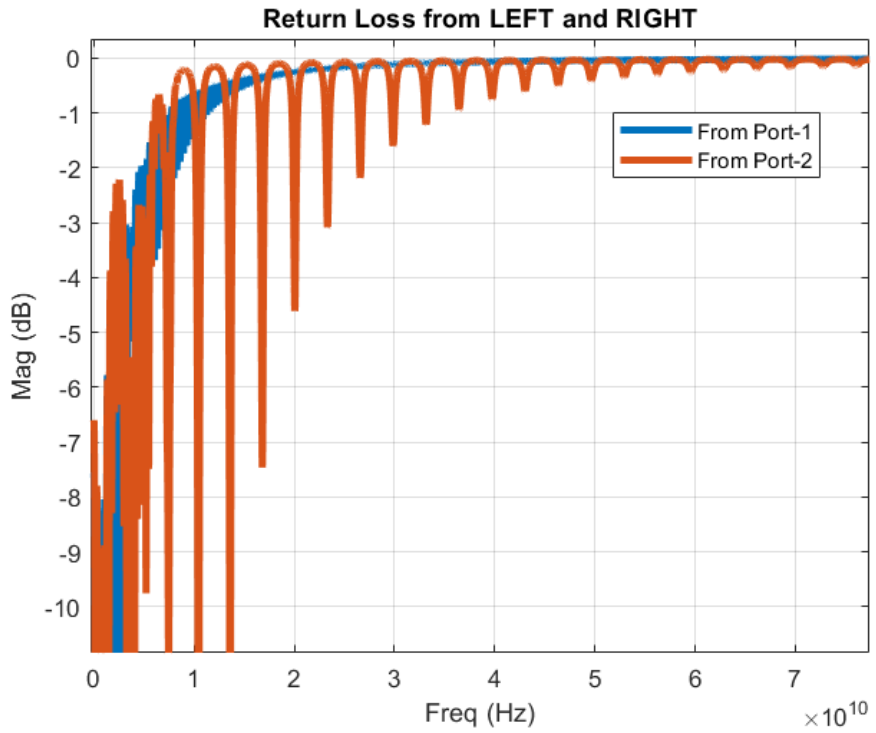
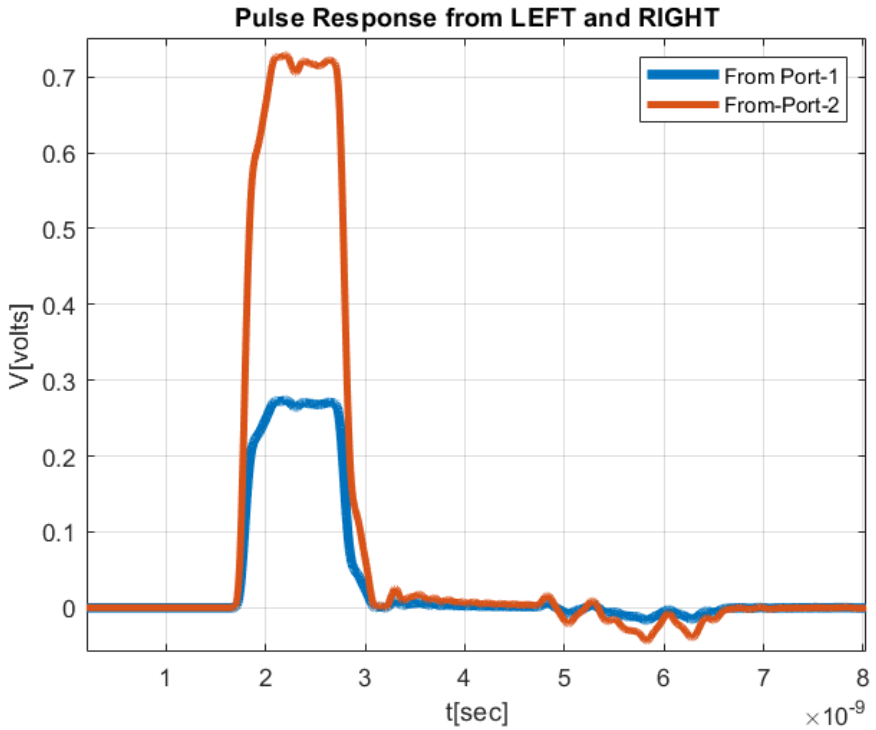
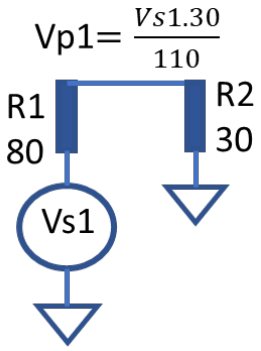


Figure 1: Simple topology, (capacitor close to one end)

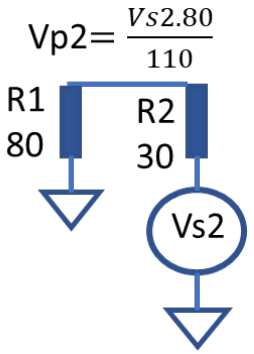


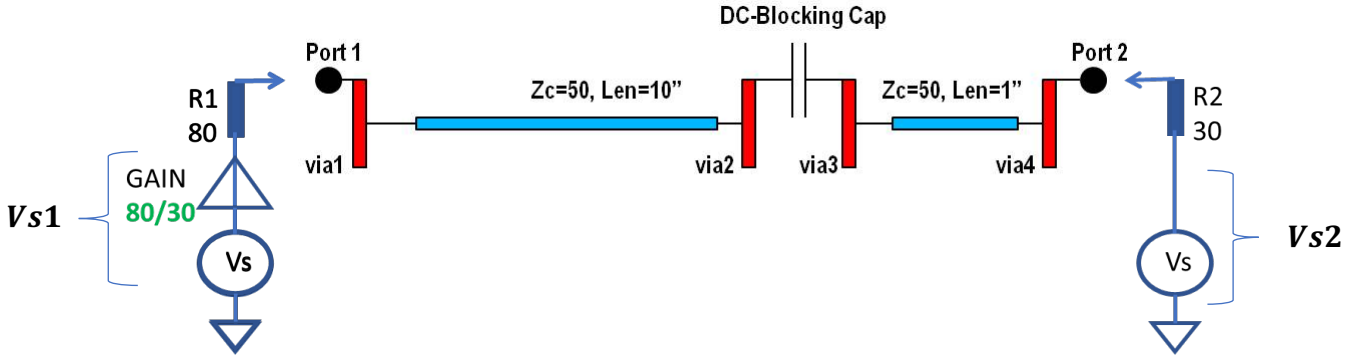


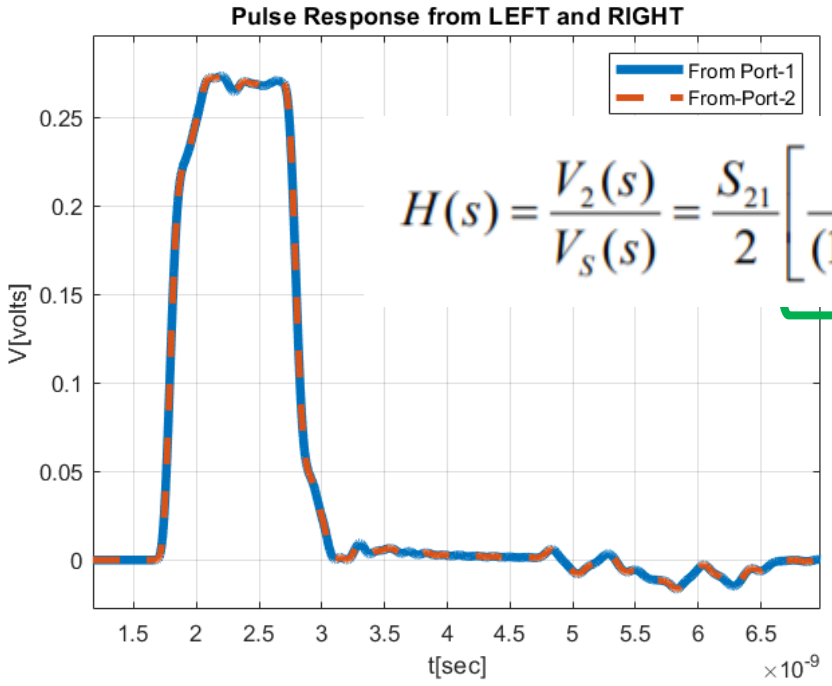
REALLY? (LET'S LOOK AGAIN)



If we want:
Vp1 == Vp2
Vs1= $\frac{Vs2.80}{30}$





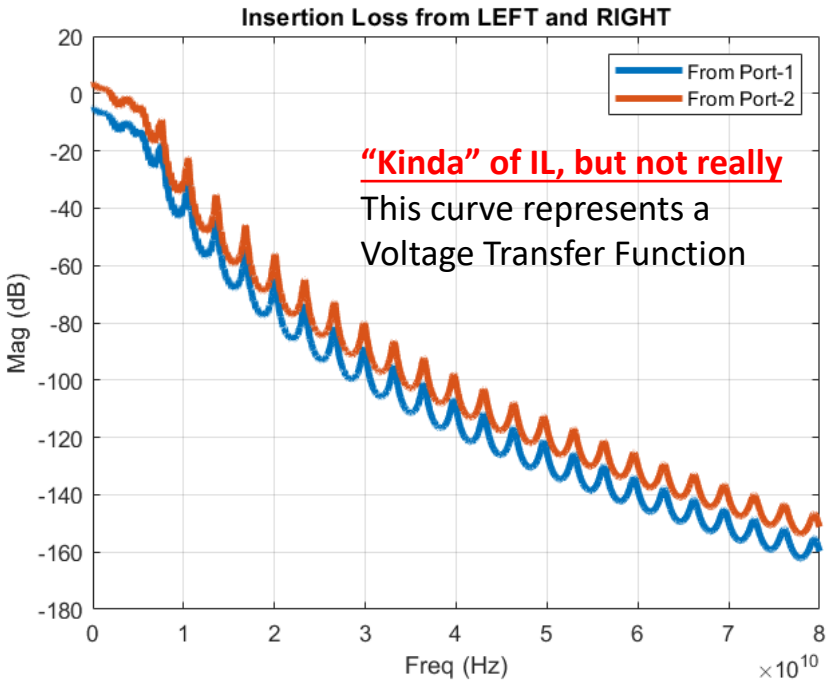


Gain

$$H(s) = \frac{V_2(s)}{V_S(s)} = \frac{S_{21}}{2}\left[\frac{(1-\Gamma_S)(1+\Gamma_L)}{(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{12}S_{21}(\Gamma_S\Gamma_L)}\right]$$

Denominator does not change

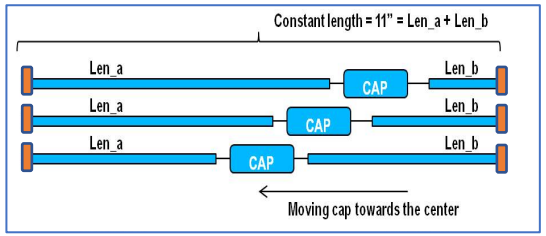
Even on the reflective case, H(s) is the same with the exception of a constant gain

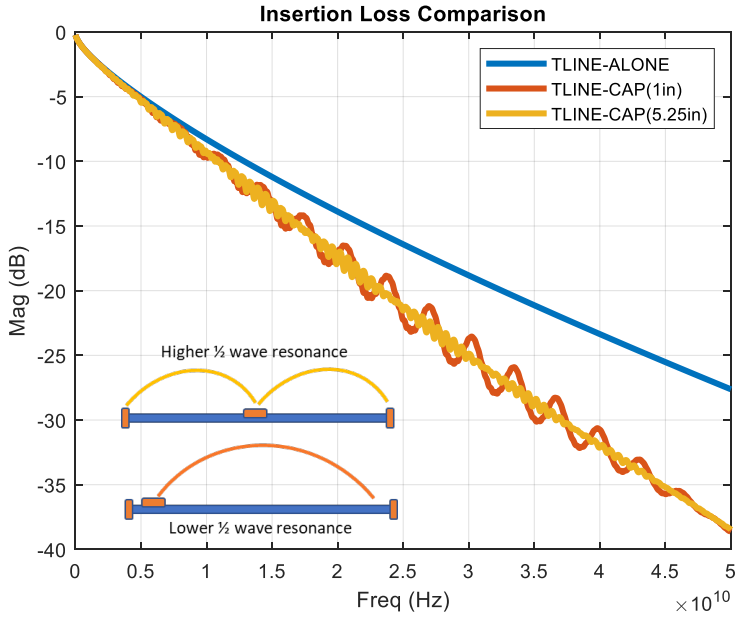


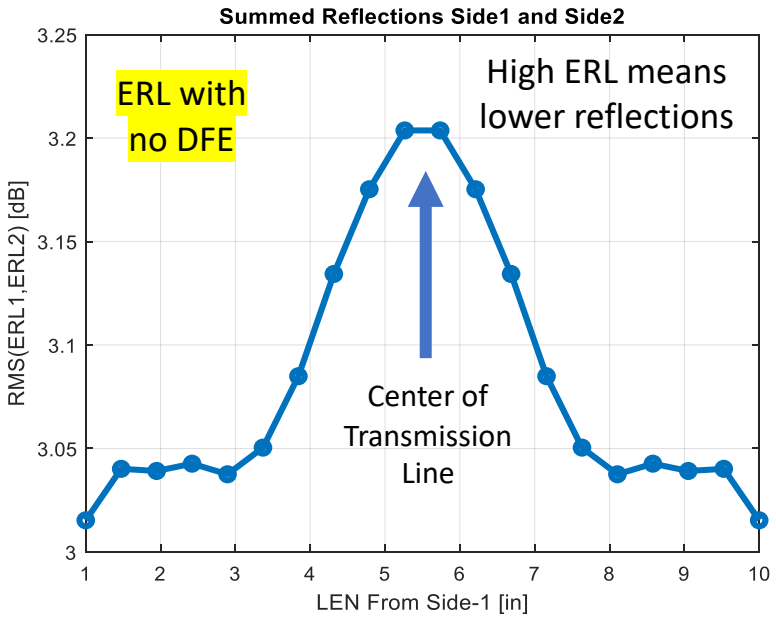
"Kinda" of IL, but not really
This curve represents a Voltage Transfer Function

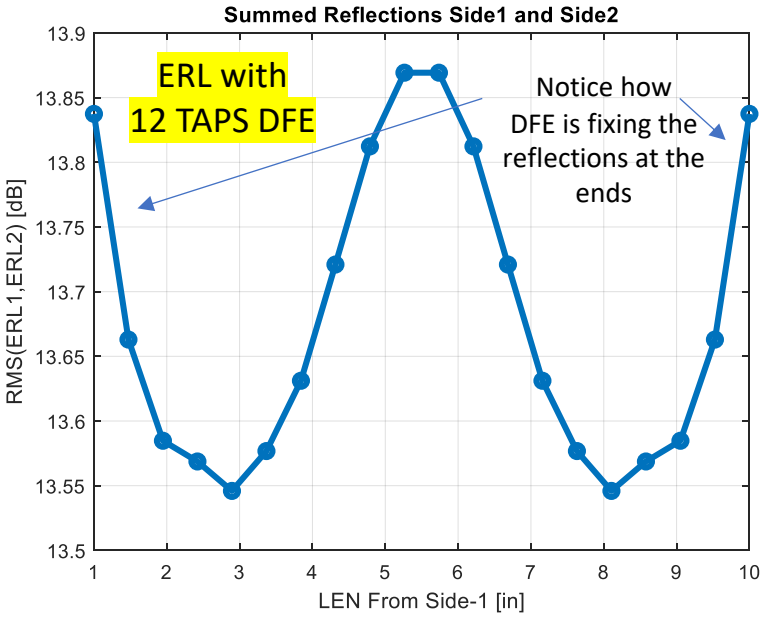
REFLECTIONS vs. POSITION

- How can we lower the reflections **simultaneously** at both ends?
- Let's do the following experiment:
  - Add Tx/Rx 200fF at the ends
  - Sweep location of DC-Blocking cap discontinuity
  - Compute ERL at side-1 and side-2 and and power-sum
    The bigger this number the less reflections -20log(V reflected)





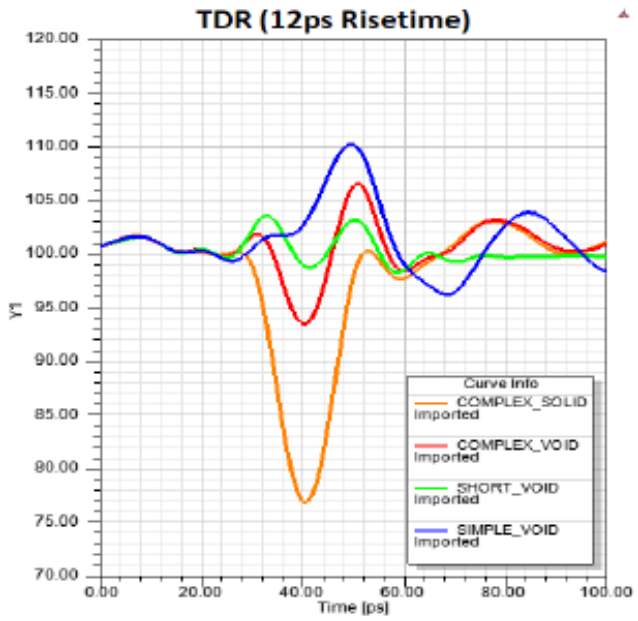


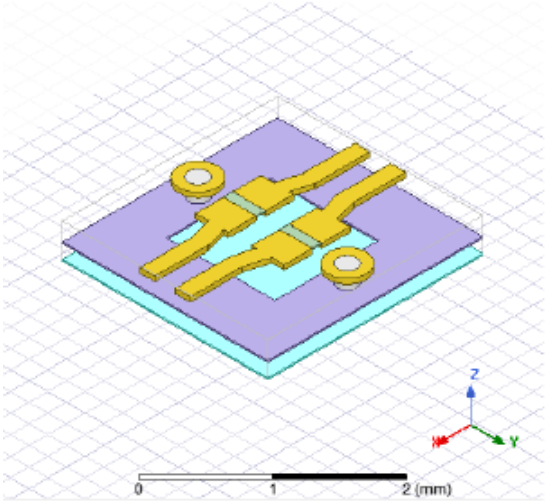


SOLUTION IS SYSTEM DEPENDENT, BUT KEEP IN MIND THE TRENDS AND USE IT TO YOUR ADVANTAGE.

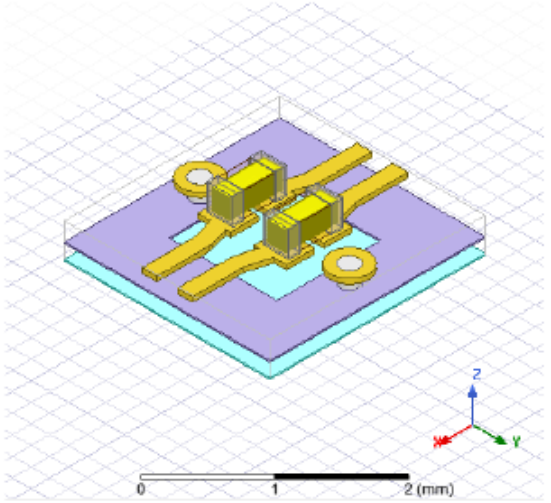
LET'S MINIMIZE DISCONTINUITIES

- Different ways to model DC-Blocking caps
- Important to reduce discontinuities

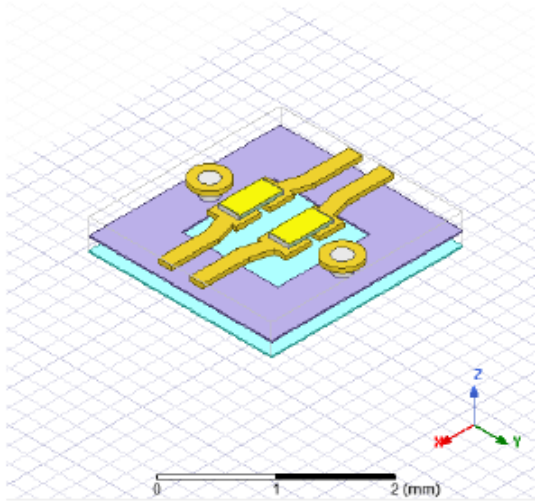




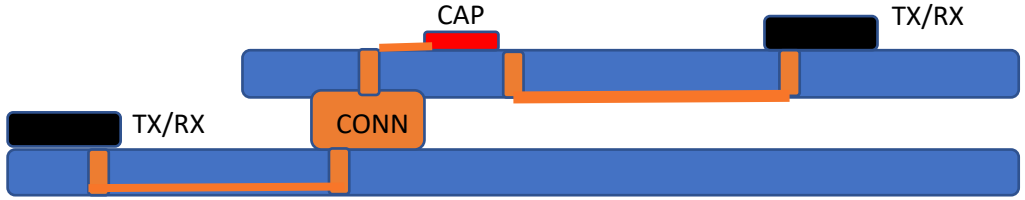
SHORT_VOID



COMPLEX_VOID



SIMPLE_VOID



TO CONCLUDE

- Same voltage transfer function, when driven from either side (+ Gain in unmatched cases)
- Reduce discontinuities by **simulating** your transitions
- Best capacitor location should be determined by understanding the **complete topology** including other discontinuities,
  (use losses to your advantage!!)

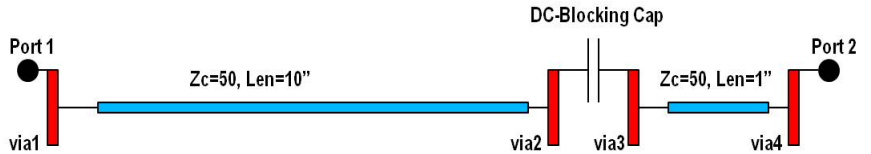
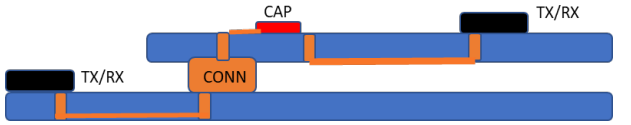
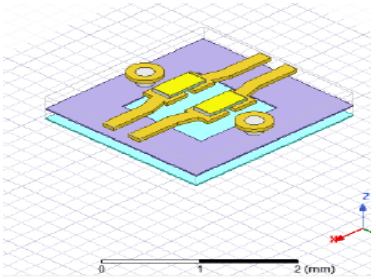
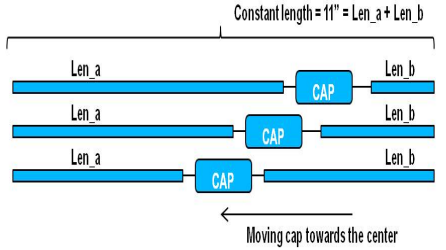


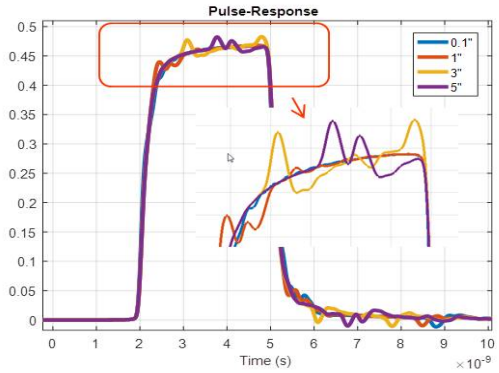
Figure 1: Simple topology, (capacitor close to one end)





SIMPLE_VOID





REFERENCES

- **Signal Integrity Journal Article**
  - https://www.signalintegrityjournal.com/authors/61-gustavo-j-blando
- **DC-Blocking Cap Paper**
  - Designing DC-Blocking Capacitor Transitions to Enable 56Gbps NRZ & 112Gbps PAM4 (Scotty Neally, Scott McMorrow), DesignCon 2018
- **ERL Reference Material**
  - http://www.ieee802.org/3/cd/public/adhoc/archive/mellitz_080217_3cd_02_adhoc.pdf
  - https://www.signalintegrityjournal.com/events/45-effective-return-loss-for-112g-and-56g-pam-4
- **DFE Reference Material**
  - http://emlab.uiuc.edu/ece546/Lect_27.pdf

For information about Samtec's gEEk® spEEk presentations,
contact: **gEEkspEEk@samtec.com**

For Signal Integrity questions, contact: SIG@samtec.com

To view previous gEEk® spEEk webinar recordings,
go to www.samtec.com/geekspeek