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PCI Express® - Is 85 ohms really needed?

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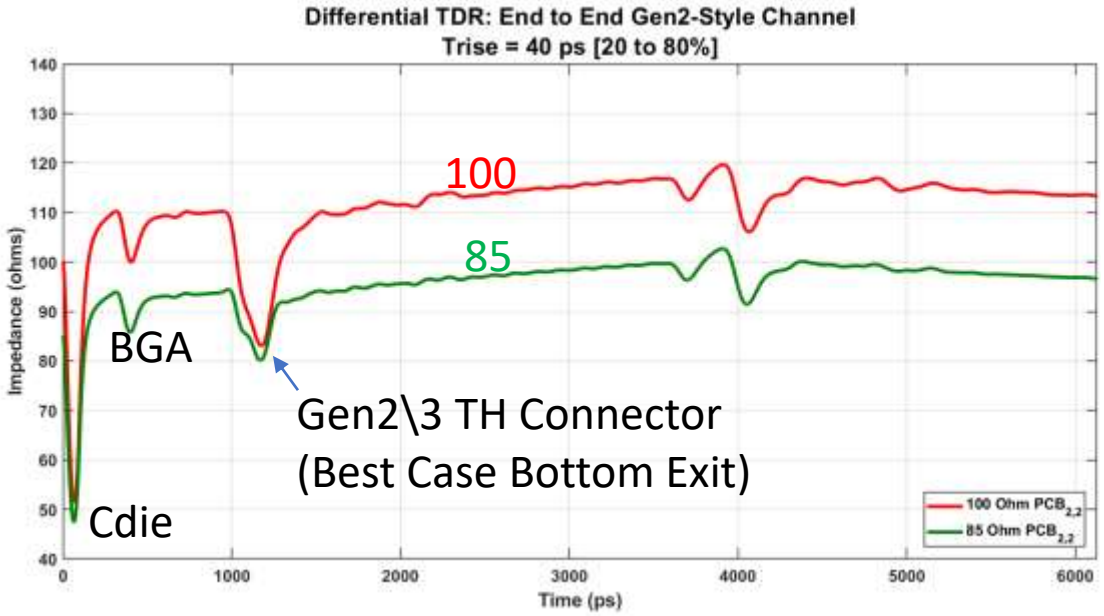
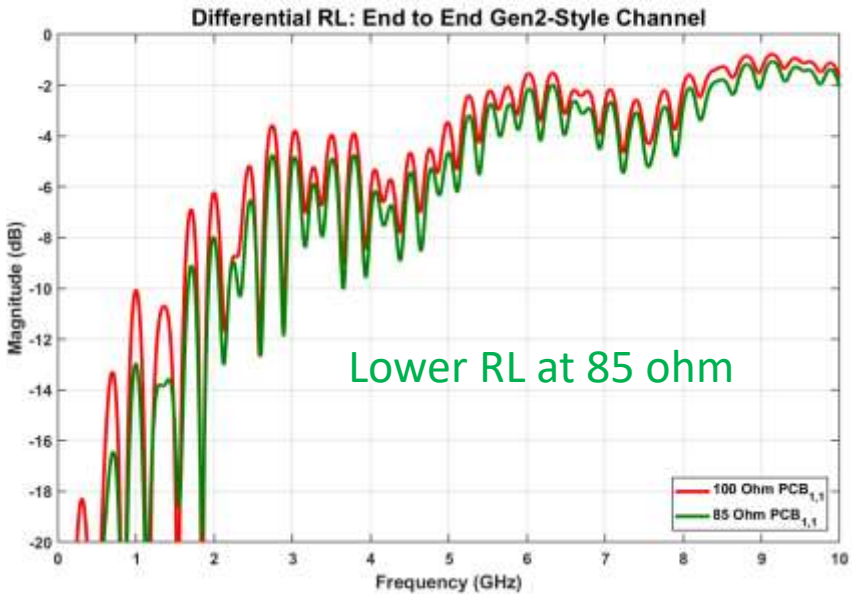
Introduction

- In PCIe® system designs, we want the design to follow the mantra of 85 ohm applications to our packages, traces, connectors, cables, and now, our vias.
- We believe we are trying to follow what the specification says is required – and that 85 ohm is optimal.
- However, sometimes 85 ohm components are not available. **Why is this?**
- And then, supplier devices may be terminated to 100 ohms.
- What should we do?

History: The Path to 85 ohms

- Near year 2000, a wider trace width to reduce trace-cracking has an SI benefit
- TX C-Die, package BGA, and connector PTH are experiencing ≤ 70 ohms
- Package socket/LGA and connectors are ≥ 100 ohms
- PCB routing at 85 ohm offers reduced reflections, balancing low + highs between the low and high impedances throughout the signal path





The Bottom Line on Specification:

- 85 ohms required for interoperable systems and cards
- 85 ohms does not apply to packages
- PCB for captive, or custom, systems do not require 85 ohms
- Connectors do not require 85 ohms
- Cables are not bound to 85 ohms

4.7.8. Differential Data Trace Impedance

The PCB trace pair differential impedance for a 5.0 GT/s capable data pair must be in the range of 68 Ω to 105 Ω. The PCB trace pair differential impedance for an 8.0 GT/s capable data pair must be in the range of 70 Ω to 100 Ω. These limits apply to both the add-in card and the system board.

Notes
- Motherboards with long (high loss) channels may need to have tighter impedance control.
- This requirement does not apply to vias, the connectors, package traces, cables, and other similar structures.
- Designs should still attempt to minimize the impedance discontinuities from vias, the connectors, package traces, cables, and other similar structures.

IMPLEMENTATION NOTE

Differential PCB Trace Impedance

The PCB trace impedance requirement specified in Section 4.7.8 only applies to topologies that support 5.0 GT/s or 8.0 GT/s covered by this form factor specification that use the connector defined in this form factor specification.

Specifically, the *PCI Express Card Electromechanical Specification* covers the following two topologies (as defined in Section 4.6.1):

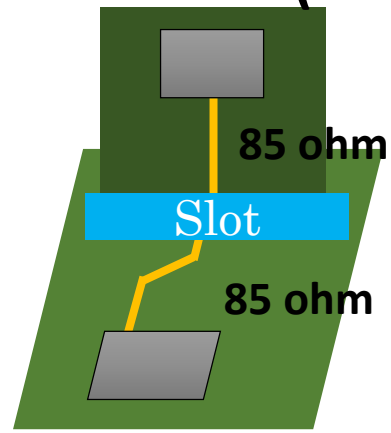
PCI Express devices across one card electromechanical connector on a system with a system board and an add-in card

PCI Express devices across two card electromechanical connectors on a system with a system board, a riser card, and an add-in card, where the connector between the riser card and the add-in card is a card electromechanical connector.

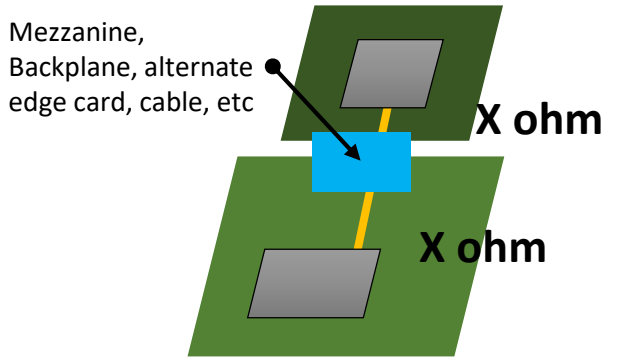
Other topologies governed by different specifications may impose different impedance requirements or leave the impedance unspecified.

For example, the topology of "PCI Express devices on the same system board" does not fit within a form factor specification and hence must only follow the requirements of the *PCI Express Base Specification*. The *PCI Express Base Specification* does not define a PCB trace impedance requirement so with this topology designers can choose the PCB trace impedance that is best for their applications.

Add In Card (CEM)



Captive Link (Everything Else)



Considerations for PCB Impedance

Motivators for 85 ohms

- Lower PCB loss than 100 ohm in same stack up
- May be best match for the densest BGA designs
- Easier to achieve on high layer count stack up
- Package impedance most devices 85 ohms
- Device termination at 100 ohms is effectively lowered by parallel die capacitances
- Reduced crosstalk on same stack up
- More tolerant to impedance variation

Motivators for alternative 92.5 or 100 ohms

- May be better match for non-CEM connectors
- Devices supporting multiple I/O may not be 85 ohms

How to decide?

First review S-parameter, then the only normative method is full channel simulation.

4.3.6.4. 8.0 GT/s Channel Compliance Testing

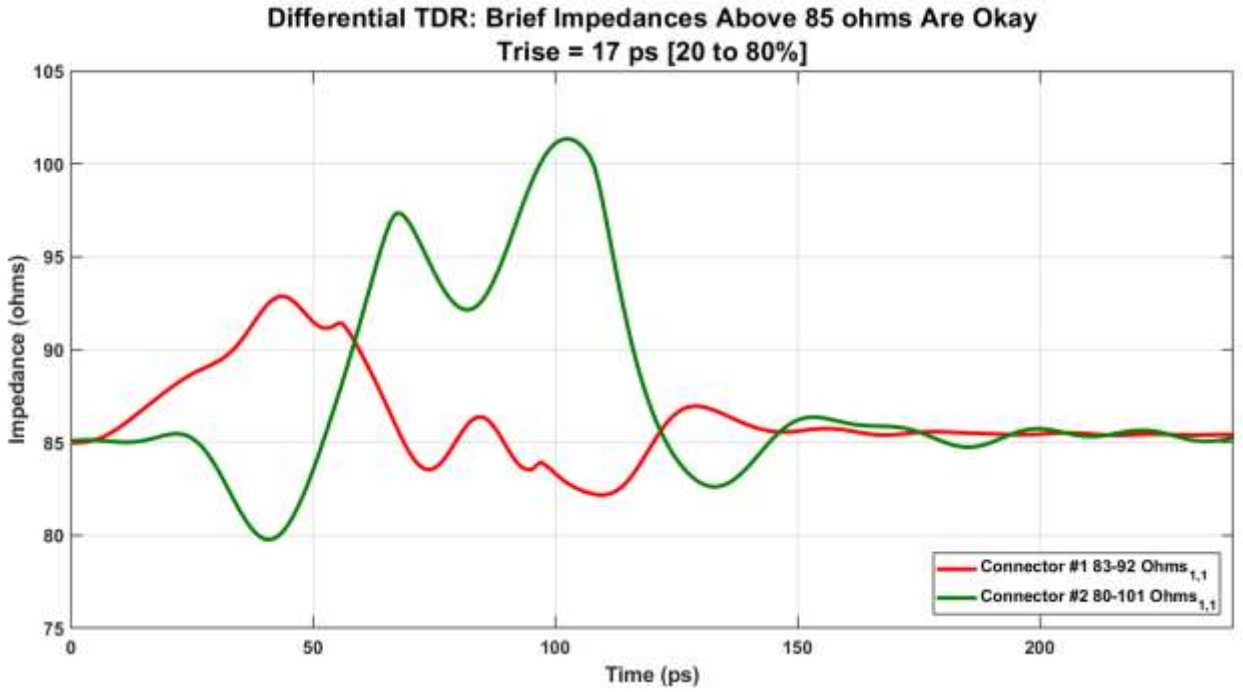
This section of the specification is relevant only for those cases where a platform design comprehends the relevant channel between transmitter device pins and receiver device pins. These types of platform designs are called "captive channels". Designs that are not captive channels shall refer to the appropriate form factor (CEM) specification, since in this case the CEM specification takes precedence over the base specification.

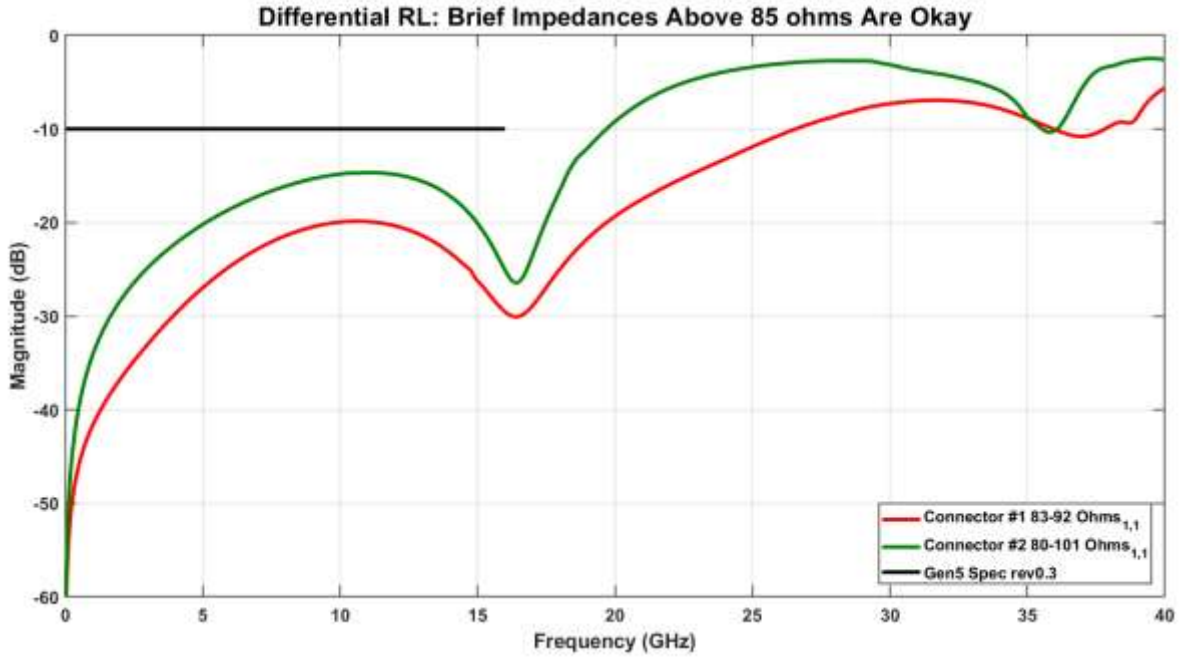
Table 4-27: Channel Tolerancing Eye Mask Values

Symbol	Parameter	Value	Units	Comments
$V_{RX-CH-EH}$	Eye height	25 (min)	mVPP	Eye height at BER=10^{-12}. Note 1.
$T_{RX-CH-EW}$	Eye width at zero crossing	0.3 (min)	UI	Eye width at BER=10^{-12}
$T_{RX-DS-OFFSET}$	Peak EH offset from UI center	±0.1	UI	See Figure 4-87 for details.
V_{RX-DFE_COEFF}	Range for DFE d_1 coefficient	±30	mV	See Figure 4-70 for details.

Components Today: Outside of 85 Ohms is OK

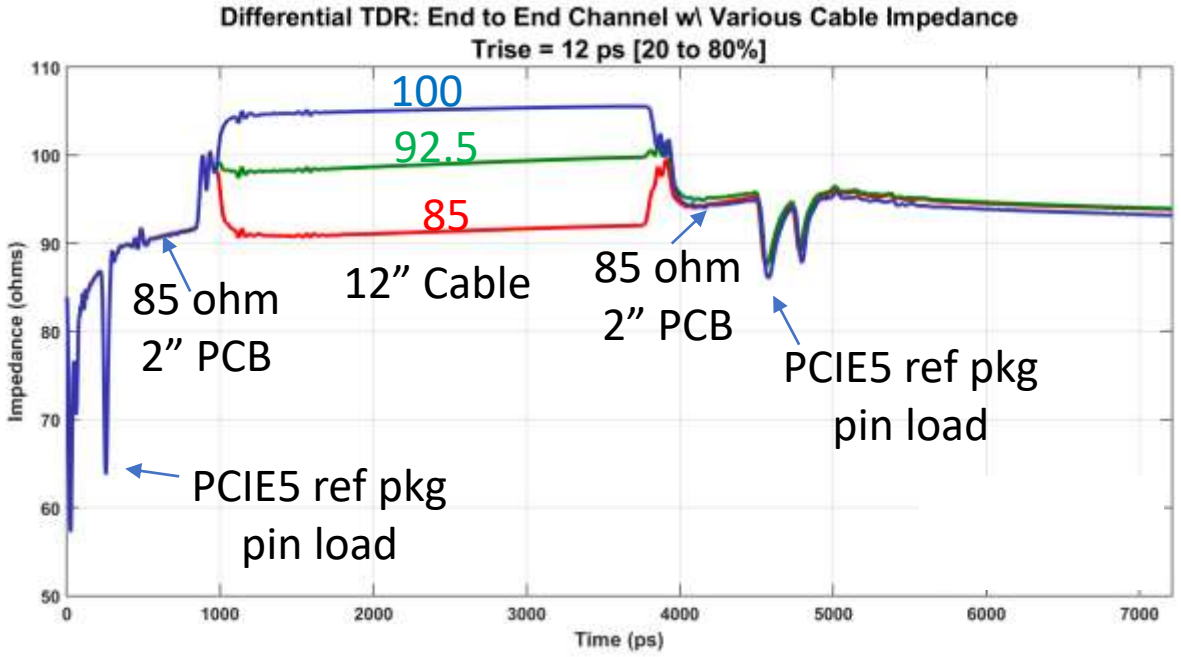
- Exposure to air - sockets and connectors - raise impedance above 85 ohms
- Gen 3/Gen 4 era SMT connectors may be near 120 ohms
- Two examples: Up to 92 ohms and up to 101 ohms for Gen 5 Compliant
  - Both case significantly below -10dB targets and acceptable in PCIe® use

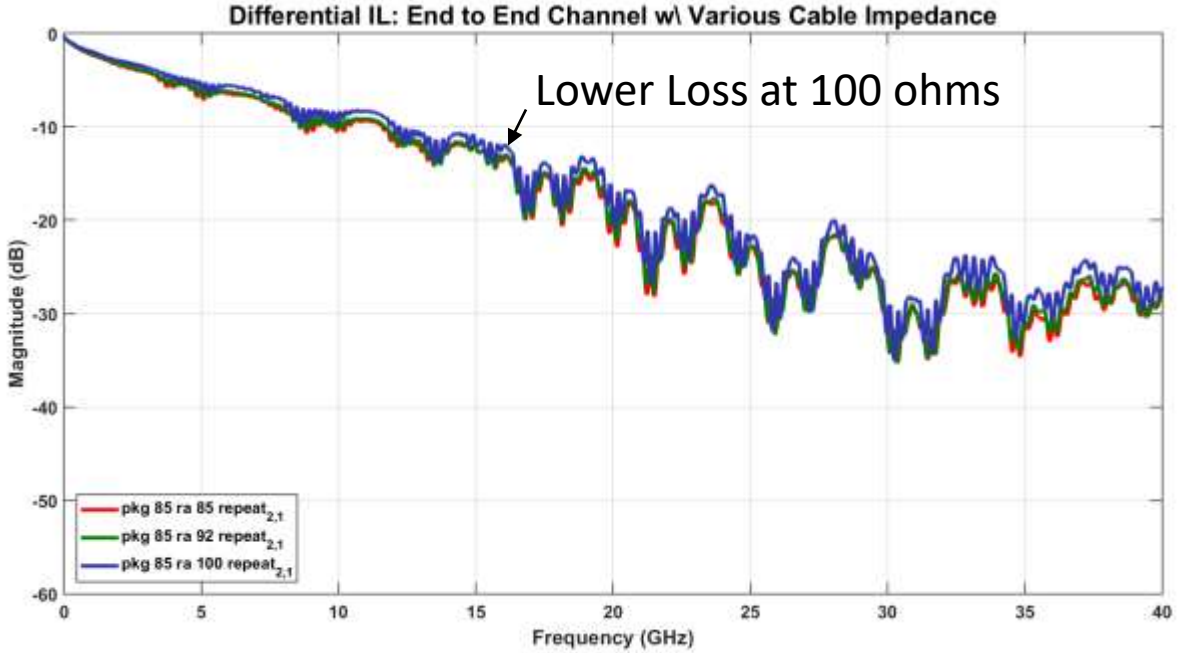




Cable Consideration

- Higher impedance twinax is lower loss (opposite of PCB)
  - For longer cables, significant gains can be made with 100 ohms
- We are tempted to select cable impedance by PCB impedance
  - Yet most relevant reflections are from the attached connector body

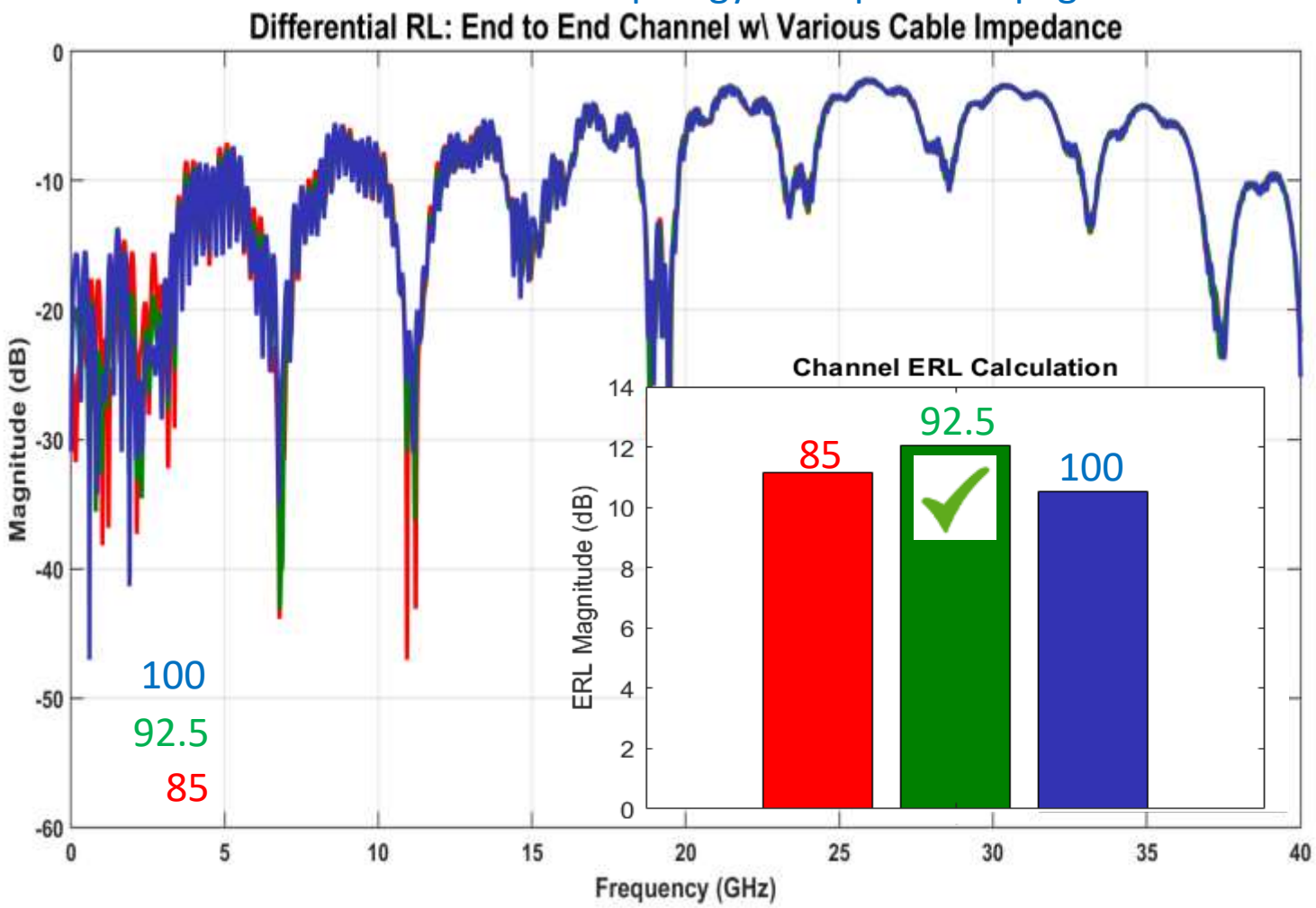




RL Challenge: Which is better?

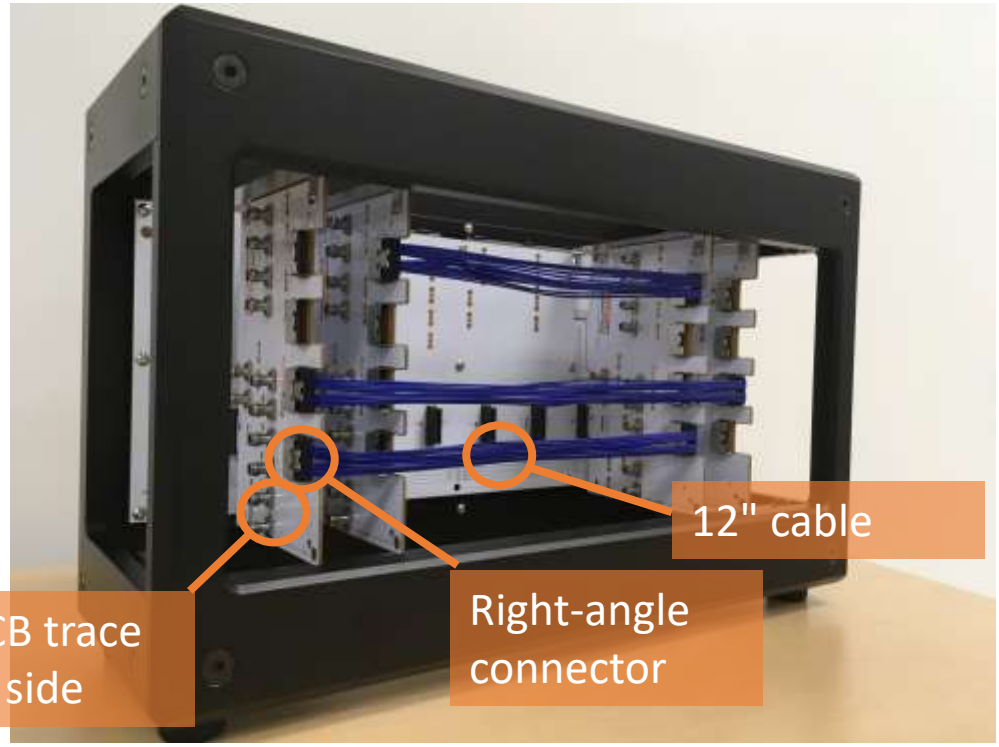
- Often RL curves look too similar
- May be difficult to assess optimal impedance choice
- Differences look negligible, and they probably are
- Channel simulation is best, but costly in time/setup
  - Channel simulation is the only normative compliance for non-CEM
- In lieu of simulation we can evaluate reflection metrics
  - ERL, RILN, IMR, IRL, etc.
- Single value metrics help us decide / fine tune without completing channel simulation

End-to-End Cable Topology from previous page

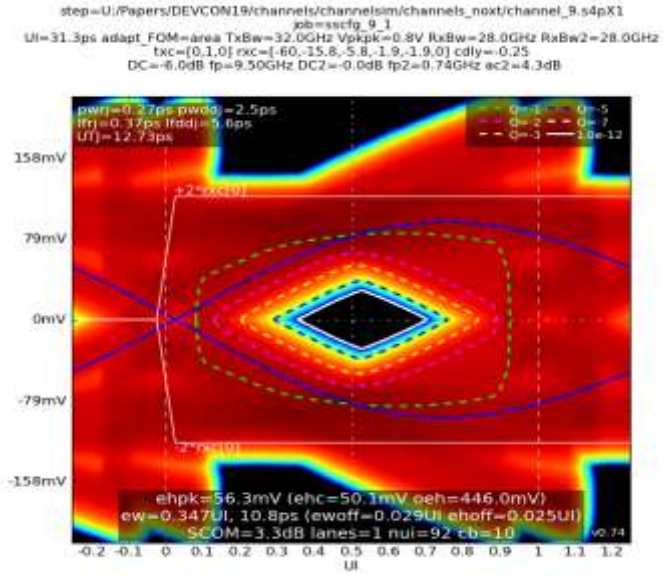


Example: High Speed Cable Assembly

- Simulation of channel topology with right-angle cable assembly
  - 2" PCB trace at 85 ohms & 12" cable at 85 or 100 ohms



Gen5 Channel Simulation Results



	Eye Height	Eye Width
85 ohm cable	48mV	0.31UI
100 ohm cable	56mV	0.34UI

Summary

- The specification allows for much flexibility in selection of connectors, cables, and traces with only exception to the CEM form factor.
- Expect to continue to see 85 ohm used most commonly, with a rise in 92 ohm applications.
- Connectors and cables may offer improved system performance at impedances other than 85 ohms – case by case diligence is needed.

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